**3GPP TSG RAN WG1 #103-e R1-20xxxxx**

**e-Meeting, October 26 – November 13, 2020**

**Source: Moderator (MediaTek)**

**Title: Email discussion on the switch delay of DCI-based multi BWP switch simultaneously**

**Agenda item: 5**

**Document for:** **Discussion and Decision**

Introduction

In RAN1#103-e meeting, an LS from RAN4 was received on DCI-based multiple BWP switch simultaneously [1] and the following question is drawn from RAN4:

* RAN4 is wondering if the DCI-based multiple BWP switch delay defined in RAN4 can be supported with existing DCI based signalling for UE’s PDSCH reception and PUSCH transmission and will be applied for HARQ processing timeline in dormancy SCell’s design.

Several related contributions on discussion and draft reply LS were submitted in this meeting [2]-[5]. As guided by the Chairman, this contribution provides a summary of the submitted contributions, discussion points and outcomes of email discussion during this meeting.

[103-e-AI5-LS-02] For LS in [R1-2007506](file:///C:\Users\wanshic\OneDrive%20-%20Qualcomm\Documents\Standards\3GPP%20Standards\Meeting%20Documents\TSGR1_103\Docs\R1-2007506.zip), a reply LS may be necessary – email discussion/approval till 11/2 – MTK (name TBD)

Discussion points (phase 1 until 28-Oct)

Based on the submitted inputs [2]-[5], for the current RAN4-defined multiple BWP switch delay:

Where,

is the single-CC BWP switch delay defined in TS38.133;

D: incremental delay for BWP switch processing on additional CCs based on UE’s capabilities.

* + Type 1 UE: D = 100us, 200us
  + Type 2 UE: D = 200us, 400us, 800us, 1000us

all companies observed that, when the number of simultaneous BWP switching on CCs is large (e.g. for SCell dormancy’s application), the delay of DCI-based multiple BWP switch simultaneously may be larger than the existing maximum K0, K1, K2 (32 slots for K0 and K2, 15 slots for K1), which is not allowed in RAN1 spec.

For this issue, two companies [2][3] proposed to let RAN4 remove D=800us/1000us to alleviate this problem. One company [4] shows that for D=200us, 400us, 800us, 1000us, the maximum value (32) of K0 and K2 restricts UE to be not able to switch the maximum number (16) of configured CC for some SCS, and suggest RAN4 to discuss further. One company [5] thinks the issue can be tackled through network implementation by scheduling less SCells to switch (dormant) BWP simultaneously.

The following questions are devised in order to formulate potential answers to RAN4’s questions. Companies are encouraged to provide their inputs below.

Question 1 (Maximum value of K0/K1/K2):

**Do you agree the maximum value of K0, K1, K2 (32 slots for K0 and K2, 15 slots for K1), should NOT be changed?**

|  |  |  |
| --- | --- | --- |
| **Company** | **Yes/No** | **Comment** |
| vivo | Y |  |
| ZTE | Yes | As least for Rel-16, we may not need to increase the maximum value of K0, K1, K2. But this can be further considered in future release. |
| Huawei, HiSilicon | Y |  |
| Nokia, NSB | Yes |  |
| Qualcomm | Yes |  |
| CATT | Yes |  |
| Ericsson | Yes |  |
| MTK | Yes |  |
| Samsung | Yes | The maximum value of K0, K1 and K2 should not be increased in Rel-16. |
| Spreadtrum | Yes |  |

Question 2 (Information to RAN4 about UE’s PDSCH reception and PUSCH transmission timeline):

**RAN4 inquires whether the DCI-based multiple BWP switch delay defined in RAN4 can be supported with existing DCI based signalling for UE’s PDSCH reception and PUSCH transmission. Do you agree to inform RAN4 the “maximum allowed number of CCs for simultaneous BWP switching using scheduling DCI” for different SCS configurations shown below to RAN4 as derived in [3]?**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| SCS | Single BWP switch delay (ms)  Type 1 / Type 2 | Maximum allowed number of CCs for simultaneous BWP switching using scheduling DCI   * with corresponding to be T (ms) | | Existing maximum K0/K2 (ms)  (Serve as upper bound of  ) |
| 15 | 1 / 3 | Type 1 UE:  For D=100us: 16 CC   * T = 2.5   For D=200us: 16 CC   * T = 4 | Type 2 UE:  For D=200us: 16 CC   * T = 6   For D=400us: 16 CC   * T = 9   For D=800us: 16 CC   * T = 15   For D=1000us: 16 CC   * T = 18 | 32 |
| 30 | 1 / 2.5 | Type 1 UE:  For D=100us: 16 CC   * T = 2.5   For D=200us: 16 CC   * T = 4 | Type 2 UE:  For D=200us: 16 CC   * T = 5.5   For D=400us: 16 CC   * T = 8.5   For D=800us: 16 CC   * T = 14.5   For D=1000us: **14 CC**   * T = 15.5 | 16 |
| 60 | 0.75 / 2.25 | Type 1 UE:  For D=100us: 16 CC   * T = 2.25   For D=200us: 16 CC   * T = 3.75 | Type 2 UE:  For D=200us: 16 CC   * T = 5.25   For D=400us: **15 CC**   * T = 7.85   For D=800us: **8 CC**   * T = 7.85   For D=1000us: **6 CC**   * T = 7.25 | 8 |
| 120 | 0.75 / 2.25 | Type 1 UE:  For D=100us: 16 CC   * T = 2.25   For D=200us: 16 CC   * T = 3.75 | Type 2 UE:  For D=200us: **9 CC**   * T = 3.85   For D=400us: **5 CC**   * T = 3.85   For D=800us: **3 CC**   * T = 3.85   For D=1000us: **2 CC**   * T = 3.25 | 4 |

|  |  |  |
| --- | --- | --- |
| **Company** | **Yes/No** | **Comment** |
| vivo | Y | This will provide clear information to RAN4 about the actual scheduling restriction based on the current RAN4 assumption on delay requirements. |
| ZTE | Yes | We are ok to add this table in the LS. |
| Huawei, HiSilicon | Ok |  |
| Nokia | Partially | We are not sure whether the numbers of CCs are correct. For example, in 120kHz and with D=1000us and K2 for UL grant (DCI format 0\_1 or 1\_1), 1 Scell BWP switching requires at least 19+8 =27 slots and 2 Scell require 27+8=35slots > 32. So RAN1 spec support 1 Scell not 2 with UL grant or DL assignment. |
| Qualcomm | Yes | RAN1 should also provide some details to RAN4 for how the table is created so that RAN4 can verify RAN1’s analysis. |
| CATT | Yes |  |
| Ericsson | No | Instead of detailed tables, prefer to indicate to RAN4 that some combinations result in scheduler restriction due to k0, k1, k2 limits and as a consequence maximum allowed number of CCs for simultaneous BWP switching using scheduling DCI may be different in different cases. |
| MTK | Yes | About Nokia’s comment, the table list BWP switching for multiple CC, not specific to SCell (since PCell can also do BWP switching when indicating SCell to do dormant BWP switching). Therefore, for 120kHz and D=1000us, 2CC switching for Type 2 UE requires 18+8=26 slots < 32. |
| Samsung | Yes |  |
| Spreadtrum | Yes | Support add this table in LS. |

Question 3 (Information to RAN4 about UE’s HARQ ACK timeline):

**RAN inquires whether the DCI-based multiple BWP switch delay defined in RAN4 can be supported with existing DCI based signalling for UE’s HARQ ACK timeline. Do you agree to inform RAN4 the “maximum allowed number of CCs for simultaneous BWP switching using non-scheduling DCI” for different SCS configurations shown below to RAN4?**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| SCS | Single BWP switch delay (ms)  Type 1 / Type 2 | Maximum allowed number of CCs for simultaneous BWP switching using non-scheduling DCI   * with corresponding to be T (ms) | | Existing maximum K1 (ms)  (Serve as upper bound of  ) |
| 15 | 1 / 3 | Type 1 UE:  For D=100us: 16 CC   * T = 2.5   For D=200us: 16 CC   * T = 4 | Type 2 UE:  For D=200us: 16 CC   * T = 6   For D=400us: 16 CC   * T = 9   For D=800us: 16 CC   * T = 15   For D=1000us: **13** CC   * T = 15 | 15 |
| 30 | 1 / 2.5 | Type 1 UE:  For D=100us: 16 CC   * T = 2.5   For D=200us: 16 CC   * T = 4 | Type 2 UE:  For D=200us: 16 CC   * T = 5.5   For D=400us: **13** CC   * T = 7.3   For D=800us: **7** CC   * T = 7.3   For D=1000us: **6 CC**   * T = 7.5 | 7.5 |
| 60 | 0.75 / 2.25 | Type 1 UE:  For D=100us: 16 CC   * T = 2.25   For D=200us: 16 CC   * T = 3.75 | Type 2 UE:  For D=200us: **8** CC   * T = 3.65   For D=400us: **4 CC**   * T = 3.45   For D=800us: **2 CC**   * T = 3.05   For D=1000us: **2 CC**   * T = 3.25 | 3.75 |
| 120 | 0.75 / 2.25 | Type 1 UE:  For D=100us: 12 CC   * T = 1.85   For D=200us: 6 CC   * T = 1.75 | Type 2 UE:  For D=200us: **0 CC**   * 2.25 > 1.875   For D=400us: **0 CC**   * 2.25 > 1.875   For D=800us: **0 CC**   * 2.25 > 1.875   For D=1000us: **0 CC**   * 2.25 > 1.875 | 1.875 |

|  |  |  |
| --- | --- | --- |
| **Company** | **Yes/No** | **Comment** |
| vivo | Y | This will provide clear information to RAN4 about the actual scheduling restriction based on the current RAN4 assumption on delay requirements. |
| ZTE | Yes | We are ok to add this table in the LS. |
| Huawei, HiSilicon | OK |  |
| Nokia, NSB | No | We think that reference point for K1 value should be relative to slot of DCI + indicted K0 in DCI format 1\_1 indicating dormancy (without PDSCH). This would provide similar numbers of CCs as for DCI formats scheduling PUSCH and PDSCH. |
| Qualcomm | Yes |  |
| CATT | Yes |  |
| Ericsson | No | Instead of detailed tables, prefer to indicate to RAN4 that some combinations result in scheduler restriction due to k0, k1, k2 limits and as a consequence maximum allowed number of CCs for simultaneous BWP switching using scheduling DCI may be different in different cases. |
| MTK | Yes | The RAN1 timeline information can be useful for RAN4. |
| Samsung | Yes |  |
| Spreadtrum | Yes | Support this table in the LS |

Question 4 (RAN4-defined D value):

**For D=200us, 400us, 800us, 1000us, the maximum value (32) of K0 and K2 restricts UE to be not able to switch (dormant) BWP for the maximum number (16) of configured CC for some SCS. Do you agree to suggest RAN4 to remove some of the large D values? If you agree, please indicate which D values you prefer to suggest RAN4 to remove in the comment.**

|  |  |  |
| --- | --- | --- |
| **Company** | **Yes/No** | **Comment** |
| vivo | N | We think the information related to Question 1/2/3 is sufficient as reply to RAN4 from RAN1 perspective. It will be up to RAN4 to discuss and decide if any D value can be removed. |
| ZTE | Yes | We propose to remove at least 800us and 1000us. We believe it is beneficial to give some suggestion on the removed values from RAN1 perspective, but whether it should finally be removed can be determined by RAN4. |
| Huawei, HiSilicon | Y | It is always possible for RAN1 to have further information as needed to tell RAN4. From our perspective we are Ok to remove those higher values and also Ok with leaving those cases for network implementation, given the late stage. |
| Nokia, NSB | No | We think D=800us and 1000us should be dropped, current deployments in FR2 support 3(7) SCells, enabling dormancy on 1 Scell out of those, provides no meaningful power saving anyway. |
| Qualcomm | No | Similar to vivo, this should be up to RAN4 decision jointly based on RAN1’s analysis of the issues and their rationale in defining the large D values. |
| CATT | No | We share the view with vivo and Qualcomm that this is up to RAN4 to make any change with RAN1 feedback on the supporting number of CCs for each D |
| Ericsson | Yes | RAN1 can suggest to RAN4 to consider removing certain D values (e.g. 800us and 1000us) for Type 2 UEs and leave final decision to RAN4. |
| MTK | Yes | Same view as Ericsson. RAN1 can suggest to RAN4 to consider removing certain D values (e.g. 800us and 1000us) for Type 2 UEs and leave final decision to RAN4. |
| Samsung | Yes | We agree to suggest RAN4 to remove some large D values, but the final decision is up to RAN4. |
| Spreadtrum | Yes | Agree with ZTE/HW… |

Proposed reply LS answers / outcome (phase 2 until 02-Nov)

**Overall Description:**

RAN1 thanks RAN4 for the LS and sharing the latest progress in RAN4 on DCI-based multiple BWP switch simultaneously. Regarding RAN4’s questions to RAN1, the following includes RAN1’s answers.

**Q:** RAN4 is wondering if the DCI-based multiple BWP switch delay defined in RAN4 can be supported with existing DCI based signalling for UE’s PDSCH reception and PUSCH transmission and will be applied for HARQ processing timeline in dormancy SCell’s design.

**Answer:** For the SCells dormant BWP switch using PCell scheduling DCI 1\_1/0\_1, the scheduled PDSCH/PUSCH is transmitted k0/k2 slots after receiving the DCI with the maximum value of k0/k2 being 32. Since the scheduled PDSCH/PUSCH need to happen after the multiple SCells dormant BWP switch, it induces scheduling restriction to maximum number of SCells for simultaneous dormant BWP switching using PCell scheduling DCI. For instance, for Type 2 UE with the incremental delay (D) values being 800us/1000us and FR2 CA with SCS = 120kHz for PCell and SCells, NW can schedule at most 2 SCells to perform dormant BWP switch at one time using the PCell scheduling DCI 1\_1/0\_1. To speed up the processing timeline with multi-SCells dormancy indication, RAN1 suggests RAN4 to further discuss the incremental delay (D) values for Type 2 UE.

RAN1 also provides a table below for RAN4’s reference, which assumes the same SCS for PCell and SCells, and the PCell scheduling DCI is received after the first 3 OFDM symbols of a slot:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| SCS | Single SCell dormant BWP switch delay (ms)  Type 1 / Type 2 | Maximum number of SCells for simultaneous dormant BWP switching using PCell scheduling DCI   * with corresponding to be T (ms) | | Existing maximum K0/K2 (ms)  (Serve as upper bound of  ) |
| 15 | 3 / 5 | Type 1 UE:  For D=100us: 15   * T = 4.4   For D=200us: 15   * T = 5.8 | Type 2 UE:  For D=200us: 15   * T = 7.8   For D=400us: 15   * T = 10.6   For D=800us: 15   * T = 16.2   For D=1000us: 15   * T = 19 | 32 |
| 30 | 2 / 3.5 | Type 1 UE:  For D=100us: 15   * T = 3.4   For D=200us: 15   * T = 4.8 | Type 2 UE:  For D=200us: 15   * T = 6.3   For D=400us: 15   * T = 9.1   For D=800us: 15   * T = 14.7   For D=1000us: **13**   * T = 15.5 | 16 |
| 60 | 1.25 / 2.75 | Type 1 UE:  For D=100us: 15 SCells   * T = 2.65   For D=200us: 15 SCells   * T = 4.05 | Type 2 UE:  For D=200us: 15   * T = 5.55   For D=400us: **14**   * T = 7.95   For D=800us: **7**   * T = 7.55   For D=1000us: **6**   * T = 7.75 | 8 |
| 120 | 1 / 2.5 | Type 1 UE:  For D=100us: 15 SCells   * T = 2.4   For D=200us: 15 SCells   * T = 3.8 | Type 2 UE:  For D=200us: **8**   * T = 3.9   For D=400us: **4**   * T = 3.7   For D=800us: **2**   * T = 3.3   For D=1000us: **2**   * T = 3.5 | 4 |

**2. Actions:**

**To RAN4:**

RAN1 kindly asks RAN4 to take the above response into account for the corresponding future works.

**Question: Are the above proposed reply answer for RAN4 acceptable? If not, which part is not acceptable and any suggested modification?**

|  |  |  |
| --- | --- | --- |
| **Company** | **Yes/No** | **Comment** |
|  |  |  |
|  |  |  |

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Summary of contribution inputs

In [2], it mentions that if interruptions to SpCell exist for SCell dormant BWP switch, Option 3 in the contribution (suggest RAN4 to remove D=800us, 1000us for Type 2 UE) should be adopted:

**Proposal-1:** Ask *RAN4 to provide feedback on impact of dormancy BWP switch to SpCell receptions and transmissions.*

On the other hand, if interruptions impact also Pcell for the whole Scell BWP delay (which seems to be current RAN4 status), then if SpCell or PUCCH cell is on FR2, then e.g. for 8x100MHz ENDC deployments, i,e. 7 Scells in FR2, the TYPE2 BWP switching delay may grow to

=18slot +1slot + 1ms\*7= 19+56=75slots

However, scheduling offsets supported by RAN1 are only up to 32slots

**Observation-1:** *Dormancy BWP switching delays may be larger than maximum value of K0, K1 and K2 supported by RAN1.*

* **Option 3**: RAN4 to remove highest capabilities: Type 2 UE: D = 200us, 400us, ~~800us, 1000us.~~ that cause the issue in the first place.

Among the options our preference is Option 3, as changing reference points for K0, K1 and K2, or RRC related changes would result in too much spec change at this late stage of R16. **And with such large delays, usability of the feature is highly questionable**.

**Proposal-2:** *If interruptions to SpCell exist, adopt Option 3*

In [3], draft answers were provided to suggest RAN4 to remove D=800us, 1000us or shorten the (multi-)BWP switch delay for Type 2 UE:

With the current TBWPSwitchDelay defined by RAN4, the BWP switch delay can be quite long for D = 800us/1000us (Type 2 UE). For the dormancy indication with scheduling DCI 1\_1/0\_1, the scheduled PDSCH/PUSCH is transmitted k0/k2 slots after receiving the DCI with the maximum value of k0/k2 being 32. For the dormancy indication with non-scheduling DCI 1\_1, the corresponding HARQ-ACK feedback is transmitted *dl-DataToUL-ACK* slots after receiving the DCI with the maximum value of *dl-DataToUL-ACK* being 15. For 120kHz SCS in FR2, 32 slots corresponds to 4ms and 15 slots corresponds to 1.875ms. Since the scheduled PDSCH/PUSCH and HARQ-ACK need to happen after the multiple BWP switch, the long TBWPSwitchDelay drags the scheduling time line for SCell dormancy. To speed up the processing timeline with multi-SCells dormancy indication, RAN1 suggests RAN4 to remove the incremental delay (D) values of 800us/1000us or shorten the (multi-)BWP switch delay for Type 2 UE.

In [4], draft answers were provided to analyze the“maximum allowed number of CCs for simultaneous BWP switching” which show that for D=200us, 400us, 800us, 1000us, the maximum value (32) of K0 and K2 restricts UE to be not able to switch BWP for the maximum number (16) of configured CC for some SCS:

1. According to TS38.300, the maximum number of configured CCs for a UE is 16 for DL and 16 for UL.
2. According to TS38.331, the maximum scheduling offset for PDSCH and PUSCH are
   1. Maximum value of K0, i.e. scheduling offset between PDCCH and its scheduled PDSCH, is 32 slots
   2. Maximum value of K2, i.e. scheduling offset between PDCCH and its scheduled PUSCH, is 32 slots
3. Based on the above 1), 2) and the delay requirement for simultaneous multiple CC BWP switching as described in R4-2012269, RAN1 provides the analysis on “maximum allowed number of CCs for simultaneous BWP switching” for different SCS configurations as in the following table.

|  |  |  |  |
| --- | --- | --- | --- |
| SCS | NR Slot length (ms) | Maximum allowed number of CCs for simultaneous BWP switching | |
| 15 | 1 | Type 1 UE:  For D=100us: 16 CC  For D=200us: 16 CC | Type 2 UE:  For D=200us: 16CC  For D=400us: 16CC  For D=800us: 16CC  For D=1000us: 16CC |
| 30 | 0.5 | Type 1 UE:  For D=100us: 16 CC  For D=200us: 16 CC | Type 2 UE:  For D=200us: 16CC  For D=400us: 16CC  For D=800us: 16CC  For D=1000us: 14CC |
| 60 | 0.25 | Type 1 UE:  For D=100us: 16 CC  For D=200us: 16 CC | Type 2 UE:  For D=200us: 16CC  For D=400us: 15 CC  For D=800us: 8 CC  For D=1000us: 6CC |
| 120 | 0.125 | Type 1 UE:  For D=100us: 16 CC  For D=200us: 16 CC | Type 2 UE:  For D=200us: 9CC  For D=400us: 5 CC  For D=800us: 3 CC  For D=1000us: 2 CC |

RAN1 does not intend to change the maximum K0 or K2, which means in the cases highlighted in red, there would be restrictions to the number of CCs for simultaneous BWP switching. RAN1 expects RAN4 will discuss whether and how to capture such restrictions in their specification.

In [5], the following observations and proposals are provided:

If the BWP switching DCI schedules PDSCH or PUSCH, the relationship of BWP switching delay and maximum K0/K2 defined in TS 38.214 should be considered, i.e. the K0/K2 indicated in the DCI should be equal or larger than BWP switching delay to guarantee the PDSCH reception/PUSCH transmission. If the BWP switching DCI does not schedule PDSCH or PUSCH, e.g. case 2 PDCCH with SCell dormancy indication, the HARQ-ACK of dormancy indication is fed back on the PCell. So if the PCell BWP is switched, the maximum K1, i.e. PDSCH to HARQ timing offset, should be equal or larger than multiple BWP switching.

The possible delay of multiple BWP switching simultaneously can be derived for type 1 UE and type 2 UE as shown in Table 1 and Table 2. It can be observed that the multiple BWP switching delay may be larger than the maximum K0/K1/K2, e.g. the case that SCS is 120 kHz, D is 1ms and N is 15, multiple switching delay is 16.25ms, but the maximum K0/K2 is 4ms and maximum K1 is 1.875ms.

***Observation 1: When the number of simultaneous BWP switching on CCs is large, the delay of DCI-based multiple BWP switch simultaneously may be larger than the existing maximum K0/K1/K2.***

***Observation 2: The RAN4 conclusion leads to the cases that delay of DCI-based multiple BWP switching simultaneously is larger than existing maximum K0/K1/K2, but those cases can be avoid through network implementation.***

***Proposal 1: The delay of DCI-based multiple BWP switching simultaneously can be equal or smaller than the existing maximum K0/K1/K2 through network implementation.***

Table 1 multiple BWP switching delay for type 1 UE

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **SCS(kHz)** | **Single BWP switch delay(ms)** | **Multiple BWP extension D(ms)** | **Multiple BWP switching delay(N=7)(ms)** | **Multiple BWP switching delay(N=15)(ms)** | **Existing maximum K0/K2 (ms)** | **Existing maximum K1 (ms)** |
| 15 | 1 | 0.1 | 1.6 | 2.4 | 32 | 15 |
| 0.2 | 2.2 | 3.8 |
| 30 | 1 | 0.1 | 1.6 | 2.4 | 16 | 7.5 |
| 0.2 | 2.2 | 3.8 |
| 60 | 0.75 | 0.1 | 1.35 | 2.15 | 8 | 3.75 |
| 0.2 | 1.95 | 3.55 |
| 120 | 0.75 | 0.1 | 1.35 | 2.15 | 4 | 1.875 |
| 0.2 | 1.95 | 3.55 |

Table 2 multiple BWP switching delay for type 2 UE

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **SCS(kHz)** | **Single BWP switch delay(ms)** | **Multiple BWP extension D(ms)** | **Multiple BWP switching delay(N=7)(ms)** | **Multiple BWP switching delay(N=15)(ms)** | **Existing maximum K0/K2 (ms)** | **Existing maximum K1 (ms)** |
| 15 | 3 | 0.2 | 4.2 | 5.8 | 32 | 15 |
| 0.4 | 5.4 | 8.6 |
| 0.8 | 7.8 | 14.2 |
| 1 | 9 | 17 |
| 30 | 2.5 | 0.2 | 3.7 | 5.3 | 16 | 7.5 |
| 0.4 | 4.9 | 8.1 |
| 0.8 | 7.3 | 13.7 |
| 1 | 8.5 | 16.5 |
| 60 | 2.25 | 0.2 | 3.45 | 5.05 | 8 | 3.75 |
| 0.4 | 4.65 | 7.85 |
| 0.8 | 7.05 | 13.45 |
| 1 | 8.25 | 16.25 |
| 120 | 2.25 | 0.2 | 3.45 | 5.05 | 4 | 1.875 |
| 0.4 | 4.65 | 7.85 |
| 0.8 | 7.05 | 13.45 |
| 1 | 8.25 | 16.25 |

References

[1] R1-2007506 LS on DCI-based multiple BWP switch simultaneously, RAN4,

[2] R1-2008208 LS on DCI-based multiple BWP switch simultaneously, Nokia, Nokia Shanghai Bell

[3] R1-2008505 [draft] LS response on DCI-based multiple BWP switch simultaneously , MediaTek

[4] R1-2008652 Draft Reply LS on DCI-based multiple BWP switch simultaneously, vivo

[5] R1-2008775 On DCI-based multiple BWP switch simultaneously, Huawei, HiSilicon