TSG-RAN Working Group 1(Radio) meeting #9
30 November – 3 December 1999, Dresden, Germany

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Agenda Item : Ad hoc 14

Source : LGIC

Title : Modification of DL-DPCH format for CPCH

Document for : Discussion and approval

1. Introduction

To avoid two slots power control delay, downlink slot format for SF 512 should be changed.

Currently, the field order for SF 512 has been proposed to be changed in CR007 of TS25.211, “Compressed mode by higher layer scheduling”. This format makes one slot power control delay possible.

The slot format for downlink in CPCH is going along with it.

But, if STTD encoding is applied in SF 512, one slot power control delay can not be achieved, because there is no processing time(512chips) between DL-TPC and UP-pilot.

Since SF 512 is a very low rate channel, some of user having power control delay with 2 slots may cause little impact on system capacity. The decrement of the capacity may be negligible.

But in case of CPCH, the data rates are different between uplink and downlink. In downlink, only DPCCH of low data rate exists for the purpose of power control. But in up-link case, most of CPCH will use high data rates, requiring high power. The power control delay in the asymmetric data service like CPCH is important because increased power control delay raises the required power, resulting in a largely reduced system capacity.

In this document it is proposed that SF 512 should be changed into SF 256 when STTD encoding is applied.

It wastes code-space in the down-link. But if CPCH is used in the uplink and transmission diversity is used in the downlink, then the limit may lie in uplink, not in downlink. Therefore, if the performance degradation due to the power control delay can be reduced(or increasing the system capacity can be obtained), the wastage of the code space by reducing the SF 512 to SF 256 is minor.

2 Text Proposal

5.3.2.3 DL-DPCCH for CPCH

The spreading factor for the UL-DPCCH (message control part) is 256. The spreading factor for the DL-DPCCH (message control part) is 256 or 512 depending on the transmit diversity. The following table 15 shows the DL-DPCCH fields (message control part) ~~which are identical to the first row of table 11 in section 5.3.2.~~

~~Table 15: DPDCH and DPCCH fields for CPCH message transmission~~

~~Slot Format #i~~	~~Channel Bit Rate (kbps)~~	~~Channel Symbol Rate (ksps)~~	~~SF~~	~~Bits/Frame~~			~~Bits/ Slot~~	~~DPDCH Bits/Slot~~		~~DPCCH Bits/Slot~~		
				~~DPDCH~~	~~DPCCH~~	~~TOT~~		~~N_{Data1}~~	~~N_{data2}~~	~~N_{TFCI}~~	~~N_{TPC}~~	~~N_{Pilot}~~
~~0~~	~~15~~	~~7.5~~	~~512~~	~~60~~	~~90~~	~~150~~	~~10~~	~~2~~	~~2~~	~~0~~	~~2~~	~~4~~

Table 15: DPDCH and DPCCH fields for CPCH message transmission

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/Frame			Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot		
				DPDCH	DPCCH	TOT		N_{Data1}	N_{data2}	N_{TPC}	N_{TFCI}	N_{Pilot}
0	15	7.5	512	60	90	150	10	0	4	2	0	4
4	30	15	256	210	90	300	20	2	12	2	0	4