TSG-RAN Working Group 1 meeting #9　　　　　　　***TSGR1#9(99)i77***
Dresden, Germany
November 30 – December 3, 1999

TSG-RAN Working Group 2 meeting #9　　　　　　　***TSGR2#9(99)h74***
Sophia Antipolis, France
November 29 – December 3, 1999

Agenda item:

Source:　　　　　Ericsson

Title:　　　　　CR 25.211-011: Sliding paging indicators

Document for:　　　Decision

1　　Introduction

The concept of "sliding" paging indicators, i.e. the fact that PIs should be transmitted in different parts of the 10 ms frame to avoid extra receiving time to sample neighbouring cells, has been accepted by both WG1 and WG2. What is missing is a concrete proposal how the sliding shall be done.

Since it was previously understood that the calculation of the PI position should take both IMSI and SFN into account, and that IMSI should not be mentioned in the L1 specifications, WG1 previously sent this issue to WG2 who responded that they will specify the sliding function.

However, after looking more into this issue, it is feasible to separate the position function into one that takes e.g. IMSI into account in the higher layer specifications, and then do the sliding in the L1 specification using only a function of SFN. This gives a very nice functionality split between the different specifications. Moreover, it was recognised that WG2 people could have difficulties to understand how a "good" sliding scheme would look like.

Hence, this contribution consist of a concrete proposal of how the PI position shall be calculated, with a CR for WG1 (25.211). The contribution is presented to both WG1 and WG2 meetings, in hope that consensus on the functionality split can be resolved even with parallel meetings.

2　　Proposal

2.1　　General

It is proposed that in the higher layer specifications, a paging indicator (PI) is computed for each UE. The calculation tries to map different users to different PIs. The PI is then mapped to actual PICH bits by a function in the L1 specification. This mapping achieves the sliding functionality, since the position is a function of SFN.

2.2　　Higher layer functionality

The paging indicator (PI) to use for a UE is computed as

　　$PI = DRX\ Index\ \bmod\ N_p$

where DRX Index = {(IMSI mod M) div (DRX Cycle Length div PBP)}, Np is the number of paging indicators per frame and PBP is the Paging Block Periodicity. PBP is only applicable for TDD, for FDD PBP = 1.

2.3   Physical layer functionality

In L1, the PI calculated by higher layers is mapped to the actual PI position PI_p (and PICH bits), where p is computed as

$$p = \left(PI + \left\lfloor \left(18 \times \left(SFN + \lfloor SFN/8 \rfloor + \lfloor SFN/64 \rfloor + \lfloor SFN/512 \rfloor \right) \right) \bmod 144 \right) \times \frac{N}{144} \right\rfloor \right) \bmod N,$$

where N is the number of paging indicators per frame. The formula introduces the function of SFN that is wanted to achieve the siding. One nice feature of the above formula is that is works well with all DRX cycles (which can be 2^k frames, $k = 0, 1, 2, \ldots, 12$).

The factor 18 determines how much the position is changed between frames in the DRX cycle. The value 18 means that the PIs for a particular UE will appear in 8 different positions within the frame, since $8 \times 18 = 144$. This is seen as a good compromise between sliding speed and sliding resolution. After 8 frames all 8 PI positions have been used, i.e all eight positions of the frame have been sampled. The addition of SFN with different dividers (corresponding to bit shifting), ensures that the formula works equally well for all DRX cycles. The factor N/144 is used to make the formula work when the number of PIs per frame is 72, 36 and 18.

Examples of how the formula works are found in the plots in Figure 1 below. What is plotted is the PI position p as a function of SFN, for different paging cycles. In the figures, it is assumed that the frame with SFN = 33 is part of the DRX cycle. Moreover, 36 PIs per frame is assumed and PI = 0.
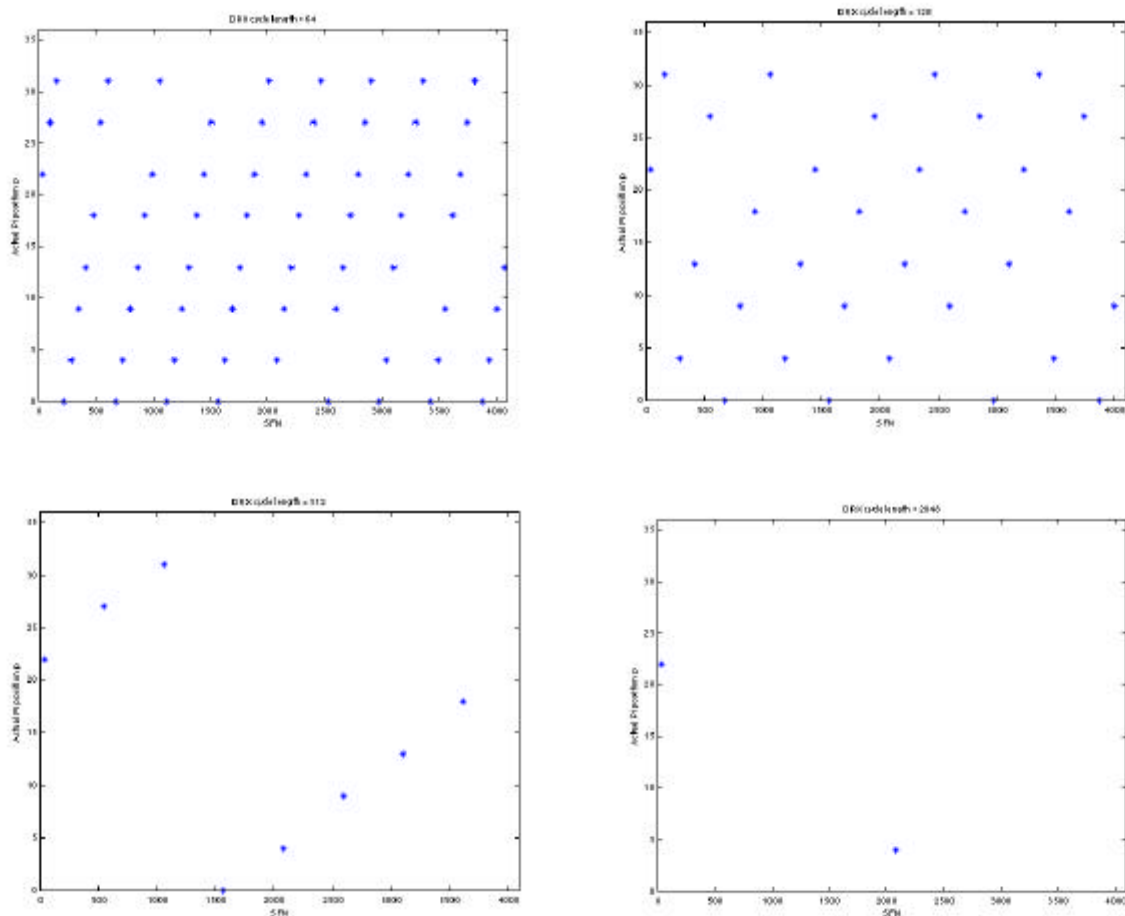

Figure 1: Examples of actual PI position as function of SFN.

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.211 CR **011**   Current Version: 3.0.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑   *↑ CR number as allocated by MCC support team*

For submission to: **TSG-RAN #6**   for approval **X**   strategic ☐   *(for SMG*
list expected approval meeting # here ↑   for information ☐   non-strategic ☐   *use only)*

Form: CR cover sheet, version 2 for 3GPP and SMG   The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

Proposed change affects: (U)SIM ☐   ME **X**   UTRAN / Radio **X**   Core Network ☐
(at least one should be marked with an X)

Source:	Ericsson	**Date:**	1999-11-22

Subject: Sliding paging indicators

Work item:

Category: F   Correction   **Release:**   Phase 2   ☐
                        A   Corresponds to a correction in an earlier release   Release 96   ☐
(only one category   B   Addition of feature   **X**   Release 97   ☐
shall be marked   C   Functional modification of feature   Release 98   ☐
with an X)   D   Editorial modification   Release 99   **X**
                                                                                                  Release 00   ☐

Reason for change: A sliding paging indicator scheme has been agreed in WG1 and WG2. This CR introduces the L1 changes need to support the scheme.

Clauses affected: 5.3.3.7

Other specs affected:
Other 3G core specifications	**X**	→ List of CRs:
Other GSM core specifications	☐	→ List of CRs:
MS test specifications	☐	→ List of CRs:
BSS test specifications	☐	→ List of CRs:
O&M specifications	☐	→ List of CRs:

Other comments:

5.3.3.7 Page Indication Channel (PICH)

The Page Indicator Channel (PICH) is a fixed rate (SF=256) physical channel used to carry the Page Indicators (PI). The PICH is always associated with an S-CCPCH to which a PCH transport channel is mapped.

Figure 22 illustrates the frame structure of the PICH. One PICH frame of length 10 ms consists 300 bits $(b_0, b_1, \ldots, b_{299})$. Of these, 288 bits $(b_0, b_1, \ldots, b_{287})$ are used to carry Page Indicators. The remaining 12 bits $(b_{288}, b_{289}, \ldots, b_{299})$ are undefined~~not used~~.
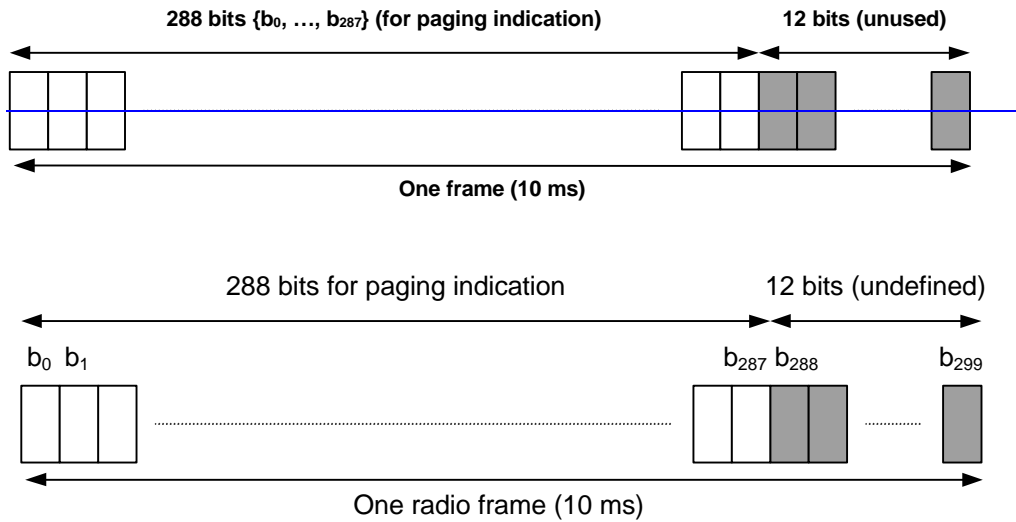

Figure 22: Structure of Page Indicator Channel (PICH)

N Page Indicators $\{PI_0, \ldots, PI_{N-1}\}$ are transmitted in each PICH frame, where N=18, 36, 72, or 144.

The PI calculated by higher layers for use for a certain UE, is mapped to the paging indicator PI_p, where p is computed as a function of the PI computed by higher layers, the SFN of the P-CCPCH radio frame during which the start of the PICH radio frame occurs, and the number of paging indicators per frame (N):

$$p = \left(PI + \left\lfloor \left(18 \times \left(SFN + \lfloor SFN/8 \rfloor + \lfloor SFN/64 \rfloor + \lfloor SFN/512 \rfloor \right) \right) \bmod 144 \right) \times \frac{N}{144} \right\rfloor \right) \bmod N .$$

The mapping from $\{PI_0, \ldots, PI_{N-1}\}$ to the PICH bits $\{b_0, \ldots, b_{287}\}$ are according to table 21.

Table 21: Mapping of Page Indicators (PI) to PICH bits

Number of PI per frame (N)	$PI_{ip} = 1$	$PI_{ip} = 0$
N=18	$\{b_{16ip}, \ldots, b_{16ip+15}\} = \{1,1,\ldots,1\}$	$\{b_{16ip}, \ldots, b_{16ip+15}\} = \{0,0,\ldots,0\}$
N=36	$\{b_{8ip}, \ldots, b_{8ip+7}\} = \{1,1,\ldots,1\}$	$\{b_{8ip}, \ldots, b_{8ip+7}\} = \{0,0,\ldots,0\}$
N=72	$\{b_{4ip}, \ldots, b_{4ip+3}\} = \{1, 1,\ldots,1\}$	$\{b_{4ip}, \ldots, b_{4ip+3}\} = \{0, 0,\ldots,0\}$
N=144	$\{b_{2ip}, b_{2ip+1}\} = \{1,1\}$	$\{b_{2ip}, b_{2ip+1}\} = \{0,0\}$

If a Paging Indicator in a certain frame is set to "1" it is an indication that UEs associated with this Page Indicator should read the corresponding frame of the associated S-CCPCH.