

TSG-RAN Working Group 1 meeting #9
Dresden, Germany
November 30 – December 3, 1999

TSGR1#9(99)i47

Agenda item:

Source: Ericsson

Title: CR 25.211-006: Change to the description of TSTD for SCH

Document for: Decision

TSTD can be applied to the SCH. How this is done is specified in section 5.3.3.4.1 in TS 25.211. However, TSTD is also described, in a very non-specification like manner in the figure in section 5.3.1.1.2. Further, the figure is not very clear and can be misleading.

This CR removes the unnessecary figure and makes editorial updates to the text in TS 25.211.

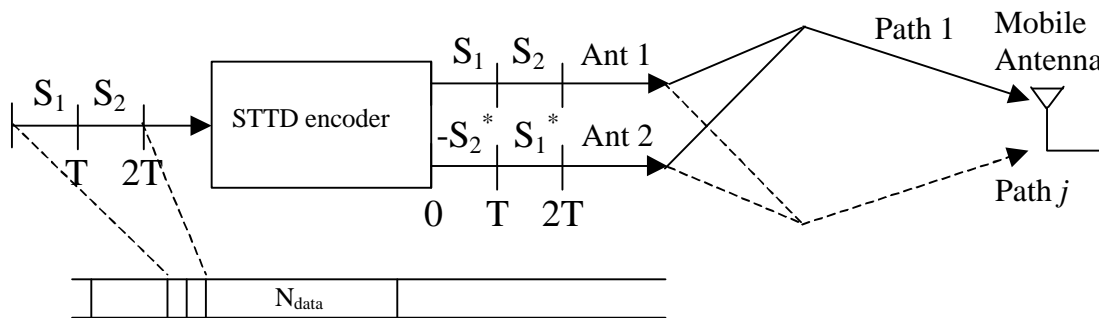


Figure 1: Block diagram of STTD encoder. The symbols S_1, S_2 are QPSK or discontinuous transmission (DTX) symbols and T denotes the symbol time.

5.3.1.1.2 Time Switched Transmit Diversity for SCH (TSTD)

[Transmit diversity, in the form of Time Switched Transmit Diversity \(TSTD\), can be applied to the SCH. TSTD for the SCH is optional in UTRAN, while TSTD support is mandatory in the UE. A block diagram of the transmitter using TSTD for SCH and STTD for P-CCPCH is shown in Figure 9. TSTD for the SCH is described in sub-clause 5.3.3.4.1.](#)

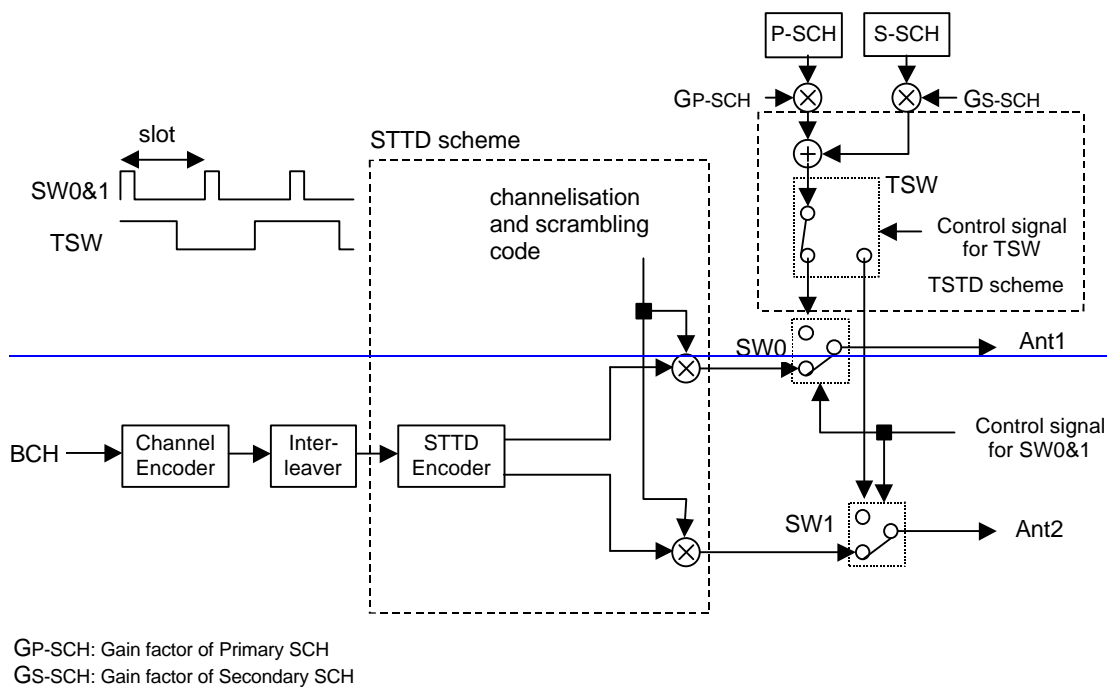


Figure 9: Multiplexing scheme of SCH (TSTD) and P-CCPCH (STTD).

5.3.2 Dedicated downlink physical channels

There is only one type of downlink dedicated physical channel, the Downlink Dedicated Physical Channel (downlink DPCH).

Within one downlink DPCH, dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH), is transmitted in time-multiplex with control information generated at Layer 1 (known pilot bits, TPC commands, and an optional TFCI). The downlink DPCH can thus be seen as a time multiplex of a downlink DPDCH and a downlink DPCCH, compare Section 5.2.1. It is the UTRAN that determines if a TFCI should be transmitted, hence making it mandatory for all UEs to support the use of TFCI in the downlink.

Error! Reference source not found. shows the frame structure of the downlink DPCH. Each frame of length 10 ms is split into 15 slots, each of length $T_{\text{slot}} = 2560$ chips, corresponding to one power-control period. A super frame corresponds to 72 consecutive frames, i.e. the super-frame length is 720 ms.