3GPP TSG-RAN WG1#7bis
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Agenda Item: 5

Source: Samsung Electronics Co.

Title: Random Gating Pattern for Uplink DPCCH Gated Transmission

1. Introduction

The gated DPCCH transmission was included as a working assumption in TS 25.214 at the TSG RAN WG1meeting #7[1]. The proposed regular gating pattern in TS 25.214 is aimed for the quality of both uplink and downlink. However, due to its periodic transmission on the uplink gated transmission, there were some concerns about undesirable EMC effects on hearing aid.

Regarding the undesirable EMC effects, Mitsubishi already submitted a proposal which uses time hopping of the period of gated transmission of uplink DPCCH which they claim has less effect on hearing aid[2].

This suggestion by Mitsubishi seems to be reasonable in some cases and can be added to the existing gating pattern. So, Samsung proposes a simple uplink random gating pattern generating method for based on SFN(System Frame Number) and real part of downlink primary scrambling code.

2. Proposed random gating pattern generation method

In order to reduce the undesirable EMC effect, we suggest randomizing the gating pattern by varying the transmission slot (for pilot and TPC) according to the combination of N chips selected from downlink primary scrambling code of the first slot of the previous gating group. The downlink primary scrambling code has period of 10ms frame length and thus it repeats for each frame. In order to avoid the periodic gating pattern with period of frame length and to make it longer up to 720ms, we introduce a chip offset from the slot boundary utilizing SFN (System Frame Number).

The detail operations are as follows.

Let x_{SFN} be the chip offset used for corresponding SFN period. The chip offset is an offset from the first slot boundary of the previous gating group as in Figure 1, and defined by

$$x_{SFN} = \text{SFN}, \qquad 0 \le \text{SFN} \le 71 \tag{1}$$

By definition given in Eq. (1), the period of gating pattern is extended to 720ms long.

Basic idea of the proposed randomization rule is modulo operation according to the gating rate. For example, in case of gating rate 300Hz, the transmission slot in current gating group *i* is decided by an operation *K(i-1) mod* 3, where *K(i-1)* is an integer value generated from the previous group. To be specific, let *K(i-1)* be the decimal value constructed by *N* chips from real part of downlink primary scrambling code with offset x_{SFN} chips from the first slot boundary of the previous gating group *i*-1, and let *S(i)* be the selected position of slot for uplink DPCCH in current gating group *i*, then the slot for uplink DPCCH allocations is decided by the following rules.

- **Gating rate 1/3**

$$S(i) = K(i-1) \bmod 3, \tag{2}$$

- **Gating rate 1/5**

$$S(i) = K(i-1) \bmod 5 \tag{3}$$

It is enough to set to 10 for *N* in order to get proper level of randomness. The estimated gate count for modulo operation with 10bit input is summarized in Table 1.

Table 1. Estimated gate count for modulo operation with 10 bit input

	Gate count	maximum estimated delay
mod 3	172	10ns
mod 5	238	10ns

Figure 1 shows the detail of the above uplink DPCCH allocation rule.

3. Conclusion

We proposed the random gating pattern generation method for uplink DPCCH gated transmission by using downlink primary scrambling code. Companies interested in the EMC issue will test the effect of the EMC by using the proposed random gating pattern.

4. Reference

[1] 3GPP RAN TS 25.214 v1.3.0(1999-09)

[2] TSGR1#8(99)f43, "Reducing EMC problem in uplink DPCCH Gated mode", Mitsubishi Electric ITE.

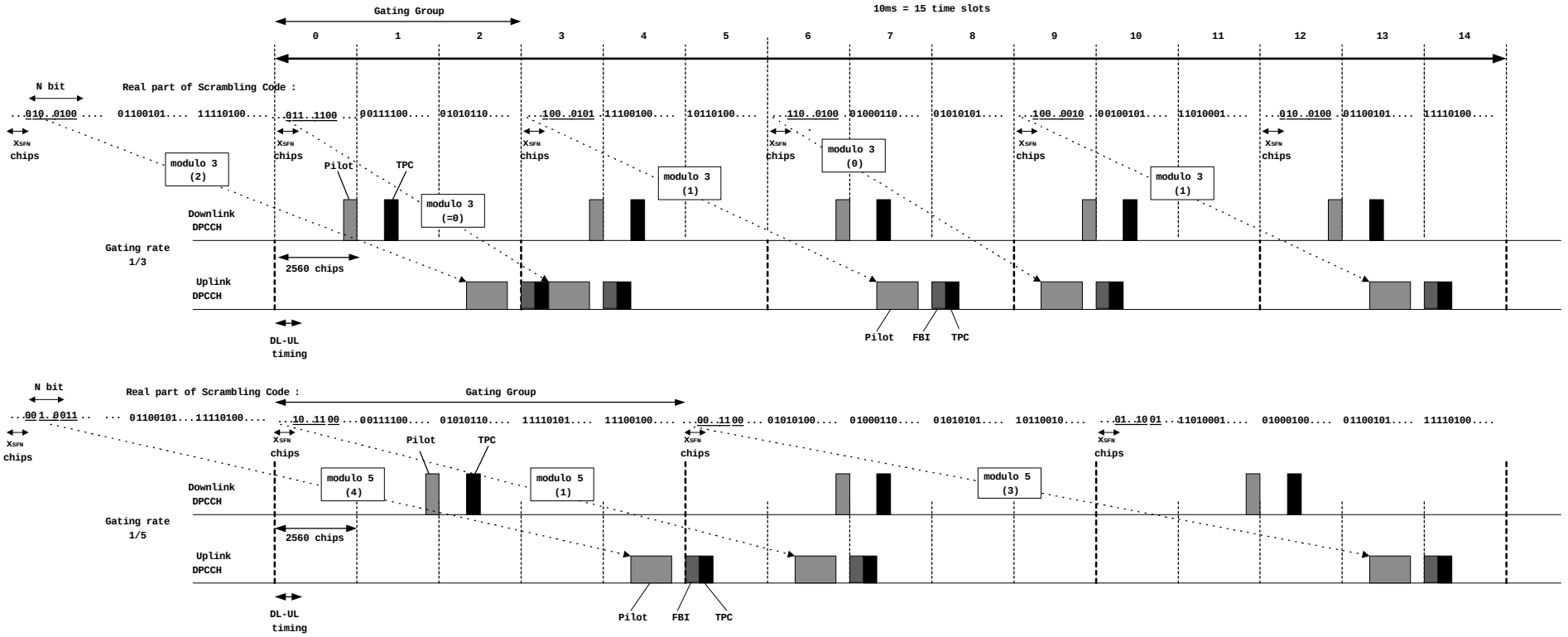

Figure 1. Description of random gating pattern generation for gating rate 1/3, 1/5