

Agenda Item:

Source: Nokia

Title: Clarifications to DSCH sections in 25.211 and 25.213

Document for: Approval

Introduction

This contributions provides clarifications to the description of the PDSCH in 25.211 and in 25.213 based on the reflector discussions prior WG1#7bis. The intention of these clarifications is to improve the text in the specifications and it is not intended to introduce any new technical items for PDSCH section.

The table has been inserted to reflect the frame bit rates with different spreading factors for PDSCH and for constant presentation though 25.211, the picture as with other common channels has been inserted on the slot and frame structure.

As there is only the case of DSCH with DPCH in release -99, only one section is used for PDSCH.

The original picture has been removed and the a picture clarifying the timing relation has been inserted to section 7 on DPCH timing. Clarification to the timing has been proposed in another contribution as well and there technical content seems to be identical and thus from this perspective section 7 can be taken from either of the documents.

The respective terminology has been updated in 25.213 also.

5.3.3.5 Physical Downlink Shared Channel

The Physical Downlink Shared Channel (PDSCH), used to carry the Downlink Shared Channel (DSCH), is shared by users based on code multiplexing. As the DSCH is always associated with a DCH, the PDSCH is always associated with a corresponding DPCH.

~~This is described respectively in Section 5.3.3.5.1.~~

~~The PDSCH does not comprise any pilot symbols, since this does not seem to be required at this stage, given information provided on the associated DPCH. This still needs to be verified.~~

~~4.1.1.1.15.3.3.5.1 DSCH associated with a DCH~~

The frame and slot structure of the PDSCH, ~~when associated with a DCH, are~~ shown on Figure 1.

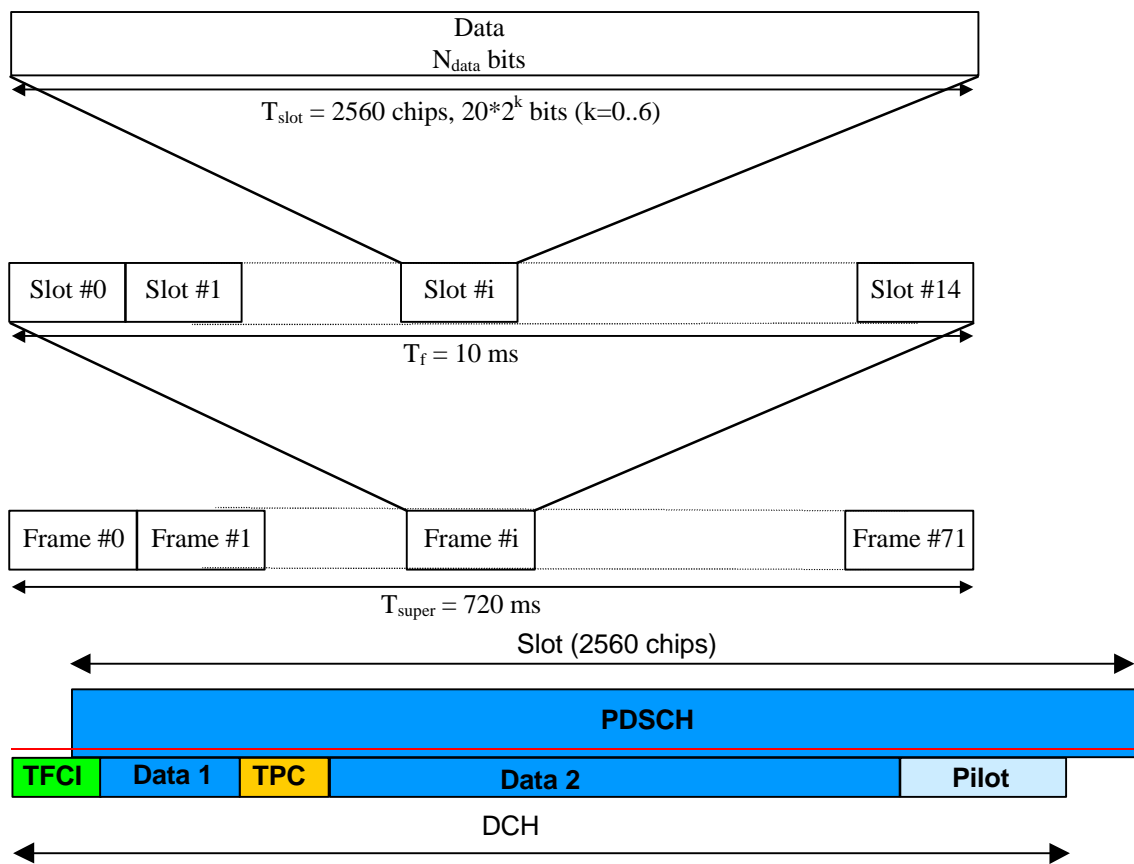


Figure 1: Frame structure for the PDSCH when associated to a DCH.

To indicate for UE that there is data to decode on the DSCH, two signalling methods are possible, either using the TFCI field, or higher layer signalling.

The PDSCH transmission with associated DPCH is a special case of multicode transmission. The channels-PDSCH and DPCH do not have necessary the same spreading factors and for PDSCH the spreading factor may vary from frame to frame. The relevant Layer 1 control information is transmitted on DCH/DPCC part of the associated DPCH, the PDSCH does not contain DPCC physical layer information. The channel bit and symbol rates for PDSCH are given in table X.

For PDSCH the allowed spreading factors may vary from 256 to 4.

If the spreading factor and other physical layer parameters can vary on a frame-by-frame basis, the TFCI shall be used to inform the UE what are the instantaneous parameters of PDSCH including the channelisation code from the PDSCH OVSF code tree.

A DSCH may consist of be mapped to multiple parallel PDSCHs codes as well, as negotiated at higher layer prior to starting data transmission. In such a case the parallel codes-PDSCHs shall be operated with frame synchronization between each other.

Table x: PDSCH fields

<u>Channel Bit Rate (kbps)</u>	<u>Channel Symbol Rate (ksps)</u>	<u>SF</u>	<u>Bits/ Frame</u>	<u>Bits/ Slot</u>	<u>N_{data}</u>
<u>30</u>	<u>15</u>	<u>256</u>	<u>300</u>	<u>20</u>	<u>20</u>
<u>60</u>	<u>30</u>	<u>128</u>	<u>600</u>	<u>40</u>	<u>40</u>
<u>120</u>	<u>60</u>	<u>64</u>	<u>1200</u>	<u>80</u>	<u>80</u>
<u>240</u>	<u>120</u>	<u>32</u>	<u>2400</u>	<u>160</u>	<u>160</u>
<u>480</u>	<u>240</u>	<u>16</u>	<u>4800</u>	<u>320</u>	<u>320</u>
<u>960</u>	<u>480</u>	<u>8</u>	<u>9600</u>	<u>640</u>	<u>640</u>
<u>1920</u>	<u>960</u>	<u>4</u>	<u>19200</u>	<u>1280</u>	<u>1280</u>

7.2 PDSCH timing

The relative timing between a PDSCH and ~~DCH~~ downlink DPCH is given as follows:

PDSCH timing is identical-time aligned to the cell primary CCPCH frame timing.

DCH timing is asynchronous~~The PDSCH frame is not frame or slot aligned with downlink DPCH frame, the PDSCH frame timing can be with~~ max 1 slot (2560 chips) ahead or max 14 slots (35840 chips) behind the associated downlink DPCH frame, with steps of 256 chips.

This determines explicitly on which frame ~~on the~~ PDSCH carries the user data based on the TFCI or higher layer signaling on downlink DPCH~~DCH~~.

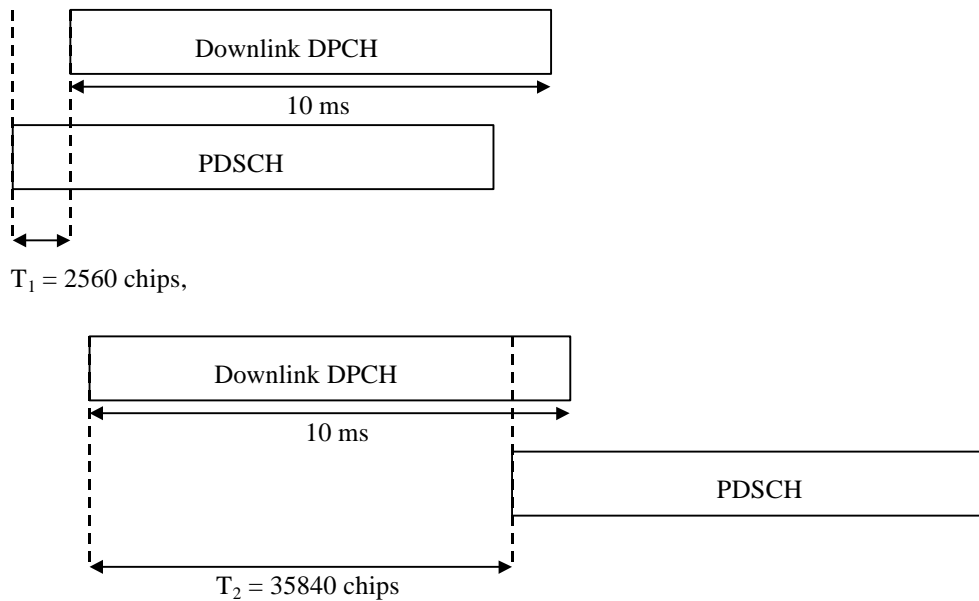


Figure x. PDSCH and downlink DPCH relative frame timing relation with maximum values of the timing offset.

25.213. section 5.2.1

In case the OVSF code on the PDSCH varies from frame to frame, the OVSF codes shall be allocated such a way that the OVSF code(s) below the smallest spreading factor will be from the branch of the code tree pointed by the smallest spreading factor used for the connection. This means that all the codes for UE for the PDSCH connection can be generated according to the OVSF code generation principle from smallest spreading factor code used by the UE on PDSCH.

In case of mapping the DSCH to multicode-multiple parallel PDSCHs-allocation, the same rule applies, but all of the branches identified by the multiple codes, corresponding to the smallest spreading factor, may be used for higher spreading factor allocation.