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Improved closed loop power control algorithm in slotted mode

Abstract

This article proposes an algorithm that improves uplink (resp. downlink) closed loop power control performances in downlink (resp. uplink) slotted mode. This algorithm consists basically in applying a larger power control step during a certain amount of time when transmission restarts, in order to recover faster a SIR close to SIR_{target}. The proposed algorithm enables to improve the performances by up to 0.8 dB compared to the standard algorithm, reducing significantly the loss caused by slotted mode.

1.Introduction

All that follows in this article is valid for both downlink and uplink slotted modes, but in order to simplify the description, only the downlink slotted mode will be considered in the following.

The slotted mode in downlink transmission has been introduced in UMTS in order to make possible for a user equipment (UE) to measure interfrequency power, to make the acquisition of control channel of other system/carrier and to perform handover. It consists basically in stopping transmission during a certain amount of time. When several slots of a frame are not used for transmission, this frame is said to be *slotted*. The number of those slots is called the *idle length*. What frames are slotted are decided by the network. Slotted frames can occur periodically or can be requested on demand ([1],[3]). Fig. 1 gives a schematic representation of slotted mode.

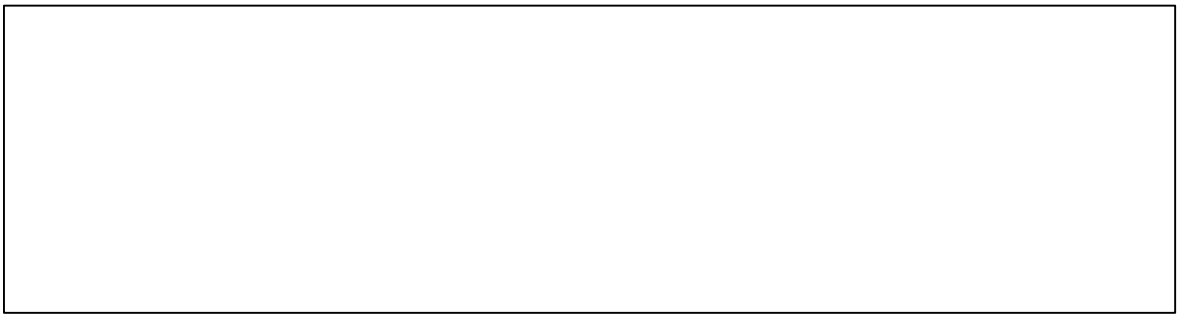

Fig. 1. Slotted mode.

One of the drawbacks of the slotted mode is that during the *idle length*, uplink closed loop power control (CLPC) is no more active. Indeed, the user equipment (UE) does not receive any TPC command in this time period. Therefore, signal to interference ratio (SIR) of the uplink signal at the base transceiver station (BTS) can deviate far from SIR_{target}, degrading performances of the uplink transmission. Fig.2 highlights this point.

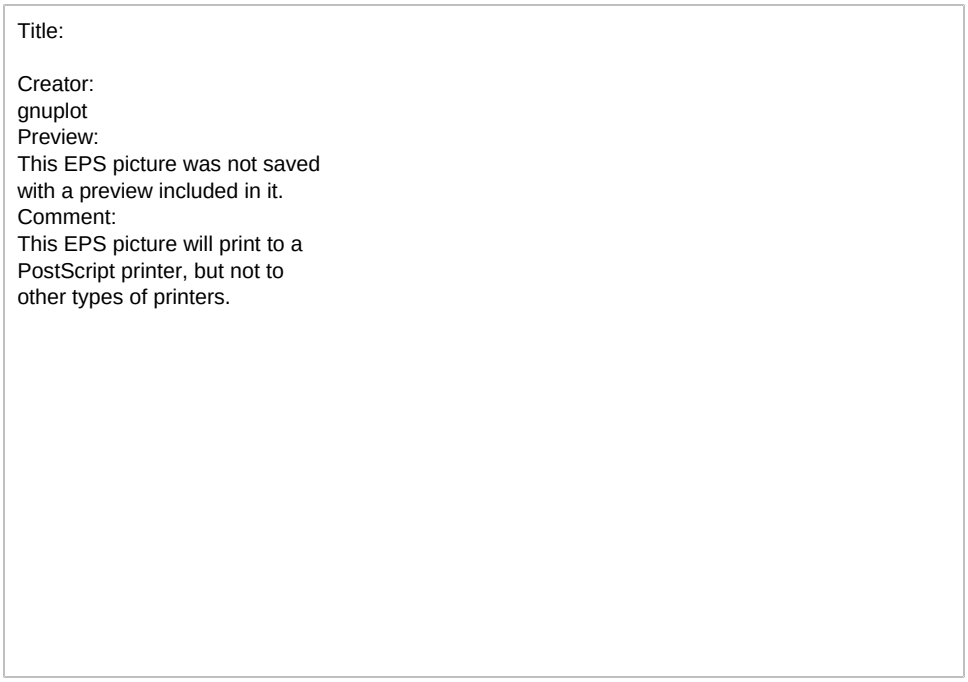

Fig.2. SIR deviation due to slotted mode (idle period from slot 600 to 608)

In the example of Fig. 2, in slotted mode, the difference between SIR and SIR_{target} is up to 6 dB, compared to only 2 dB in non-slotted mode . We can also notice that, using the power control algorithm we propose, SIR faster recovers values close to SIR_{target}.

The proposed algorithm for CLPC in slotted mode is described in part 2. In part 3 and 4, we expose our simulations parameters and results. Fifth part is the conclusion.

2. Proposed algorithm

During the idle period, uplink CLPC is no longer active. Of course, uplink CLPC restarts when downlink transmission restarts. The proposed algorithm consists in using a higher power control step during a *recovery period* after CLPC restarts (see fig.3). This method allows recovering SIR_{target} faster than if we restarted CLPC with the same power control step. On fig.3, the delay *D* between downlink and uplink idle periods, corresponds to the delay between TPC command reception at the UE and application of this TPC command on uplink by UE. The number of slots in the idle period is called the *idle length* N_{idle} and the number of slots in recovery period is called the *recovery length* N_{rec}.

The proposed algorithm is as follows:

Every time slot (TS),

1) if we are in the idle period, do not perform any power control action
2) if we are in the recovery period, perform CLPC algorithm with step $\Delta' > \Delta$
3) if we are not in one of those 2 cases, perform CLPC algorithm with step Δ

We remind that the CLPC algorithm with step Δ can be written [2]:

Every TS,

1) the BTS estimates the average received SIR during the TS
2) the BTS compares this SIR to SIR_{target}

- if SIR>SIR_{target}, the BTS sends a “down” TPC command to the UE, and UE decreases its power by Δ dB.
- if SIR<SIR_{target}, the BTS sends a “up” TPC command to the UE, and UE increases its power by Δ dB.

We can notice that the standard CLPC algorithm is a particular case of the proposed algorithm, for which recovery period is zero or, equivalently, Δ’ = Δ.

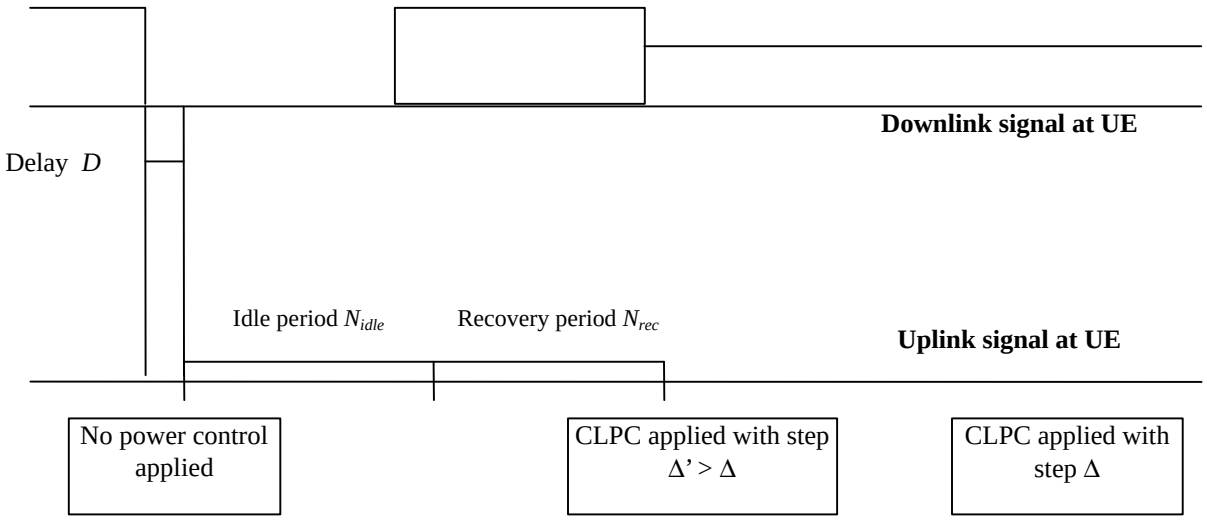

Fig.3. Proposed algorithm.

For the proposed algorithm parameters values, we recommend Δ’ = 2Δ and $N_{rec} = N_{idle}$, as they appear to be the most interesting. Nevertheless, other values are still being investigated.

3. SIR variance

In this section, we compare SIR variance of the 3 methods as a function of the UE speed, for different parameter values, in order to demonstrate that the proposed algorithm improves performances of power control in slotted mode for all speeds.

3.1. Working model

3.1.1. SIR estimation

We assume a perfect SIR estimation. Indeed, it is computed from the actual channel energy. However, in real systems, the channel energy is unknown and is estimated with help of pilot bits. Some simulation results with larger transmission error probability (TEP) of TPC commands are presented to take into account the performance degradation due to real SIR estimation.

3.1.2. Power control dynamic range

In this study, we suppose that the entity that executes power control commands can increase or decrease its power without limits. Of course, transmit power is always limited. Nevertheless, transmit power is rarely huge, i.e. only when the channel attenuation (Rayleigh fading+shadowing+path loss) is strong. Therefore, as our performance estimator is SIR variance (see section 3.1.3.), our results are

nearly not affected by this approximation. Anyway, the impact of the dynamic range on performances is very weak.

3.1.3. Performances estimator

SIR variance is our estimator of power control performances. It is evaluated in N_{mes} slots after each idle period (see fig.4), since we only want to see how different the 3 methods (non-slotted PC, std. Slotted PC and mod. Slotted PC) are. Indeed, the proposed power control algorithm in slotted mode only differs from the current algorithm in a short period after the idle period. This period is called the *measurement period*. The number of slots in this period is the *measurement length* N_{mes}.

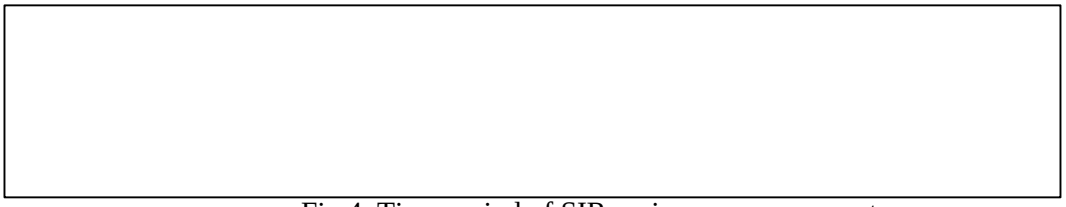

Fig.4. Time period of SIR variance measurement.

3.1.4. Simulation parameters

- *loop delay* has been set to 1 slot.
- Δ has been set to 1dB.
- Δ' has been set to 2 dB.
- In the presented simulations, the slotted mode is periodic with period *N slots*. We checked by simulation that the performance are similar with non periodic slotted mode. The simulations results are presented with N = 160 slots (10 frames). They would nearly not change for other values of N as long as $N>2N_{idle}$.
- N_{idle} has been set to 8 slots. The performance gain shown with the proposed algorithm would be larger with higher values than 8 slots.
- N_{mes} has been set to 8 slots.

3.2. Results

3.2.1.Pedestrian A, $N_{rec} = N_{idle} = 8$

The case where $N_{rec}=N_{idle}$ and Δ' is two times Δ is pretty natural. Indeed, as we stopped power control during N_{idle} slots, it seems reasonable to apply a double power control step over $N_{rec} = N_{idle}$ slots. Moreover, we set TEP = 4%, where TEP is the raw bit error rate (BER) on TPC commands. A value of 4% for TEP is an order of magnitude for speech. Results are shown in fig.5.

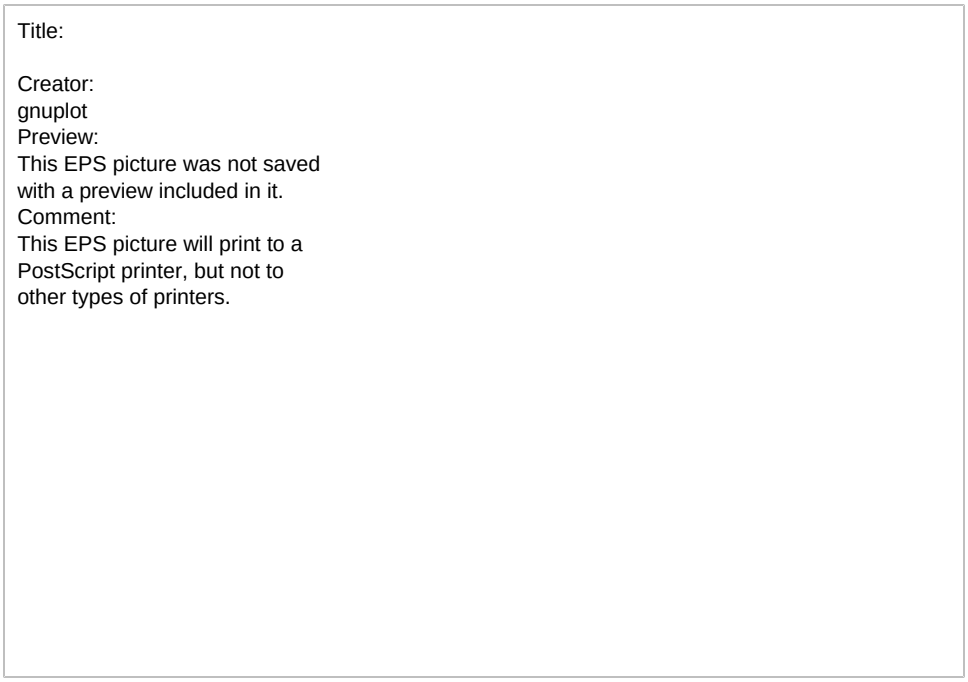

Fig.5.SIR variance of 3 methods. Pedestrian A channel. N = 160. N_{rec} = N_{idle} = 8. TEP = 4%.

We see that proposed algorithm leads to an improved SIR variance by up to 5 dB as compared to the standard algorithm. Best improvements occur for low to intermediate speeds. Indeed, at high speeds (higher than 80 km/h), power control is no more efficient and the 3 methods lead to similar performances. For large speeds, the proposed algorithm in slotted mode is even better than in non-slotted mode, since a power control step of 2 dB is better than 1 dB for these speed (in non-slotted mode, the SIR variance at 50 km/h is 14 dB with a step of 1 dB and 9 dB with a step of 2 dB).

3.2.2. Influence of recovery length: N_{rec} = 4

We show here the effect of a diminution of the recovery period. Other parameters remain unchanged. The results are shown in fig.6.

Fig.6. SIR variance of 3 methods. Pedestrian A channel. N = 160. N_{rec} = 4, N_{idle} = 8. TEP = 4%.

A recovery periods of 4 slots instead of 8 slots decreases the performances at medium and large speeds (>10 km/h). Indeed, a larger recovery period enables to better recover huge attenuation. However, the performances are slightly improved at very low speed (<10 km/h), since a power control step of 2 dB is far from the optimum step at these speeds. Therefore, it is advantageous to have a lower period where this step is applied.

3.2.3. Influence of larger error probability on TPC commands (TEP= 15%)

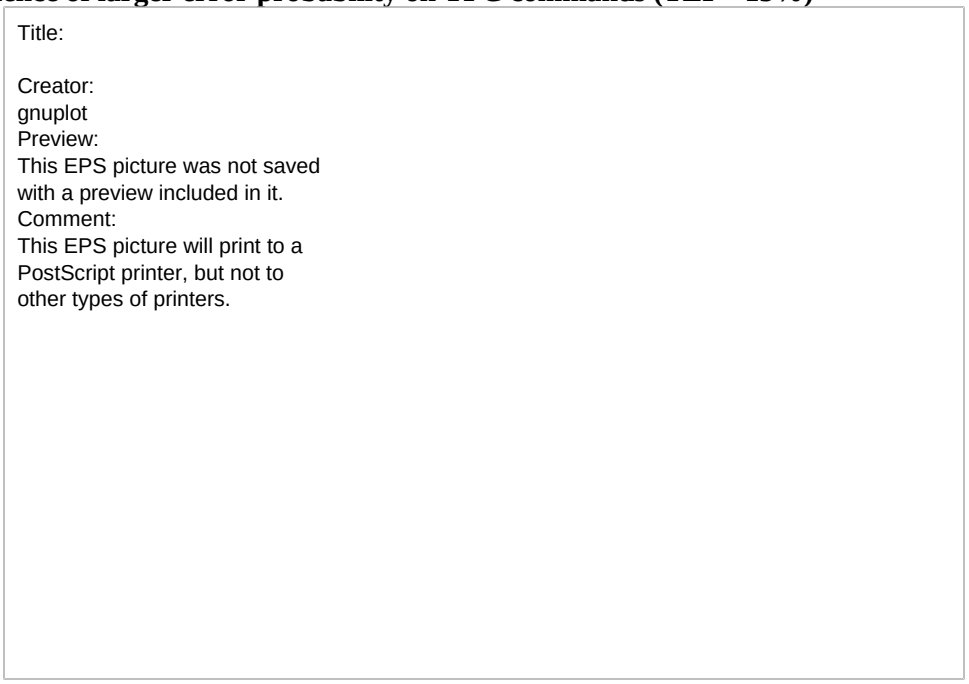

Fig.7.SIR variance of 3 methods. Pedestrian A channel. N = 160. N_{rec} = N_{idle} = 8. TEP = 15% (representation of non-ideal SIR estimation).

We see that even for the extreme case where TEP = 15%, the proposed algorithm remains very good (4 dB better than standard algorithm at intermediate speed.

3.2.4 Performances in vehicular A

Fig.8 shows that our proposed algorithm is still better than the standard one for another channel than Pedestrian A. Some other simulations have been done in other channels (pedestrian B, …) and confirm these results.

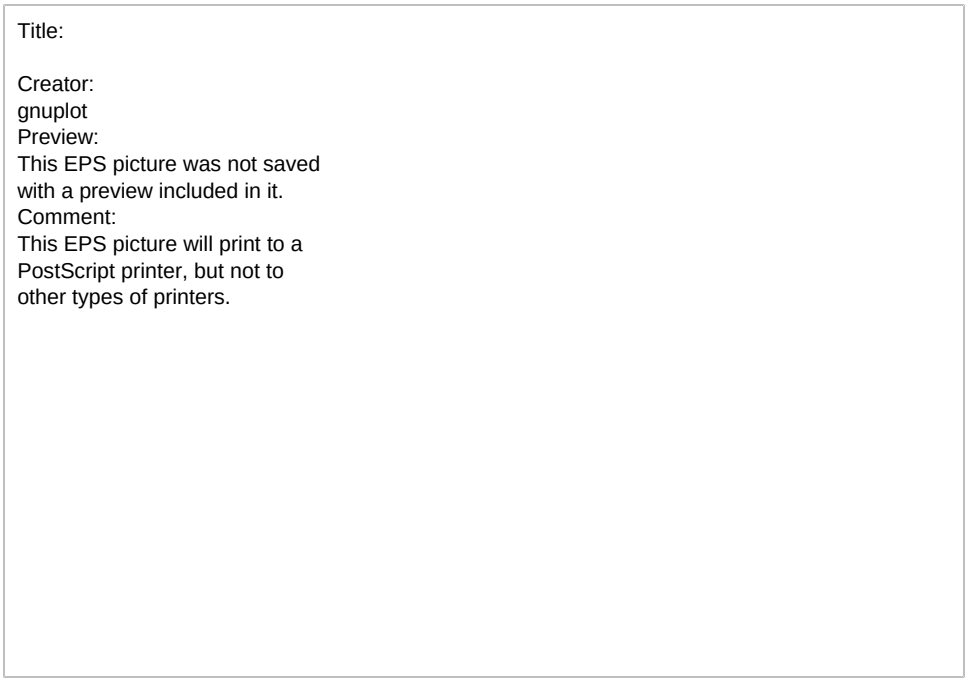

Fig.8. SIR variance of 3 methods. Vehicular A channel. N = 160. N_{rec} = N_{idle} = 8. TEP = 4%.

In this case, proposed algorithm still leads to SIR variance improvements. At 10 km/h, SIR variance for proposed algorithm is slightly larger than the standard algorithm one. This is due to the fact that at such a speed, a power control step of 1 dB is better than 2 dB. However, the proposed algorithm still enables to recover much faster the target SIR and thus does not lead to a performance degradation in term of BER for this speed also.

4. BER performances

In this section, we give some BER results, that confirm that the proposed algorithm is a real improvement.

4.1. Simulation parameters

Parameters	Values, assumptions, …
Service	**Speech**
Carrier frequency	2 GHz
Channel	Indoor to Outdoor and Pedestrian A channel where the delays of the different paths are multiple of the chip period.
Link direction	Uplink
Power control	- Fixe step of 1 dB - 1 slot delay (=0.625 ms) - Infinite dynamic range - 4% random error on TPC commands (TEP=4%) The SIR estimation is ideal (the channel energy is used).
Eb/N0 scaling	Eb is computed as the received power for each information bit including all overhead (coding, tail, pilot, TPC, TFCI, rate matching, block number, CRC)
Rake receiver	2 fingers/antenna. An ideal path searcher with fixed delays is used. The oversampling rate is the chip rate.
Channel estimation method	Channel estimation is based on the present pilot group, two previous pilot groups before and two pilot groups after the present slot (with same weight equal to 1).
Slotted mode	Period 160 slots (N), idle length 8 slots (N_{idle}) For the proposed algorithm: recovery length of 8 slots (N_{rec}) and power control step of 2 dB during the recovery length
Information bit rate	8 kbps
Physical channel rate	32 kbps (sf=128)
Number of info bits per frame	80
CRC	16 bits
Coding	Convolutional coding Constraint length 9, rate 1/3, 8 tail bits
Rate matching	Repetition: 8 bits
Interleaving	10 ms
Pilot/TPC/TFCI bits per slot	6/2/2
Number of reception antennas	1
DPCCH/DPDCH power	-3 dB
Inter-users interference	Modeled as AWGN noise. It is assumed constant and known in the simulations.

Tab.1. Simulation parameters.

4.2. Results

4.2.1. UE speed = 3 km/h

Fig 9. shows that at very low speed (3 km/h), the performances are not much degraded by the power control interruption of the uplink signal during downlink slotted mode. Thus, the performances of the proposed algorithm and the performances of the standard algorithm are similar.

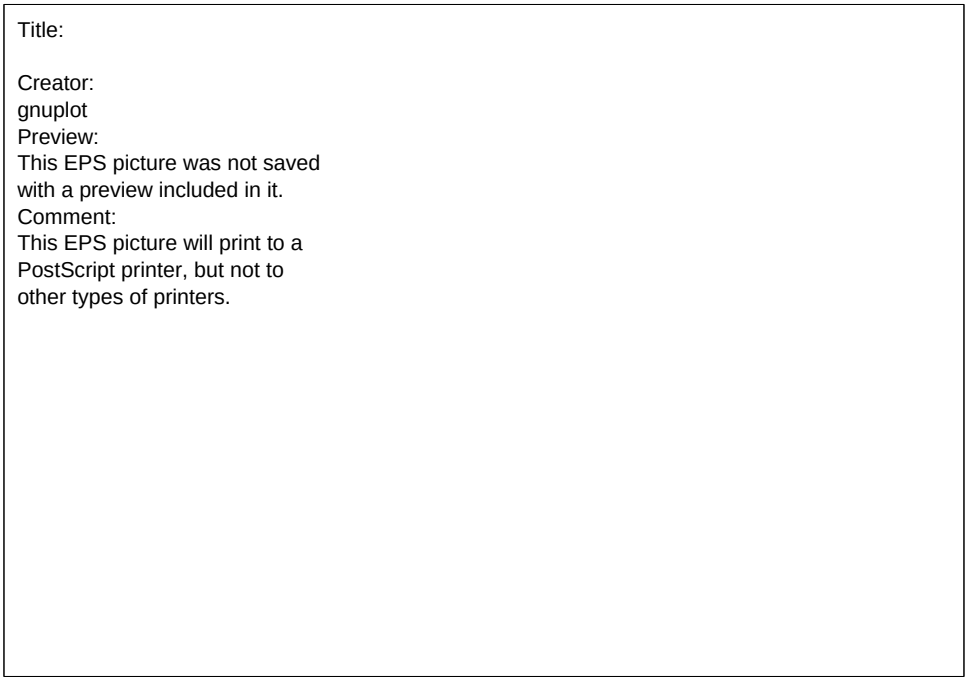

Fig.9. BER for the 3 methods. UE speed = 3 km/h.
Pedestrian A channel. N = 160. $N_{rec} = N_{idle}$ = 8. TEP = 4%.

4.2.2. UE speed = 20 km/h

Fig 10 shows that at 20 km/h, the performances in slotted mode are around 1 dB lower than in non-slotted mode for a BER of 10^{-3}. The proposed algorithm enables to reduce significantly this loss to only 0.2 dB instead of 1 dB. Thus, the gain of the proposed algorithm over the standard one is **0.8 dB**.

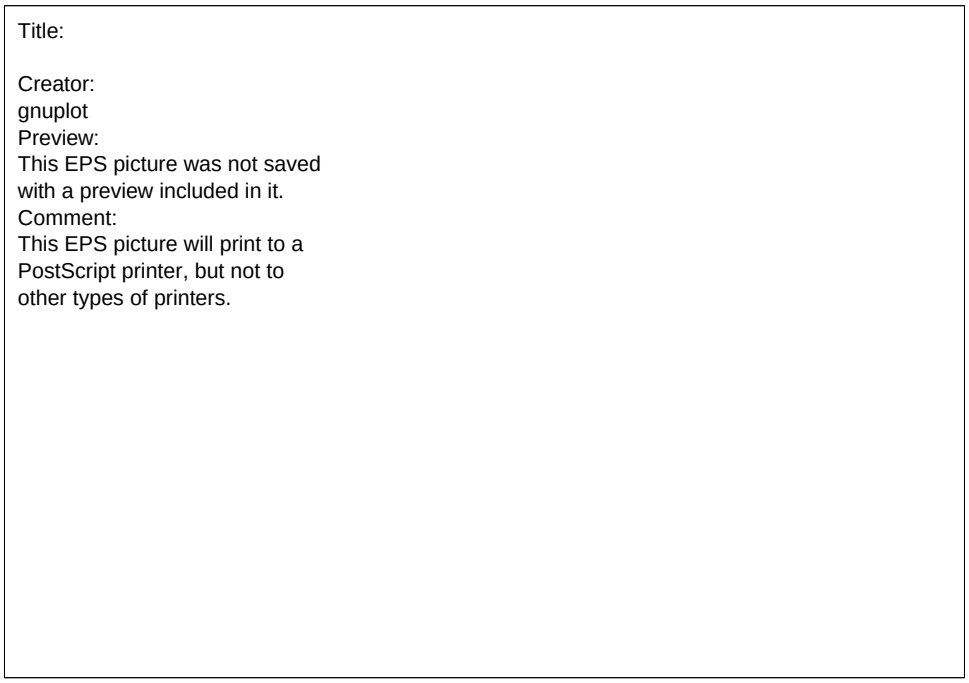

Fig.10. BER for the 3 methods. UE speed = 20 km/h.
Pedestrian A channel. N = 160. $N_{rec} = N_{idle}$ = 8. TEP = 4%.

5.Conclusion

This study shows that the proposed algorithm leads to significant improvements of the closed loop power control efficiency in slotted mode (up to 0.8 dB). The principle of this algorithm is very simple. It consists in increasing uplink power control step for a certain amount of time when downlink transmission restarts. It has the double advantage to lead to a significant improvement and to be very simple (no impact on the signaling nor on the computational complexity). Moreover, the current power control scheme can be seen as a particular case of the proposed algorithm.

References

[1] **TS S1.12** V1.1.0, 3GPP/TSG/RAN/WG1, Multiplexing and channel coding (FDD) (1999-03)

[2] **TS S1.14** V1.0.1, 3GPP/TSG/RAN/WG1, Physical Layer procedures (FDD) (1999-03)

[3] **TS S1.31** V0.0.2, 3GPP/TSG/RAN/WG1, Measurements (1999-03)