TSG-RAN Working Group 1 (Radio) meeting #3 ***TSGR1#3(99)158***
NYNÄSHAMN, Sweden 22-26, March 1999

Agenda Item: **6**

Source: **Ad Hoc #7**[*]

Title: **Report from Ad Hoc #7: Slot Structure**

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1 Summary of discussed issues

At the 2nd WG1 meeting, the following issues are identified as FFS items in Ad Hoc #7 [1]:

1. Modification and extension of the field sets for downlink DPCH and uplink DPCCH;
2. SF 128 for uplink DPCCH;
3. Bit allocation in Secondary CCPCH for SFs other than 64;
4. The pilot patterns not defined in ARIB, i.e., pilot patterns for different field lengths from ARIB;
5. Bit allocation for chip rates other than 4.096 Mcps.

Ad Hoc #7 discussed these issues except Item 5. Item 5 seems impossible to solve by April. The summary of the discussions is described below.

Ad Hoc #7 also made a liaison statement to WG2 [2] as concerns transport channel properties which includes two issues: 1) the necessity of the downlink DPCH with SF 512, and 2) the necessity of TFCI for Secondary CCPCH. The liaison statement was sent under the name of Ad Hoc #7 to the 2nd WG2 meeting on March 11, but it was not presented in the meeting unfortunately.

2 Current status of discussed items

2.1 TPC field expansion in downlink DPCCH

CSELT proposed expanding the TPC field. Since the proposal is quite recent, we have not reached an agreement yet.

Details: ---

CSELT distributed their simulation results [4] in which some BER performances are shown in changing both the number and the power of TPC bits. They propose increasing the number or the power of TPC bits in case of low spreading factors (<= 16). The proposed bit assignments are Pilot / TPC / TFCI = 16 / 8 / 8 (with TFCI) and 24 / 8 / 0 (without TFCI).

The Ad Hoc chairman recommended that the Data1 field should be punctured if the TPC field would be expanded.

2.2 Downlink DPCH field formats for SF 512

The Ad Hoc chairman proposed changing the field order only for SF 512, from TFCI / Data1 / TPC / Data2 / Pilot to TFC / TFCI / Data2 / Pilot. Texas Instruments expressed their concern about impacts on UE design. There is no other argument. This issue also relates to LS-to-WG2. This proposal would not be adopted in the April specification.

Pros of the new field order “TFC / TFCI / Data2 / Pilot”:

- Because the end of the TPC field becomes the same as those in the other SFs, UE can control the transmit power of uplink DPCH at each slot head.
- Since SF 512 is a very low rate channel, we may not need TFCI. No bits are assigned to the Data1 field. Then, the field order looks the same as those in the other SFs.

2.3 Uplink DPCCH field formats

There is no proposal using SF 128.

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For SF 256, there are some comments. These are classified into two questions:

a) Can we puncture the Pilot field down to 5 bits ?
b) Do we need 2 bits for the FBI field ?

Ad Hoc #7 has reached an agreement that we may puncture the Pilot field down to five bits instead of puncturing the TPC field. As concerns the second question, Ad Hoc #7 would like to await the Ad Hoc #6 decision whether two bits are needed for the FBI field or not. Therefore, the former four formats in the following table are agreed, and the latter two formats are FFS. The Ad Hoc chairman proposed the field order should be Pilot / TFCI / FBI / TPC.

Table 1 in S1.11: DPCCH fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{pilot}	N_{TPC}	N_{TFCI}	N_{FBI}
16	16	256	160	10	6	2	2	0
16	16	256	160	10	8	2	0	0
16	16	256	160	10	5	2	2	1
16	16	256	160	10	7	2	0	1
16	16	256	160	10	[6]	[2]	[0]	[2]
16	16	256	160	10	[5]	[1]	[2]	[2]

Details: ---

CSELT distributed their simulation results [3] in which one-bit puncturing of the Pilot bits in uplink DPCCH, i.e., from 6 bits to 5 bits, causes degradation of about 0.1 – 0.2 dB for the system working point of 0.1 % BER. They also pointed out [4] that TPC bit puncturing is a problem with low data rate services, e.g., speech.

Alcatel presented their simulation results in which the degradation is 0.5 dB. They estimated the loss would be 1 dB when considering the performance degradation of pass searchers. However, Nokia expressed their estimation, and supported the CSELT's results.

As concerns 2-bit FBI field, Motorola supported the idea. They raised three reasons;

1. further improvement in downlink performance using FB mode Tx diversity (higher update rates),
2. possibility to combine SSTD and FB mode Tx diversity to improve performance during SHO,
3. possibility to extend FB mode Tx diversity to the case of more than two antennas.

They will present their results in Ad Hoc #6. (Very recently, they pointed out that Eb/No of TPC information is going to be higher even with 1-bit TPC in LCD and UDD services.)

Nokia expressed their worry about 2-bit FBI that there is not any such a big need and 2-bit FBI will also increase the complexity. They suggested that this issue is left FFS and only if later a clear benefit is seen, then we can think whether we want to adopt it.

2.4 Uplink DPDCH gain factors

CSELT proposed the following set, but Ericsson expressed their concern. This issue needs further investigations.

Proposed gain factors (DPCCH/DPDCH) in dB:
infinite (no DPDCH transmitted), 0, -1.5, -3, -4.5, -6, -7.5, -10.

To Ad Hoc #3:
The gain factors whatever is the final conclusion on the precise values will be applied to PRACH message part.

Ericsson's concern:
One should look at the implementation when defining these ratios. The multiplier at baseband does not work in steps of 1.5 dB in power. Since the multiplier works at chip rate, doing 4 Mcps with 4-bit resolution or 12-bit resolution makes a big difference.
It is currently assumed that when the rate and rate matching changes, the power should change as well. It is not clear with what resolution such a power change due to rate change should be done. It may be difficult to adjust the power in too small steps, since that would require multiplications with many bits.

2.5 Secondary CCPCH formats for SFs other than 64

The Ad Hoc chairman proposed Secondary CCPCH formats, but there is no argument. This issue relates to the LS-to-WG2, whether TFCI is necessary or not. We should await the WG2 decision.

Proposed format sets by the Ad Hoc chairman:

We can apply similar formats to those in downlink DPCH, excluding TPC field. The field order is Data/(TFCI)/Pilot, and the pilot patterns can be the same as those in downlink DPCH.

Table 2 in S1.11: Secondary CCPCH fields

Without TFCI

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}	N_{pilot}
32	16	256	320	20	12	8
64	32	128	640	40	32	8
128	64	64	1280	80	72	8
256	128	32	2560	160	152	8
512	256	16	5120	320	304	16
1024	512	8	10240	640	624	16
2048	1024	4	20480	1280	1256	16

With TFCI

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}	N_{pilot}	N_{TFCI}
32	16	256	320	20	10	2	2
64	32	128	640	40	30	2	2
128	64	64	1280	80	64	2	8
256	128	32	2560	160	144	2	8
512	256	16	5120	320	296	16	8
1024	512	8	10240	640	616	16	8
2048	1024	4	20480	1280	1256	16	8

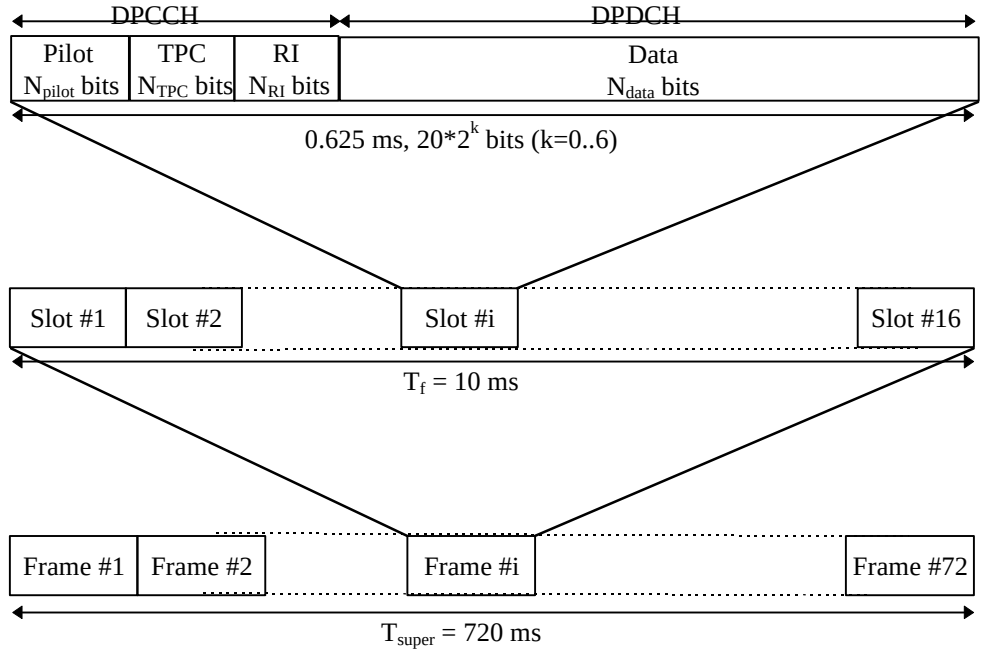

Figure 1 in S1.11: Frame structure for Secondary Common Control Physical Channel (with TFCI).

Reference

[1] Ad Hoc #7: "Report from Ad Hoc #7: Slot structure", TSGR1#2(99)059 rev.

[2] Ad Hoc #7: “Liaison statement to WG2 on transport channel properties”, TSGR1#3(99)144.
[3] CSELT: “Impact of the number of pilot bits on the uplink performance”, TSGR1#3(99)170.
[4] CSELT: “BER on power control bits”, TSGR1#3(99)171.