RAN WG1 #2 **TSGW1#2(99)106**

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Title : Discussion on channel interleaver for 3GPP selection

Source : Nortel Networks [1]

## 1. Introduction

In order to progress on the channel interleaver subject, and as this issue has not been discussed in details in ETSI, this document tries to list first some requirements for channel interleaver selection in 3GPP, then different combinations for first and second interleavers with pros and cons, and proposes two interleaver solutions that would provide good performance, flexibility and low implementation complexity.

## 2. Requirements for channel interleaver

### 2.1. Compatibility of second interleaver with multiplexing step :

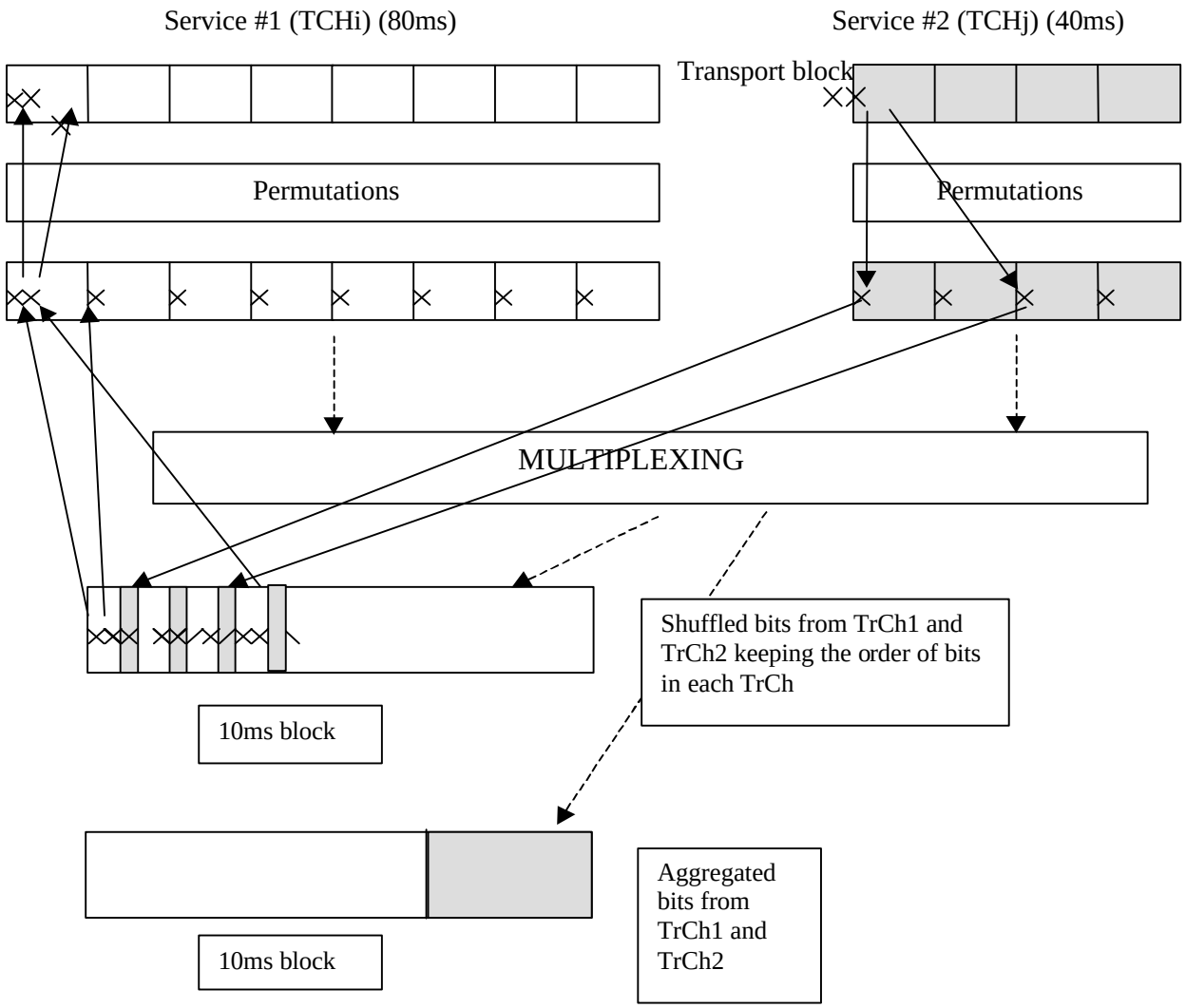
In the current channel coding and multiplexing scheme, which is advised by ad-hoc 4 to be selected in the merging process for 3GPP, the channel interleaver consists in two parts. The first interleaver applies to each Transport Channel independently, and is an inter-frame interleaver. The second interleaver applies to bits of several Transport Channels once they have been multiplexed in a block corresponding to one frame, it is intra frame interleaving. Thus the second interleaver is performed on a block made of bits from different TrChs for example 10bits from TrCh1, 5 bits from TrCh2, and 5 bits from TrCh3. This leads to some requirements in terms of compatibility between the way Transport Channels are multiplexed and the second interleaver design. There is also a risk that the second interleaver spoils the effect of the first interleaver. For example if some bits of a TrCh were initially next to each other in the TrCh, and are well spread by the 1st Interleaver, they should not be put back next to each other by the second interleaver.

Since the second interleaver applies to a mixture of bits from several TrCh, some care should be taken to find a criteria to ensure that it improves performance for each TrCh once all TrChs are mixed together.

In the same idea, if rate matching occurs between the two interleavers steps, as is proposed for uplink by ad hoc 4, this might need to be considered when designing the second interleaver.

The following figure details the two interleaver steps, along with two multiplexing schemes.

[1] Contact Person : Catherine Gauthier, Nortel
1 Place des Freres Montgolfier, 78042 Guyancourt, France
Tel : +33 1 39 44 57 47, Fax : +33 1 39 44 50 12, e-mail : gauth@nortel.com




2.2. Low Complexity :

Since the channel interleaver is made of two parts, and each part will probably have to be defined for several sizes, this might result in a high number of interleaver designs. Thus some care should be taken regarding the interleavers complexity. For example, storage of index tables for all different sizes should be avoided if possible and replaced by some more condensed means.

## 3. Review of different first and second interleavers combinations

In this paragraph, some possibilities for first and second interleaver design are listed and the pros and cons are identified.

### 3.1. Both first and second interleaver mixing bits

*Description* :

The first interleaver spreads the bits on several transport blocks of each Transport Channel independently.

Then the multiplexing step mixes bits from several TrChs. This can be done two ways. First way : the bits from different TrChs are aggregated, i.e. in each 10ms block, bits from the first TrCh are taken, then bits from the second TrCh, then from third, etc.. . Second way : the bits are uniformly shuffled as described in Todc 706, i.e. the bits of the second TrCh are dispatched between those of the first TrCh, then the bits of the third TrCh are dispatched between the previous bits, etc…This is shown in the following figure.

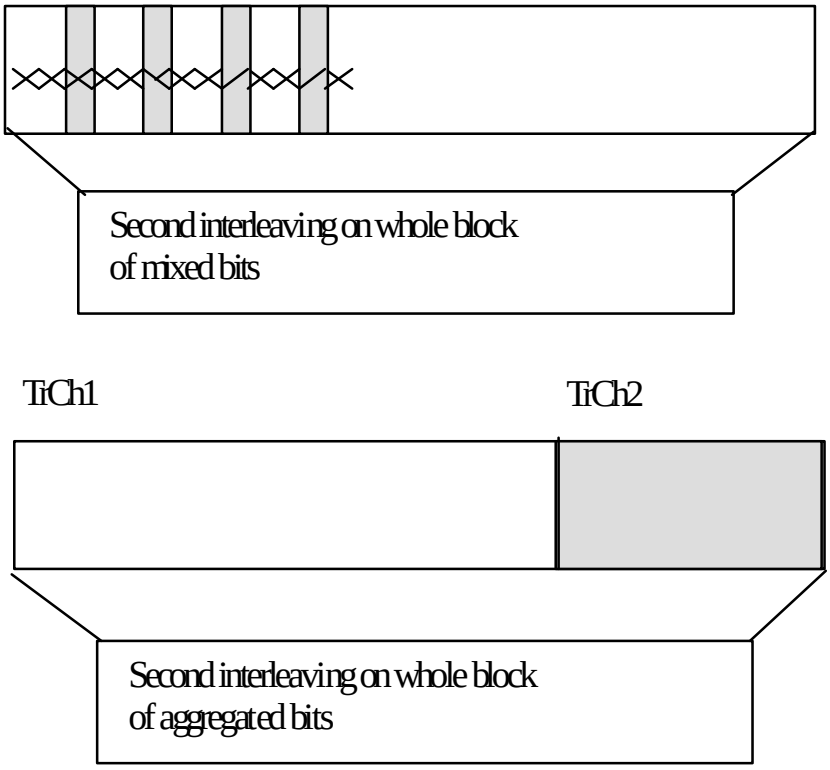
Then the second interleaver is applied to the mixture of bits in each 10ms block.

*Pros and cons :*

If the second interleaver applies to the whole 10ms block of mixed bits, then which criterion could ensure that the effects of all different first interleavers is not destroyed, and how can the second interleaver be optimized for all TrCHs together?

This optimization should probably take into account the way bits are multiplexed since the final objective is that bits of one TrCh which were consecutive initially (i.e. before first interleaver and multiplexing) are well spread in the 10ms burst. This does probably not only consist of spreading apart bits that are consecutive before second interleaving, but some distinction should be done on to which TrCh the bits belong.

Possibly the global effect could be optimized for each TrCh but it does not seem obvious thus it should be well demonstrated before acceptance of such a scheme.




### 3.2. First interleaver complex and second interleaver straight forward

*Description* :

As described in ETSI/UMTS/L1 Tdoc 706, the first interleaver is optimized for spreading the bits of one TrCh, the multiplexing step and intra frame interleaving steps can be very simple with just uniform shuffling of the bits of different TrChs together, which does not change the order of the bits of one TrCh.

*Pros and cons :*

This has the following advantages. It provides a good first interleaver which can be optimized for the known possible blocks sizes of one TrCh. It has a simple multiplexing and intraframe interleaving step. The second step does not destroy the effect of first interleaver since the order of bits in each TrCh is not changed. It even still improves it, since some bits of each TrCH are spread further when bits of other TrChs are put inbetween.

However some improvement might be brought by more sophisticated second interleaving, if joint optimization for all TrChs is feasible.

### 3.3. First interleaver simple and second interleaver optimized

*Description* :
The first interleaver would just mix transport blocks of one TrCH without changing the order of the bits inside the transport blocks. The second interleaver would take bits from several TrCh and be a standard interleaver acting as if it was applied to bits of one same TrChs.
*Pros and cons :*
This has the advantage of being very simple as well, and define only few interleaver sizes. Since the second interleaver applies to a 10ms full block, the different possible sizes are in fact as numerous as the possible spreading factors.
However the performance might not be as good : even if the bits are well spread considered as a whole, there might be a risk that sometimes two bits of a TrCh get next to each other since this has not been taken into account in the interleaver design.

## 4. Nortel proposals

### *First proposal :*

Nortel's first proposals consists of having an optimised first interleaver, which can be described by using only a few parameters for each possible interleaving size instead of storing the whole table of interleavers index, and having a very simple multiplexing and second interleaving scheme as described in Tdoc 706.

$$r(k) = (a_i^1 * k + b_i^1) \bmod N1, \quad k = 0,1,2,..N1-1$$
$$c(k) = (a_i^2 * k + b_i^2) \bmod N2, \quad k = 0,1,2,..N2-1$$

The exact parameters and block sizes to be defined depend on the different channel rates and possibly the rate matching if this step occurs before first interleaving, as it is foreseen in ad hoc 4 for downlink. Thus exact definition of these parameters will occur after a solution has been adopted regarding the whole scheme.

### *Second proposal :*

Nortel's second proposal would be to have a simple first interleaver that would cope with any sizes, like for example bit reversal block interleaver, and have a second interleaver with good performance and at the same time low complexity where rows and columns permutations would be defined by a congruent system.

$$r(k) = (a_i^1 * k + b_i^1) \bmod N1, \quad k = 0,1,2,..N1-1$$
$$c(k) = (a_i^2 * k + b_i^2) \bmod N2, \quad k = 0,1,2,..N2-1$$

Parameters table for different 10ms bit numbers

| Physical channel | Symbol rate [ksps] | The number of bits in a frame [bits] | N1 | N2 | Alpha 1 Beta 1 | Alpha 2 Beta 2 |
|---|---|---|---|---|---|---|
| Downlink DPCH | 8 | 64 | 32 | 2 | | |
| | 16 | 160 | 32 | 5 | | |
| | 32 | 480 | 32 | 15 | | |
| | 64 | 1120 | 32 | 35 | | |
| | 128 | 2400 | 32 | 75 | | |
| | 256 | 4832 | 32 | 151 | | |
| | 512 | 9952 | 32 | 311 | | |
| | 1024 | 20192 | 32 | 631 | | |
| | 2048 | 40416 | 32 | 1263 | | |
| | 4096 | 81376 | 32 | 2543 | | |
| Uplink DPCH | 16 | 160 | 32 | 5 | | |
| | 32 | 320 | 32 | 10 | | |
| | 64 | 640 | 32 | 20 | | |
| | 128 | 1280 | 32 | 40 | | |
| | 256 | 2560 | 32 | 80 | | |
| | 512 | 5120 | 32 | 160 | | |
| | 1024 | 10240 | 32 | 320 | | |
| | 2048 | 20480 | 32 | 640 | | |
| | 4096 | 40960 | 32 | 1280 | | |

However this scheme would have to be refined to ensure good performance for each TrCh, optimised jointly with the first interleaver.

## 5. Conclusion

This document listed some requirements foreseen for channel interleaver design, and some possibilities in term of first and second interleaver combination. It then proposed two interleaver schemes with good performance and low complexity, which should be refined once some assumptions are made on rate matching and multiplexing steps.

WG1 is invited to give some feedback on these thoughts, in order to prepare selection of the channel interleaver for 3GPP.