TSG-RAN meeting #25 RP-040273
Palm Springs, USA, 7-9 September 2004

Status Report for SI to TSG

Study Item Name: Feasibility Study for the analysis of higher chip rates for UTRA TDD evolution

SOURCE: Rapporteur (Martin Beale, IPWireless) **TSG:** RAN **WG:** 1

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Ref. to SI sheet: RAN_Study_Items.doc

Progress Report since the last TSG (for all involved WGs):

RAN1#38: Three documents were presented in RAN1 covering system level simulation results for voice bearers, application to 3GPP systems and services and the conclusions section of the TR. The conclusion of the study item is provided in Appendix A for information.

There was a good deal of discussion on the conclusions section of the TR. RAN1 were unable to agree on a recommendation for further work. RAN1 were also not able to agree on a section of the proposed conclusion summarising work carried out in RAN4 as RAN1 considered that this section of the conclusion should have been approved by RAN4. The section of the proposed conclusion relating to RAN4 work is included in Appendix B.

List of Completed elements (for complex work items):

- Higher chip rate reference configuration.
- Simulation assumptions
- Link level simulation results for Release 5 type bearers
- System level simulation results for Release 5 type bearers
- Link level results for Release 99 type bearers
- Release 99-type system level simulations
- Backwards compatibility and mobility sections of feasibility study
- Complexity analysis
- Coexistence of higher chip rate TDD with HCR-TDD, LCR-TDD and FDD
- Feasibility analysis
- Conclusion

List of open issues:

none

Estimates of the level of completion (when possible):

100%

SI completion date review resulting from the discussion at the working group:

RAN#25 (Sept 2004)

References to WG's internal documentation and/or TRs:

RP-040361 “TR25.895 v2.0.0 : Analysis of higher chip rates for UTRA TDD evolution”

Appendix A: Conclusions of TR25.895 [1]

In the study "Analysis of higher chip rates for UTRA TDD Evolution", use of higher chip rates for TDD have been studied. The chip rate of 7.68Mcps has been studied in detail. The study considered a reference configuration at 7.68Mcps showing minimal changes from the 3.84Mcps UTRA TDD specifications. The following aspects of this system were considered:

- *system and link level performance*
- *complexity*
- *link budget, coexistence and backwards compatibility*
- *mobility*
- *impact on working groups, specifications and signalling*
- *aspects related to 3GPP systems and services, antenna systems and higher chip rates than 7.68Mcps*

Some specific aspects of antenna systems were not studied.

Simulation results presented in RAN1 have shown a significant performance improvement of the order of 30-40% for packet services when a chip rate of 7.68Mcps is adopted. The packet call rate increases by approximately 30-40% and packet delay decreases by approximately 30-40% at the higher chip rate. Alternatively, approximately 30-40% more users can be supported at the same packet call rate. These gains are witnessed over a range of channel models and for different traffic types (HTTP and FTP traffic types were studied, TCP was modelled). These gains are due to statistical multiplexing gains at 7.68Mcps (reduced blocking probability), the ability of the packet scheduler to allocate more resource to UEs at the higher chip rate and due to link level gains.

Simulation results for 12.2kbps DCH channels carrying voice traffic show an increase in capacity of the order of 10-15% across a range of channel types. The increased capacity at the higher chip rate is due to trunking efficiency gains (according to the Erlang-B model) and due to link level gains at the higher chip rate.

The gains stated above are the gains for a 7.68Mcps system over two independent 3.84Mcps system occupying the same bandwidth. Other methods of using the 10MHz bandwidth may be feasible, but are out of the scope of this study and have not been studied.

Link results have shown link level performance gains of 0-2dB at 7.68Mcps. These link level gains are particularly evident in channel PA3 and for high coding rates and modulations in other dispersive channels. The link level gains are due to the superior ability of the higher chip rate to resolve multipath components. These link level gains lead to cell throughput gains of the order of 5-10% for packet services in dispersive channels.

The complexity of a 7.68Mcps UE is approximately 33% greater than that of a 3.84Mcps UE for the same UE capability. Dual mode 3.84Mcps / 7.68Mcps TDD UEs are feasible. Node B baseband processing complexity is approximately 30% greater than at 3.84Mcps, though other aspects of Node B complexity are similar at 3.84Mcps and 7.68Mcps. Node B and RNC throughput, buffering and interfaces need to be dimensioned to support a greater cell throughput and more active users at 7.68Mcps.

The feasibility study shows that 7.68Mcps TDD can be designed to be backwards compatible with other UTRA modes (when a 7.68Mcps TDD UE also implements at least one of the other UTRA modes). Mobility of a UE between a 7.68Mcps UTRAN and UTRANs for other UTRA modes has been shown to be feasible.

Introduction of a higher TDD chip rate will have impacts on RAN working groups and specifications. The working groups that are principally affected are RAN1 and RAN4. By and large, it is only the TDD aspects of these working groups that are affected. The specifications controlled by these working groups are impacted in a substantive way. Specifications controlled by RAN2, RAN3 and T1 are impacted to a lesser extent. Some signalling impacts have been identified in the study (related to signalling of parameters of the 7.68Mcps TDD system – number of channelisation codes, timing advance quantization etc.).

Appendix B: proposed RAN4 related conclusion not included in TR25.895

Studies in RAN4 have shown that 7.68Mcps systems can coexist with 3.84Mcps TDD and 1.28Mcps TDD systems. The studies showed that the co-existence between TDD and FDD downlink is not affected by modulation bandwidth specific issues, hence already known TDD / FDD coexistence results will apply both to 3.84Mcps and 7.68Mcps TDD. The capacity reduction in the FDD uplink has been shown to be less that 1% due to an adjacent 7.68Mcps TDD system. RAN4 studies have shown that the link budget at 7.68Mcps is similar to the 3.84Mcps TDD link budget.