TSG-RAN meeting #21 RP-030400
FRANKFURT, Germany, 16-19 September 2003

Status Report for SI to TSG

Study Item Name: Feasibility Study for the analysis of higher chip rates for UTRA TDD evolution

SOURCE: Rapporteur (Martin Beale, IPWireless) **TSG:** RAN **WG:** 1

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Ref. to SI sheet: RAN_Study_Items.doc

Progress Report since the last TSG (for all involved WGs):

- RAN1#33: Five documents were presented covering the following aspects :
  - Downlink link level results for Release 99 channels
  - System level simulation results for HSDPA channels
  - Schedulers used in system level results
  - Interpretation of system level results

  A text proposal (Tdoc R1-030887) on the system level simulation results was presented, this proposal is currently being reviewed by RAN1, so far no fundamental concerns have been stated on the presented results.

- RAN4#28: no contributions

List of Completed elements (for complex work items):

- Higher chip rate reference configuration.
- Simulation assumptions
- Link level simulation results for Release 5 type bearers
- Downlink link level results for Release 99 type bearers
- Backwards compatibility and mobility sections of feasibility study

List of open issues:

- Uplink link level performance for Release 99 type bearers
- Complexity analysis.
- Feasibility analysis.
- System level simulation results (system simulation results for Release 5 type bearers have been presented in RAN1#33 and are under review in RAN1).

Estimates of the level of completion (when possible):

50%

SI completion date review resulting from the discussion at the working group:

RAN#22 (Dec 2003)

References to WG's internal documentation and/or TRs:

R1-030926 "TR25.895 v1.2.0 : Analysis of higher chip rates for UTRA TDD evolution"