3GPP TSG RAN **Tdoc RAN 705/99**
13 - 15 December 1999
Nice, France

Source : RAN WG1 Chairman

Object: Time-plan for RAN WG1 in 2000

The following time-plan is submitted for approval in RAN plenary.

The work in year 2000 will be prioritised according to the following:
- Completion of outstanding items for release 99
- Corrections and clarifications of release 99 specifications
- Specification of release 00 features

For the work in year 2000, but still part of release-99, the following items are identified. (With the common deadline for 3/2000 (Subject to TSG RAN approval for inclusions in release –99)
- TDD cell parameter cycling
- Out of synchronisation refinements
- Small turbo coding block sizes (Turbo interleaver below 320 bits)
- Compressed mode with puncturing
- CPCH issues
- DPCCH gating

These items are proposed by WG1 to be presented for RAN#7 for approval.

The following features are scheduled for release 00:
- Hybrid ARQ
- FAUSCH
- TDD 1.28 Mchips/s
- TX diversity refinements

The following milestones are proposed the the release 2000 items:

RAN#8: Reporting the conclusions of Hybrid ARQ studies

RAN#9: CRs for 25.2-series finalised on:
- Hybrid ARQ
- FAUSCH
- TDD 1.28 Mchips/s
- TX diversity refinements

Note: There exists additional smaller items that may be studied for release 2000 and whether they result to any changes for specifications is to be seen. Conclusions should be reached by RAN#9 in any case and reported to TSG RAN. Such items include for example Paging channel configuration change indicator for FDD or Joint Predistortion for TDD. This workplan in not intended to prevent proposing any new items but for such items the milestone having conclusions by RAN#9 shall apply.

RAN#10: Remaining corrections/clarifications for Release 2000 items.