**3GPP TSG-RAN4 Meeting # 111 *R4-2408256***

**Fukuoka City, Fukuoka , Japan, 20th – 24th May, 2024**

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| *CR-Form-v12.3* |
| **CHANGE REQUEST** |
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|  | **38.133** | **CR** |  | **rev** |  | **Current version:** | **18.5.0** |  |
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| *For* [***HE******LP***](http://www.3gpp.org/3G_Specs/CRs.htm#_blank)*on using this form: comprehensive instructions can be found at* [*http://www.3gpp.org/Change-Requests*](http://www.3gpp.org/Change-Requests)*.* |
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| ***Proposed change affects:*** | UICC apps |  | ME | **x** | Radio Access Network |  | Core Network |  |

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| ***Title:***  | [NR\_FR2\_multiRX\_DL-Core] Draft CR for dual TCI state switching of R18 Multi-Rx |
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| ***Source to WG:*** | ZTE Corporation, Sanechips, Nokia, BeammWave |
| ***Source to TSG:*** | R4 |
|  |  |
| ***Work item code:*** | NR\_FR2\_multiRX\_DL-Core |  | ***Date:*** | 2024-05-10 |
|  |  |  |  |  |
| ***Category:*** | F |  | ***Release:*** | R18 |
|  | *Use one of the following categories:****F*** *(correction)****A*** *(mirror corresponding to a change in an earlier release)****B*** *(addition of feature),* ***C*** *(functional modification of feature)****D*** *(editorial modification)*Detailed explanations of the above categories canbe found in 3GPP [TR 21.900](http://www.3gpp.org/ftp/Specs/html-info/21900.htm). | *Use one of the following releases:Rel-8 (Release 8)Rel-9 (Release 9)Rel-10 (Release 10)Rel-11 (Release 11)…Rel-17 (Release 17)Rel-18 (Release 18)Rel-19 (Release 19) Rel-20 (Release 20)* |
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| ***Reason for change:*** | In 110 meeting, one R15 CR R4-2403412 was approved to revise the wording in MAC-CE based TCI state switching delay. Some of revision is not captured in dual TCI state switching of multi-Rx, we add such revision. |
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| ***Summary of change:*** | Add the revision approved for R15 MAC-CE based TCI state switching. |
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| ***Consequences if not approved:*** | Not accurate enough |
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| ***Clauses affected:*** | 8.10E.3.1, 8.10E.3.2, 8.10E.4.1, 8.10E.6 |
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|  | **Y** | **N** |  |  |
| ***Other specs*** |  | **X** |  Other core specifications  | TS/TR ... CR ...  |
| ***affected:*** | **X** |  |  Test specifications | TS 38.533 |
| ***(show related CRs)*** |  | **X** |  O&M Specifications | TS/TR ... CR ...  |
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| ***Other comments:*** | The first three changes in this draft CR is based on the draft big CR R4-2406506 endorsed in 110bis meeting.The last change is based on TS38.133 v18.5.0. |
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| ***This CR's revision history:*** |  |

# <Start of Change #1>

### 8.10E.3 MAC-CE based dual DL TCI state switch delay

#### 8.10E.3.1 MAC-CE based dual DL TCI state switching delay for sDCI

The requirement in this clause applies when UE is provided with *twoQCLTypeDforPDCCHRepetition.*

When a MAC CE command for indication of UE-specific PDCCH TCI state as defined in clause 6.1.3.15 of TS 38.321 [7] indicating TCI state switch with CORESET index p are received in slot n, and if the TCI state is known, UE shall be able to receive PDCCH with the target TCI state at the first slot that is after slot n+ THARQ + $3N\_{slot}^{subframe,µ}$+ TOk\*( Tfirst-SSBp, + TSSB-proc) / *NR slot length*. The UE shall be able to receive PDCCH with the old TCI states until slot n+ THARQ + $3N\_{slot}^{subframe,µ}$ .

Where:

- THARQ is the timing between DL data transmission and acknowledgement as specified in TS 38.213 [3].

- Tfirst-SSBp is time to first SSB transmission (associated with TCI state of CORESET p) after MAC CE command is decoded by the UE; The SSB shall be the QCL-TypeA or QCL-TypeC to target TCI state.

- TSSB-proc = 2 ms.

- TOk = 1 if target TCI state is not in the active TCI state list for PDSCH, 0 otherwise.

When UE receives TCI state switch command for CORESET index pwhile UE is performing TCI state switch of CORESET index q*,* UE shall be ready to receive PDCCH with the target TCI states of CORESET index p and q after completing both the TCI state switch of CORESET p and q.

# <End of Change #1>

# <Start of Change #2>

#### 8.10E.3.2 MAC-CE based dual DL TCI state switching delay for mDCI

The requirement in this clause applies when UE is capable of *multiDCI-MultiTRP-r16* and configured with two *CORESETPoolIndex*es.

When a MAC CE command for indication of UE-specific PDCCH TCI state as defined in clause 6.1.3.15 of TS 38.321 [7] indicating a TCI state switch for *CORESETPoolIndex p* is received at slot n, and if the TCI state is known, UE shall be able to receive PDCCH with the target TCI state at the first slot that is after slot n+ THARQ + $3N\_{slot}^{subframe,µ}$+ TOk\*( Tfirst-SSBp, + TSSB-proc) / *NR slot length*. The UE shall be able to receive PDCCH with the old TCI states until slot n+ THARQ + $3N\_{slot}^{subframe,µ}$.

Where:

- THARQ is the timing between DL data transmission and acknowledgement as specified in TS 38.213 [3].

- Tfirst-SSBp is time to first SSB transmission (i.e., SSB associated to *CORESETPoolIndex p*) after MAC CE command is decoded by the UE; The SSB shall be the QCL-TypeA or QCL-TypeC to target TCI state.

- TSSB-proc = 2 ms.

- TOk = 1 if target TCI state is not in the active TCI state list for PDSCH, 0 otherwise.

When UE receives TCI state switch command for *CORESETPoolIndex p* while UE is performing TCI state switch of *CORESETPoolIndex* q*,* UE shall be ready to receive PDCCH with the target new TCI states of *CORESETPoolIndex* p and q after completing both the TCI state switch of *CORESETPoolIndex* p and q.

**--- Unchanged text in this clause is omitted ---**

# <End of Change #2>

# <Start of Change #3>

### 8.10E.4 DCI based dual DL TCI state switch delay for sDCI and mDCI

#### 8.10E.4.1 DCI based dual DL TCI state switching delay for sDCI

For sDCI, if the dual target TCI states are known, when a UE is configured with the higher layer parameter *tci-PresentInDCI* from one TRPwhich is set as 'enabled'for the CORESET scheduling two PDSCHs at slot n, UE shall be able to receive PDSCHs with target TCI states of the serving cell on which TCI state switch occurs at the first slot that is after slot n+*timeDurationForQCL*, where, *timeDurationForQCL* is the time required by the UE to perform PDCCH reception and apply spatial QCL information received in DCI for PDSCHs processing as described in TS 38.214 [26], the value of *timeDurationForQCL* is defined in TS 38.331 [2].

For sDCI, If TCI state switching is from dual TCI states to single TCI state and the target TCI state is one of the source TCI states, there is no TCI state switching delay allowed, provided that UE is configured with group-based RSRP report (*groupBasedBeamReporting-r17*).

The known condition for dual target TCI states defined in clause 8.10E.2 is applied.

# <End of Change #3>

# <Start of Change #4>

### 8.10E.6 Active DL TCI state list update delay

For sDCI, if the dual target TCI states are known, upon receiving PDSCH carrying MAC-CE for activation/deactivation of UE-specific PDSCH TCI state as defined in clause 6.1.3.14 of TS 38.321 [7] from a TRP at slot n, UE shall be ready to receive PDCCH to schedule PDSCHs from both TRPs with the new target TCI states at the first slot that is after n+ THARQ +$3N\_{slot}^{subframe,µ}$ +TOk\*(max (Tfirst-SSB1, Tfirst-SSB2)+ TSSB-proc) / *NR slot length*. Where THARQ, Tfirst-SSB1, Tfirst-SSB2, TSSB-proc and TOk are defined in clause 8.10E.3.

For mDCI case, if the target TCI state is known, upon receiving PDSCH carrying MAC-CE for activation/deactivation of UE-specific PDSCH TCI state as defined in clause 6.1.3.14 of TS 38.321 [7] from a TRP at slot n, UE shall be ready to receive PDCCH to schedule PDSCH from the TRP with the new target TCI state at the first slot that is after n+ THARQ +$3N\_{slot}^{subframe,µ}$ +TOk\*(Tfirst-SSB + TSSB-proc) / *NR slot length*. Where THARQ, Tfirst-SSB, TSSB-proc and TOk are defined in clause 8.10.3. Dual target TCI states can be used in the same slot for PDCCH or PDSCH only after both TCI states on TCI state list(s) are activated.

# <End of Change #4>