**3GPP TSG-RAN WG2 Meeting #114 electronic  *R2-210xxxx***

**19th May – 27th May 2021**

**Agenda item: 9.1.4**

**Source: ZTE (email discussion rapporteur)**

**Title: Report of [AT114-e][302][NBIOT/eMTC R17] NB-IoT/eMTC Other (ZTE)**

**Document for: Discussion and Decision**

# Introduction

This document contains the summary of the offline email discussion “*[AT114-e][302][NBIOT/eMTC R17] NB-IoT/eMTC Other”*, as indicated below:

* *[AT114-e][302][NBIOT/eMTC R17] NB-IoT/eMTC Other (ZTE)*

*Scope: Discussion of open points in agenda item 9.1.4.*

*Intended outcome: Report in R2-2106603*

*Deadline: Monday May 24 1200 UTC*

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# Offline email discussion

## 16-QAM for NB-IoT

In RAN2#113bis-e meeting, for supporting 16-QAM in NB-IoT, the following agreements are achieved:

|  |
| --- |
| RAN2#113bis-e agreements:   * *Working assumption: For the UE supporting 16-QAM, the L2 buffer size is 12000 bytes.* * *Working assumption: Support of 16-QAM has separate UE capabilities for DL and UL* |

In RAN2#114e meeting, 16-QAM related issues are further discussed in contribution [2][5][6].

**#Issue 1: UE capability**

Based on the following RAN1# 103-e agreement:

|  |
| --- |
| RAN1# 103-e agreement:  *For 16-QAM in NB-IoT, separate optional UE capabilities for UL and DL are supported:*   * *The support of 16QAM in DL is indicated by an optional UE capability signaling.* * *The support of 16QAM in UL is indicated by an optional UE capability signaling.* |

In [5], it is proposed to confirm the RAN2 working assumption in last meeting about separate UE capabilities. Based on that, the following proposal is suggested:

**Draft Proposal 1: Confirm the working assumption: The support of 16-QAM uses separate UE capabilities for DL and UL.**

DP1 is identified as an easy proposal for agreement. Companies are invited to provide your feedback on DP1.

|  |  |  |
| --- | --- | --- |
| **Company** | **Support DP1**  **(yes/no)** | **Additional comment(s)** |
| ZTE | Yes |  |
| Qualcomm | Yes |  |
| Huawei, Hisilicon | yes |  |
| MediaTek | yes |  |
| Nokia | Yes |  |
| Sequans | Yes |  |

**Conclusion:**

**Proposal:**

**#Issue 2: 16QAM configuration**

Based on the following RAN1# 103-e agreement:

|  |
| --- |
| RAN1# 103-e agreement:  *For 16-QAM in NB-IoT, separate UE-specific RRC signaling for UL and DL are supported:*   * *16QAM for UL is configured by UE-specific RRC signaling.* * *16QAM for DL is configured by UE-specific RRC signaling.* |

In [5], it is proposed to introduce separate UE-specific RRC signaling for configuration of 16QAM for DL and 16QAM for UL. And in both [2] and [5], similar TPs are provided for this part. Based on that, the following proposal is suggested:

**Draft Proposal 2: Introduce the support of 16-QAM using separate UE dedicated RRC signaling for DL and UL into *NPDSCH-ConfigDedicated-NB* and *NPUSCH-ConfigDedicated-NB* included in *physicalConfigDedicated-NB* separately.**

DP2 is identified as an easy proposal for agreement. Companies are invited to provide your feedback on DP2.

|  |  |  |
| --- | --- | --- |
| **Company** | **Support DP2**  **(yes/no)** | **Additional comment(s)** |
| ZTE | Yes |  |
| Qualcomm | Yes |  |
| Huawei, HiSilicon | maybe | As discussed last meeting, we don’t need to refer to ASN.1 details. Also this should not be about support but configuration.  **P2: 16QAM is configured via dedicated signaling** **separately for UL and DL** |
| MediaTek | yes |  |
| Nokia |  | Agree with Huawei. Separate parameter for configuration is only needed. |
| Sequans | Yes |  |

**Conclusion:**

**Proposal:**

**#Issue 3: L2 buffer size**

In RAN2#113bis-e meeting, two different L2 buffer size calculation, e.g., 12000 bytes and 16000 bytes were proposed. As a bit more companies agree on 12000 bytes, RAN2 has made a working assumption that for the UE supporting 16-QAM, the L2 buffer size is 12000 bytes. However, in this meeting, in [6], company give another calculation for total L2 buffer size for Cat NB2 supporting 16 QAM, e.g., 15008 bytes and the approximate value of 16000 bytes is proposed. The three calculation ways are summarized in the following table:

|  |  |  |
| --- | --- | --- |
| Alts | Tdoc | Details |
| Alt1 | [R2-2103488](https://www.3gpp.org/ftp/tsg_ran/WG2_RL2/TSGR2_113bis-e/Docs/R2-2103488.zip)  (R2#113bis, HW) | In Rel-14, compared to Cat. NB1, the maximum TBS of Cat. NB2 is 2.536 times for UL and 3.73 times for DL as large as the maximum TBS of Cat. NB1. But the L2 buffer size is only doubled. For Rel-17 16-QAM, since only the DL TBS is doubled compared to Cat. NB2, following the same principle as we did for Cat. NB2 (keep the L2 buffer size as low as possible to avoid big impact on the memory of the UE), we think the L2 buffer size should not be larger than 8000 bytes \* 1.5 = 12000 bytes. |
| Alt2 | R2-2103365  (R2#113bis, ZTE) | As explained in last meeting, TBS/soft channel bits in UL (2536bits) and DL (12800bits) can be considered for L2 buffer size calculation, e.g., :  Total L2 buffer size for Cat NB2 = (12800+2536) \* 8 (considering re-transmission) / 8(for bits->bytes) = 15336 ≈16000 bytes |
| Alt3 | R2-2106158  (R2#114, Ericsson) | Have similar view as that comment in previous meeting that calculation for NB-IoT is related to traffic model. As typical data sizes were assumed to be between 20 and 200 bytes for NB-IoT, if same layer 2 buffer size is defined as for Cat 0 or Cat M1, L2 buffer size would be over-dimensioned for NB-IoT.  Moreover, total layer 2 buffer size is generally defined as the sum of the number of bytes that the UE is capable of storing in the RLC transmission windows and RLC reception and reordering windows for all radio bearers. In NB-IOT considering that the number of HARQ processes is limited not too many RLC PDUs are received in parallel and thus the UE can send the RLC status PDU rather quickly when reception failure of RLC data PDU is detected. Although the actual number of RLC PDUs depends on the scheduling and delay, it is unlikely that the number of RLC PDUs in the buffer comes up to 75.  Therefore:  *Total L2 buffer size for Cat NB2 = maximum downlink data rate \* # of RLC PDUs*  *+ maximum uplink data rate \* # of RLC PDUs*  where # of RLC PDUs is 16, we have the following total L2 buffer size for Cat NB2 supporting 16 QAM:  *Total L2 buffer size for Cat NB2 = ((4968) \* 16 + 2536 \* 16) / 8 = 15008 bytes => ~16 000bytes* |

As there is new calculation, the following proposal is suggested:

**Draft Proposal 3: RAN2 discuss whether the working assumption that the L2 buffer size is 12000 bytes for the UE supporting 16-QAM can be confirmed.**

Companies are invited to provide your preference on the calculation alternatives above. If it’s Alt1, that means company agree to confirm the working assumption. Otherwise, that means company suggests to revise the working assumption.

|  |  |  |
| --- | --- | --- |
| **Company** | **Preferred Alternatives** | **Additional comment(s)** |
| ZTE | Alt3 | For Alt1, we think to use rough times may be not suitable as the absolute TBS/soft channel bits are increased much more.  For Alt2, it seems not suitable to use soft channel bits for DL while to use TBS for UL. Therefore, we think Alt3 is correct and ok with Alt3. |
| Qualcomm | Alt3 | L2 buffer size listed in 3GPP specs are just a guide. |
| Huawei | Alt1 | For Alt1: In Rel-13, we decided the L2 buffer size based on the traffic model, i.e, one PDCP PDU in UL followed by a PDCP PDU in DL. Considering the PDCP PDU is 1600 bytes, in UL, this was more or less mapping to 16 RLC PDUs of 1000 bits.  During the discussion in rel-14, it was highlighted that higher data rate or TBS did not change the traffic model and in theory there was no need to increase the L2 buffer size. However, it was also felt that it would be beneficial to increase to some extent to allow new application but the cost of memory should also be considered. We agreed on an intermediate value of 8000 bytes.  For Rel-16, we think the same approach should be followed, i.e. increase the L2 buffer size to allow new application without compromising the cost of the device. We think 12 000 bytes is a reasonable value.  For alt 3: It is clear that applying the formula to Rel-14 will not have led to 8000 bytes.  Also, if we were applying the formula just to calculate the increase compared to rel-14, this would give *4,864bytes ~5 Kbytes* which is a lot lower that the proposed additional 8 Kbytes.  we do not agree with Qualcomm that the L2 buffer size listed in 3GPP specs are just a guide. they are minimum requirement. |
| MediaTek | Alt3 | The calculation in Alt3 seems more legitimate. |
| Nokia | Alt2 | Use of TBS sizes of 16QAM seems to be right calculation. However both Alt2/Alt3 leads to approximately same number as minimum requirements. So we are OK to consider 16000 as L2 buffer size for 16 QAM. |
| Sequans | Alt1 preferrable  Alt 3 acceptable | We agree with HW’s comments that it’s not strictly necessary to go up to 16,000 but are OK to compromise with majority |

**Conclusion:**

**Proposal:**

**#Issue 4: Channel quality report for 16QAM**

According to WID, 16QAM channel quality reporting would be supported. As mentioned in [2], the channel quality report for 16QAM is based on NPDSCH transport block that achieves an error probability not exceeding 10% BLER, which is similar as that for CQI-NPDCCH report but not exactly same. Channel quality reporting for 16QAM may need finer granularity.

However, 16QAM related channel quality reporting in Msg3 may have many impacts on RAN2 specification. So company proposes in [2] that 16QAM related channel quality reporting in Msg3 is not supported. In [5], it mentions RAN2 should wait for RAN1 and/or RAN4 agreements to decide if channel quality report in RRC\_IDLE mode will be supported.

Based on above, the following proposal is suggested:

**Draft Proposal 4a: From RAN2 perspective, 16QAM related channel quality reporting in Msg3 is not supported.**

Companies are invited to provide your feedback on DP4a.

|  |  |  |
| --- | --- | --- |
| **Company** | **Support DP4a (yes/no)** | **Additional comment(s)** |
| ZTE | Yes |  |
| Qualcomm | Yes | Channel quality is for the downlink channel and as MSG2 is not transmitted with 16QAM then channel quality reporting for 16QAM in MSG3 is not feasible. |
| Huawei HiSilicon | No | Wait for RAN1 first |
| MediaTek | Maybe | Wait for RAN1 agreement before it comes to RAN2. |
| Nokia | No | Wait for RAN1. |
| Sequans | Yes, but OK to wait | Agree with QC, but OK to postpone until more details from RAN1 |

**Conclusion:**

**Proposal:**

In [2], it further proposes to support 16QAM related channel quality reporting in RRC\_CONNECTED state, e.g., by extending the quality report value and/or the "R" bits in current DCQR and AS RAI MAC CE. Details can be FFS and wait for RAN1 and RAN4 agreement. In [5], it also mentions RAN2 should wait for RAN1 and/or RAN4 agreements to decide how to update DCQR and AS RAI MAC control element to support 16-QAM.

Based on above, the following proposal is suggested:

**Draft Proposal 4b: From RAN2 perspective, 16QAM related channel quality reporting can be supported in RRC\_CONNECTED state. Details FFS.**

Companies are invited to provide your feedback on DP4b.

|  |  |  |
| --- | --- | --- |
| **Company** | **Support DP4b (yes/no)** | **Additional comment(s)** |
| ZTE | Yes | In [2], it has mentioned the following possible ways for quality report for 16QAM:   * Alt1: The *Quality report* field can be re-used for 16QAM NPDSCH channel quality report but only the 3 remaining values (e.g. 13, 14, 15) can be used. E.g., if 0~12 is reported, NW can know it’s legacy CQI report. If 13~15 is reported, NW can know it’s CQI report for 16QAM. Alt1 is simplest but the available values are limited. * Alt2: There are two reserved bits in the DCQR and AS RAI MAC control element which might be used. For example, 1 reserved bit can be used as an additional indication. If it’s set to “1”, all the 4 bits of *Quality report* field can be used for new feature, e.g., 16QAM related channel quality. That means at least 16 values can be used for 16QAM feature. * Alt3: If all the two reserved bits can be used, that means at most 51 values can be used for the 16QAM NPDSCH channel quality report.   With above possible ways, it’s no need to introduce new MAC CE or signaling IE for 16QAM related channel quality report. So they can be taken as start point for discussion.  Moreover, we notice that during RAN1 on-going discussion for 16QAM in this meeting, there are opinions that three candidate values for 16-QAM can be added in the legacy table or the decision of candidate values can be left to RAN4/RAN2. In order to make more efficient discussion, we think RAN2 can suggest a value range to RAN1 based on assumption for signaling impacts, e.g., no more than 51 values for channel quality report for 16QAM. |
| Qualcomm | Yes | If RAN1/RAN4 decides existing channel quality values are not sufficient for 16QAM. |
| Huawei, HiSilicon | No | Wait for RAN1 first |
| MediaTek | Maybe | Wait for RAN1 agreement before it comes to RAN2. |
| Nokia | Yes | We think extending CQI for 16QAM is needed for suitable decision at network for MCS selection. |
| Sequans | Probably yes | But better wait for RAN1 |

**Conclusion:**

**Proposal:**

**#Issue 5: Applicability of 16-QAM for PUR and Multi-TB**

As mentioned in [2], considering that 16QAM can only be used in the high channel quality state and the eNB cannot pre-estimate the channel quality of the (later) occasion of PUR transmission when configuring PUR resource, there may be a risk that 16QAM cannot be used under the channel quality when transmitting PUR. So company think RAN1 may need to further evaluate the applicability of 16-QAM for PUR. In [5], it is also proposed that RAN2 should wait for RAN1 to decide on the applicability of 16-QAM for PUR and Multi-TB.

Since companies think RAN2 should wait for RAN1 evaluation or agreement, no proposal is suggested for this issue.

**#Issue 6: Downlink/uplink power configuration**

In [5], it mentions that RAN1 discussion about downlink power configuration has not concluded yet on the signaling details. Moreover, regarding the uplink power configuration to support 16-QAM, RAN1 plan to discuss additional power control parameter in future meeting. RAN2 should continue to wait for RAN1 agreement. Therefore, no proposal is suggested for this issue.

## 14 HARQ processes in DL for HD-FDD Cat M1 UEs

In RAN2#113bis-e meeting, for 14 HARQ processes for eMTC UE, the following agreements are achieved:

|  |
| --- |
| RAN2#113bis-e agreements:   * *14 HARQ activation is configured by dedicated RRC signalling.* * *Working assumption: No change to current L2 buffer size requirement.* |

In RAN2#114e meeting, 14 HARQ processes related issues are further discussed in contribution [3][6].

**#Issue 1: UE capability**

In [3], it mentions that UEs support 14 HARQ should always support 10 HARQ. As 10 HARQ can only be supported in coverage enhancement mode A, company think RAN2 can assume 14 HARQ is only supported in CE Mode A.

The following proposal is suggested:

**Draft Proposal 5: RAN2 assumes that 14 HARQ is only supported in CE mode A.**

Companies are invited to provide your feedback on DP5.

|  |  |  |
| --- | --- | --- |
| **Company** | **Support DP5 (yes/no)** | **Additional comment(s)** |
| ZTE | Yes |  |
| Qualcomm | Maybe |  |
| Huawei | No | There’s no need to assume anything, we can wait for L1 capabilities from RAN1 |
| Sequans | No | Wait for RAN1 |

**Conclusion:**

**Proposal:**

**#Issue 2: L2 buffer size**

As mentioned in [6], since 14 HARQ processes are supported only in DL, it may be justified to increase the total layer 2 buffer size with a factor of 1.25 or 1.3. But considering that this is HD-FDD Cat M1 UEs, no change is required to the current L2 buffer sizes.

As RAN2 already has had working assumption on this issue, the following proposal is suggested:

**Draft Proposal 6: Confirm the working assumption: No change to current L2 buffer size requirement for HD-FDD Cat M1 UEs supporting 14 HARQ processes in DL.**

Companies are invited to provide your feedback on DP6.

|  |  |  |
| --- | --- | --- |
| **Company** | **Support DP6 (yes/no)** | **Additional comment(s)** |
| ZTE | Yes |  |
| Qualcomm | Yes | As per our reply to DP3, L2 buffer sizes in spec are just a guide. |
| Huawei | Yes |  |
| Nokia | Yes |  |
| Sequans | Yes |  |

**Conclusion:**

**Proposal:**

## Max DL TBS of 1736 bits for HD-FDD Cat. M1 UEs

In RAN2#113bis-e meeting, for maximum DL TBS of 1736 bits for eMTC UE, the following agreements are achieved:

|  |
| --- |
| RAN2#113bis-e agreements:   * *DL TBS of 1736 bits is configured by dedicated RRC signalling.* * *FFS: Whether to update L2 buffer size requirement* |

In RAN2#114e meeting, maximum DL TBS of 1736 bits related issues are further discussed in contribution [3][4][6].

**#Issue 1: UE capability**

As mentioned in WID, this feature is supported via “*a Rel-17 optional UE capability to support a maximum DL TBS of 1736 bits for HD-FDD Cat. M1 UEs in CE mode A only*”. Furthermore, in [3], considering that 1736 bits DL TBS feature can be enabled by unicast RRC configuration (as mentioned in RAN1 agreement LS[1]), company proposes that the UE should report its capability by unicast signaling, e.g. by *UE-EUTRA-Capability.*

The following proposal is suggested:

**Draft Proposal 7: The Max DL TBS of 1736 bits capability is defined in *UE-EUTRA-Capability* for HD-FDD Cat. M1 UEs in CE mode A.**

Companies are invited to provide your feedback on DP7.

|  |  |  |
| --- | --- | --- |
| **Company** | **Support DP7 (yes/no)** | **Additional comment(s)** |
| ZTE | Yes |  |
| Qualcomm | Yes |  |
| Huawei | No | There’s no need to agree anything, we can wait for L1 capabilities from RAN1, this proposal assumes proposal 5 is agreed. |
| Nokia | No | Wait for L1 capability from RAN1 |
| Sequans | No | Wait for RAN1 |

**Conclusion:**

**Proposal:**

**#Issue 2: Max DL TBS of 1736 bits configuration**

In RAN1 agreement LS[1], it mentions that the 1736 bits DL TBS feature is enabled by unicast RRC configuration. As RAN2 has achieved the similar stage-2 agreement in last meeting, rapporteur think no need of further discussion in RAN2 and the specific signaling can be left to stage-3 discussion. Therefore, no proposal is suggested for this issue.

**#Issue 3: L2 buffer size**

According to RAN1 agreement LS[1], in [3] and [4], there are similar proposals that the table 4.1A-1 in TS 36.306 for DL Category M1 needs to be updated to indicate 1736 bits TBS and 43008 soft channel bits.

**Draft Proposal 8a: The table 4.1A-1 in TS 36.306 for DL Category M1 needs to be updated to indicate 1736 bits TBS and 43008 soft channel bits.**

Companies are invited to provide your feedback on DP8a.

|  |  |  |
| --- | --- | --- |
| **Company** | **Support DP8a (yes/no)** | **Additional comment(s)** |
| ZTE | Yes |  |
| Qualcomm | Yes | With note to clarify 1736/43008 values apply to UE supporting DL TBS of 1736 bits. |
| Huawei | Yes | This is what RAN1 have requested |
| Nokia | Yes |  |
| Sequans | Yes |  |

**Conclusion:**

**Proposal:**

In [3][4][6], three calculation ways are summarized in the following table:

|  |  |  |
| --- | --- | --- |
| Alts | Tdoc | Details |
| Alt1 | R2-2105660 [4]  (R2#114, HW) | The current L2 buffer requirement is based on 1000 bits TBS in both uplink and downlink, resulting in a peak rate of 2Mbps.  For 1736 bits TBS, the peak data rate can be either ~0.82 Mbps, or ~1.02 Mbps or ~1.23 Mbps depending on whether 8, 10 or 14 HARQ processes are used. It can be seen that even with the increased peak rate for HD-FDD by utilising 1736 TBS and 14 HARQ processes, this does not exceed the peak rate (UL+DL for full duplex). Therefore the L2 buffer size requirement does not increase compared to the currently specified value of 20,000 if we assume the same HARQ RTT (75ms) as for full duplex with 8 HARQ processes.  However, the RTT for the case of HD-FDD with 14 HARQ processes may be 137ms that may result L2 buffer requirement exceeds the current L2 buffer size.  As company think it is unlikely that a HARQ process would reach the maximum number of transmissions while the peak rate is maintained at maximum, for the sake of simplicity, company think the current L2 buffer requirement isn’t updated. |
| Alt2 | R2-2105363 [3]  (R2#114, ZTE) | The total layer 2 buffer sizes ≈ (Maximum number of DL-SCH transport block bits received within a TTI + Maximum number of UL-SCH transport block bits transmitted within a TTI) \* 80/8  Proposal 4a: The UE supports "Total layer 2 buffer size" of 30 000 bytes if the UE indicates not support of *ce-PUSCH-NB-MaxTBS-r14* but support of *maximum DL 1736 bits TBS*.  Proposal 4b: The UE supports "Total layer 2 buffer size" of 50 000 bytes if the UE indicates support of both *ce-PUSCH-NB-MaxTBS-r14* and *maximum DL 1736 bits TBS*. |
| Alt3 | R2-2106158 [6]  (R2#114, Ericsson) | Total layer 2 buffer size for 8 HARQ processes:  *Total layer 2 buffer size = Max(“Maximum number of DL-SCH transport block bits received within a TTI”, “Maximum number of UL-SCH transport block bits transmitted within a TTI”) / 0.001 \* 0.075s / 8.= (1736) / 0.001 \* 0.075 / 8 = 16 275 bytes*  Total layer 2 buffer size can be adjusted for 14 HARQ processes if multiplied with a factor of .~1.3:  *Total layer 2 buffer size = 16275 \* 1.3 = 21158 => 24 000 bytes.*  When maximum number of UL-SCH transport block bits transmitted within a TTI is 2984 bits, the buffer size for a Cat M1 UE supporting max DL TBS of 1736 bits can be calculated as follows:  *Total layer 2 buffer size = (“Maximum number of DL-SCH transport block bits received within a TTI” + “Maximum number of UL-SCH transport block bits transmitted within a TTI”) / 0.001 \* 0.075s / 8.= (2984) / 0.001 \* 0.075 / 8 = 27975 bytes => ~30 000bytes* |

The following proposal is suggested:

**Draft Proposal 8b: RAN2 discuss whether and how to update the L2 buffer size for the UE supporting max DL TBS of 1736 bits.**

Companies are invited to provide your preference on the calculation alternatives above:

|  |  |  |
| --- | --- | --- |
| **Company** | **Preferred Alternatives** | **Additional comment(s)** |
| ZTE | Alt2 | We think change to L2 buffer size is needed.  For Alt3, per our understanding for the company’s principle, we assume the last formula may have the following typo:  *Total layer 2 buffer size =Max (“Maximum number of DL-SCH transport block bits received within a TTI” , “Maximum number of UL-SCH transport block bits transmitted within a TTI”) / 0.001 \* 0.075s / 8.= (2984) / 0.001 \* 0.075 / 8 = 27975 bytes => ~30 000bytes*  Then, it can be seen, the main difference between Alt2 and Alt3 is that the total value of UL TBS and DL TBS is used in Alt2 while the maximum value of UL TBS and DL TBS is used in Alt3. The other factors are similar.  With reference to the discussion for Proposal 3, we think even for HD-FDD UE, it’s possible both the DL data and UL data are buffered and also maximum number of (re)transmissions can be assumed. Therefore, we think it’s more suitable to use total value of UL and DL TBS for L2 buffer size calculation. |
| Qualcomm | Alt1 | It’s not necessary to spend time on this as it is only a guide. |
| Huawei | Alt1 | Alt2 calculation is based on full duplex, it’s not correct. Alt3 is based on HD however it assumes transmission in every TTI which is not the case in practice. |
| Sequans | Alt1 | Agree with HW |

**Conclusion:**

**Proposal:**

**#Issue 4: Applicability of Max DL TBS of 1736 bits for EDT and PUR**

In [3], considering that the maximum TBS of 1736 bits can increase the data rate without significant specification impact, it is proposed that maximum DL TBS of 1736 bits can be supported for PUR. Then a 1736 bits DL TBS activation needs to be configured in *PUR-Config*.

**Draft Proposal 9a: Max DL TBS of 1736 bits can be supported for PUR and a 1736 bits DL TBS activation is configured in *PUR-Config*.**

Companies are invited to provide your feedback on DP9a.

|  |  |  |
| --- | --- | --- |
| **Company** | **Support DP9a (yes/no)** | **Additional comment(s)** |
| ZTE | Yes |  |
| Qualcomm | Yes | The assumption is that network may use smaller TBS when PUR is actually used. |
| Sequans | Yes | We don’t see a reason to limit |

**Conclusion:**

**Proposal:**

In [3], it also mentions complicated specification impacts can be foreseen for introducing DL TBS of 1736 bits into EDT, e.g., how to report UE capability, how to activate the feature and how to avoid unnecessary padding ect? Therefore, from RAN2 perspective, it’s suggested not to support maximum DL TBS of 1736 bits for EDT.

**Draft Proposal 9b: From RAN2 perspective, Max DL TBS of 1736 bits is not supported for EDT.**

Companies are invited to provide your feedback on DP9b.

|  |  |  |
| --- | --- | --- |
| **Company** | **Support DP9b (yes/no)** | **Additional comment(s)** |
| ZTE | Yes |  |
| Qualcomm | Yes | Agree E-UTRAN cannot obtain UE’s capability after MSG1 hence UE cannot be configured in MSG2 for larger DL TBS. |
| Huawei | Yes | The intention is to improve peak throughout, there is no need to support for EDT. |
| Nokia | Yes |  |
| Sequans | Yes | Both not necessary and not feasible |

**Conclusion:**

**Proposal:**

# Conclusion

TBD

# References

1. R2-2104706, R1-2103942, LS on Agreements Related to Support of a maximum DL TBS of 1736 bits as a Rel-17 optional UE capability
2. R2-2105318, Further discussion on 16QAM for NB-IoT, ZTE Corporation, Sanechips
3. R2-2105363, Further discussion on 14 HARQ and DL TBS of 1736bits for eMTC, ZTE Corporation, Sanechips
4. R2-2105660, Support of DL TBS of 1736 bits for HD-FDD Cat. M1 Ues, Huawei, HiSilicon
5. R2-2106078, Support of 16-QAM for unicast in UL and DL in NB-IoT, Ericsson
6. R2-2106158, Total L2 Buffer Size for NB-IoT and LTE-M UEs, Ericsson