3GPP TSG RAN WG2 #4 **Tdoc RAN WG2 371/99**
25-28 May 1999
Berlin, Germany

Source: **WG4**

Title: LS to WG1 on clarification on PC step sizes in the closed loop power control

TO: **3GPP RAN WG1, TSG RAN WG2, TSG RAN**

WG4 would like to thank WG1 for the information related to the work carried on closed loop power control issues and on the multiple step size power control scheme.
As outlined in a previous LS to WG4 (R4-99095), WG4 started to merge power control step requirements defined in ETSI and ARIB.
During WG4#3 meeting the LS from WG1 (R4-99126) and power control issues were discussed and some clarification was felt as needed in relation with the following:

Single step size

UE side:
1) According to WG4 view, the step size defined in S4.01 is the smallest TX power change of the output power TX between the reception of two PC commands.
In the current version of S4.01A, power control step sizes were defined with the associated tolerance for the UE; WG4 choice of the step size was not based on an accurate analysis of the system performances (link level simulations) but the 1 dB is what it is thought to be achievable with present day UE technology.

WG4 is seeking guidance from WG1 on the following topics:
- is the current value of Uplink PC step size of 1 dB considered as appropriate by a system performance point of view ?
- are different or additional (lower) PC step sizes considered useful and worthy to be included in the specifications, if future development of the technology will allow UEs to implement these different PC step size values ?

It is however WG4 belief that the BTS SIR measurement accuracy should also be taken into account when defining the minimum step size; the BTS SIR accuracy is currently under investigation in WG4.

BTS side:
1) According to WG4 view, the step size defined in S4.01 is the smallest TX power change of the output power for a single dedicated channel.
In the current version of S4.01 B, power control step size was defined with the associated tolerance for the BTS ; WG4 choice of the step size was not based on an accurate analysis of the system performances (link level simulations).

Therefore WG4 is seeking guidance from WG1 on the following:

- is the current minimum value of Downlink PC step size of 1 dB considered as appropriate by a system performance point of view (link level simulations) or should a lower value (e.g. 0.5 dB) be considered ?

However, it is WG4 belief that the UE SIR measurement accuracy should also be taken into account when defining the minimum step size for the DL; the UE SIR accuracy is currently under investigation in WG4.

Multiple step size

When considering a TX output power change multiple of the minimum step size in the UE (e.g. uplink slotted mode) or in the BTS, WG4 is requesting WG1 to define which values should be considered in order to assess the correct RF requirements (e.g tolerance related to each multiple step size).

WG4 also stresses that the specification shall be done in such a way to allow changes to the agreed step sizes in a way that will not create backward compatibility problems for early hardware implementation based on first release of specification.

DPCCH/DPDCH

It is current WG4 understanding that the power control commands should be applied to the RF part on the baseband modulated I/Q signal, without therefore impacting the baseband DPDCH/DPCCH gains; WG4 is requesting WG1 and WG2 to confirm its understanding on the application of PC step size in relation to each UL physical channel.

Relation of outer loop power control with closed loop power control

It is WG4 understanding that closed loop power control will be based on Eb/N0 targets set by outer loop power control; WG4 would like to highlight the importance of a correct interworking between outer and closed loop power control, especially if exact BTS behavior on the reception of PC commands sent by UE is not going to be standardized.
Since this subject can be considered as a typical Radio Resource Management issue, WG4 is seeking guidance from WG2 in order to set (if necessary) any RF requirement involving a correct PC outer loop and closed loop interworking.

Closed loop power control and UE behavior
During discussions related to the outage definition, it was acknowledged the importance of defining UE's behavior when closed loop PC is lost; since it is assumed that this topic is not under WG4's scope, WG4 would like to highlight the importance of such a topic to WG2 and WG1.