TSG-RAN Working Group 1 meeting #20 **TSG R1-01-0532**

Busan, Korea
May 21st – May 25th, 2001

Agenda item: 8.1 (Improvement of inter-frequency and inter-system measurements)
Source: ETRI
Title: Enhancement of inter-frequency hard handover for release 5
Document for: Discussion and Decision

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1. Introduction

Tdoc R1-00-0689 pointed out the inter frequency hard handover related problem of current 3GPP's rel'99 specifications. The problem is that several TTI blocks should be missed when the UTRAN does not know the frame offset between the UE's CFN and target BS's SFN. Liaison statements had been exchanged between RAN1 and other working groups to solve this problem [2,3,4,5]. But the opinions of each working group were somewhat different and due to the concern of implementation in time, this item did not further considered for Rel'99 specification.

In addition to the above problem, there is another problem with current Rel'99 specification. This problem is due to the fact that the target BS should find the uplink signal after the UE changed its uplink frequency. After the frequency change, the initial transmit power of UE should only rely on the open loop power estimate. So, the received power at the target BS may be excessively large in some cases but may be very small in other cases. This inaccurate initial power may cause severe uplink synchronization delay for the UE or critical performance degradation for other UEs in the target BS. As a result, frequent call dropping may take place especially when some UEs are in inter frequency hard handover situation. Even dual receiver UE also cannot avoid this problem. In the stage of commercialisation of IS-95 based CDMA cellular system we had experienced this problem. So, the current CDMA cellular system in Korea does not adopt direct inter-frequency hard handover procedure. The situation is more severe in WCDMA, because the round trip delay from the UE and the target BS could not be measured before handover execution. So, the uplink handover search window size heavily depends on the cell coverage (ex, 1024 chip for 40 Km cell coverage).

We feel that the current specification did not fully consider above problems, so in order to improve the performance of inter-frequency hard handover, we propose to make a work item for the enhancement of inter-frequency hard handover for Release 5 specifications or to deal with this item in the existing "improvement of inter-frequency and inter-system measurements" work item (RP-0016).

2. Inefficiency in current specification

2.1 In efficiency when the (single receiver) UE could not measure the SFN_{target}

As stated in the introduction, Tdoc R1-00-0689 pointed out the inter frequency hard handover related problem of current 3GPP's rel'99 specifications [1]. The problem is that the SFN of the handover target cell should be determined by reading the system information block (SIB) transmitted on the BCH of the target cell after having abandoned the old link and before establishing the new link. But in addition to this inefficiency there is another inter frequency hard handover related problem with current specification. In the following sub section, we will describe this problem in detail.

2.2 Uplink synchronization time and initial UE Tx power related problem

The distinctive feature of WCDMA is that each node B operates asynchronously so that it may not be required external timing reference such as GPS. But due to this property, there is no way to estimate the round trip delay ($2T_{p2}$ in figure 1) between the UE and the target node B in the handover situation. In the downlink, the SFN (PCCPCH) frame boundary from target cell can be measured using downlink compressed mode or using dual receiver before inter-frequency hard handover execution. And using the measured chip time offset (T_m in the figure), the frame boundary of DPCH from the target cell can be aligned with that from home cell for time maintained inter-frequency hard handover (or soft handover case).

On the other hand, at the uplink at least $2T_{p2}$ should be required for uplink handover search window. Considering 40 Km cell coverage, the search window becomes about 1024 chips. And the important thing is that the target node B should find the uplink signal via the search window after the UE changes its frequency regardless of whether the UE is a single receiver UE or a double receiver UE.

Figure 1 shows the uplink handover search window for WCDMA [6].

Based on the above assumption, we performed the analysis of uplink handover searcher. This performance analysis was based on the uplink multi-path/handover searcher structure of WCDMA base station, which has being developed in ETRI.
Figure 2 and Figure 3 are the mean acquisition time performance example.
The results in the figure 2 and 3 are the one when the search window size (W) is 1024 chip and subset (Ws) is 64 chip. Subset means the number of chip that the searcher can search at one time.

The detailed parameters for the performance analysis are described in the appendix of this contribution.

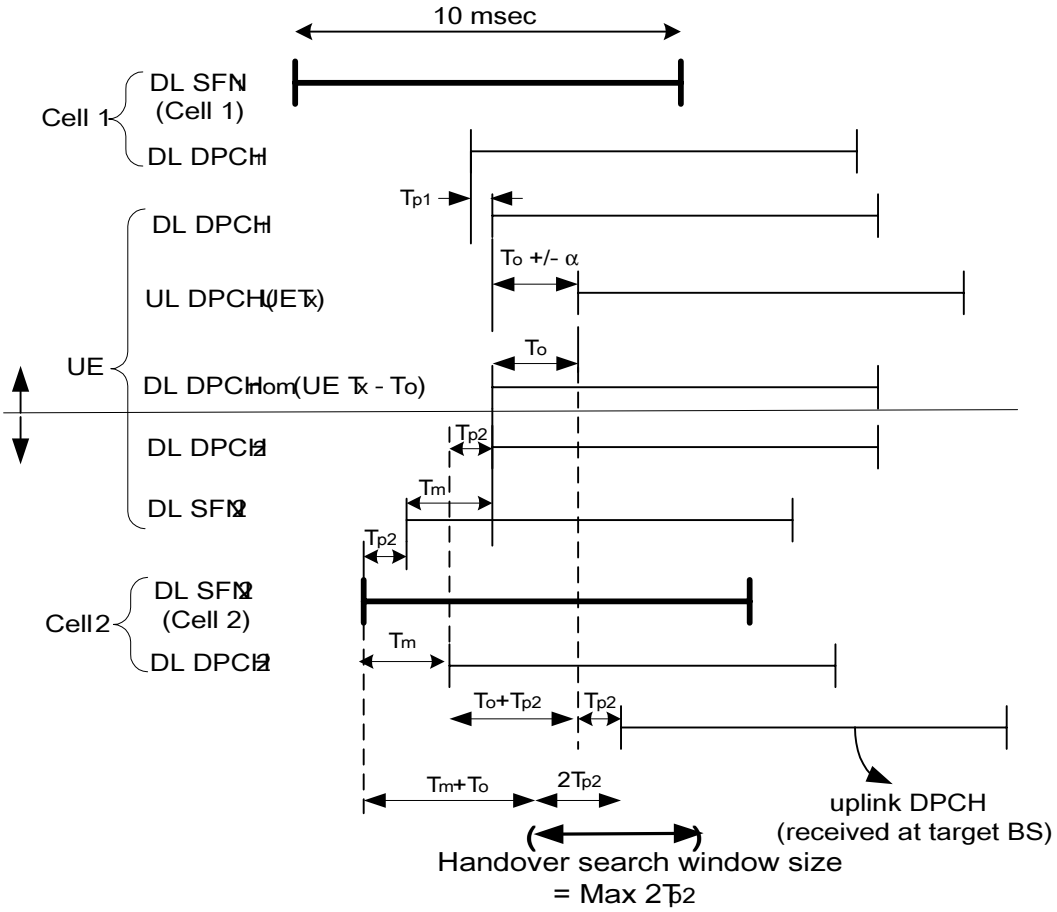

Figure 1. Uplink Handover Search window

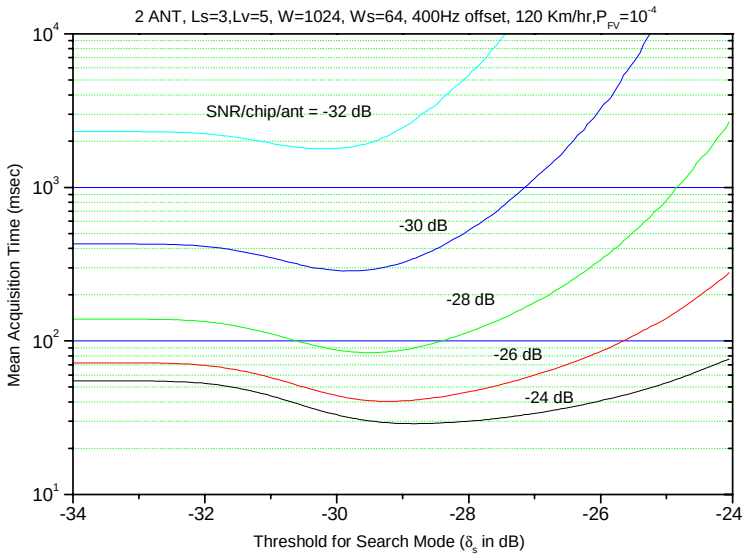

Figure 2. Mean acquisition time performance when Ls=3 slots, Lv=5 slots

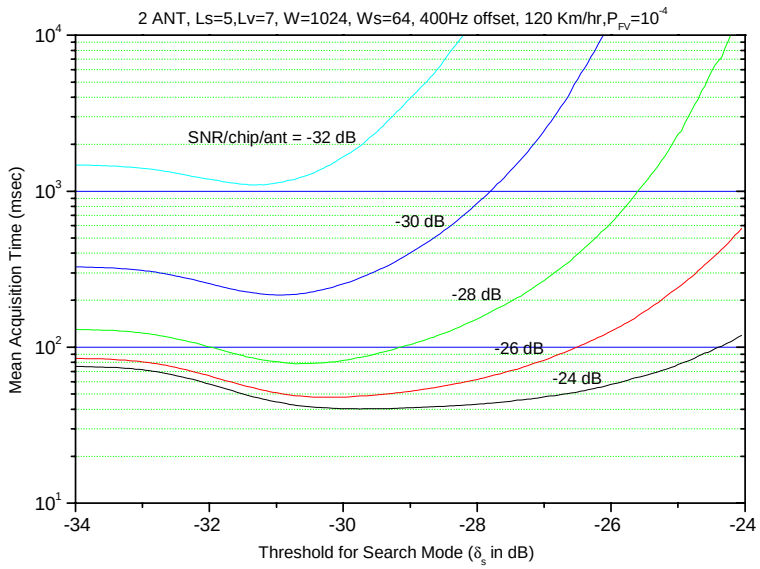

Figure 3. Mean acquisition time performance when Ls=5 slots, Lv=7 slots

The basic assumption of performance analysis was that there is only uplink DPCCH signal before uplink synchronization completion and that the transmitted power of the UE after frequency change is not adjusted.

According to the TS25.214 [7], there are two options for uplink power control before the uplink synchronization completion. The one is slow power up with parameter "*n*", that is, the UE repeat the power up and power down "*n*' times and then increase 1 dB. The other one is fast power up, that is, 1 dB power up per slot. So, the above assumption may be similar with the initial radio link setup power control option 1 with large "*n"*.

After frequency change, the initial UL DPCCH (or power control preamble) transmitted power only relies on the open loop estimation based on the CPICH_RSCP of the target cell. Due to the CPICH_RSCP measurement error and up/down link power unbalancing, the initial received uplink DPCCH SNR/chip at the target node B can deviate from the required value. According to our experience, the amount of the deviation can be larger than 20 dB in worst case. This means that if the required initial uplink DPCCH SNR/chip at the target BS is –20 dB, the real received SNR/chip can be –40 dB or can be 0 dB.

When the initial received SNR/chip is low (ex, –40 dB), if the rate of power up of UE is loose before the synchronization completion, then the acquisition time of target cell may be large as we can foresee in the figures. But when the initial received SNR/chip is high (ex, 0 dB), the interference to other UEs becomes critical, especially when the rate of power up of UE is fast.

(When the received SNR is high the mean acquisition time is reduced. But even though it does, the

acquisition time may take at least several msec. And if the search window is large compared to the number of correlator, then the basic acquisition time is increased. Besides the acquisition time, if we consider the time for finger assignment of target BS and TPC mode change in the downlink and Tx power adjustment of the UE, the total time from the UE's transmission starting time to the steady state (steady state means the time when the uplink signal is normally power controlled so that the received uplink DPCH SNR at the target BS becomes the required target SNR) may be several frames even though the initially received uplink DPCCH SNR/chip is very high. And during this time the interference to other UEs may be great. And if several UEs are in hard handover situation to the target node B, we could not guarantee the uplink performance of the target BS.)

4. Conclusion

In this contribution, in addition to the SFN detection related problem [1] in inter frequency hard handover situation, another problem was pointed out.

This problem is that there may be severe uplink synchronization delay after frequency change of the UE or there may be critical performance degradation for other UEs in the target BS. As a result, frequent call dropping may take place especially when some UEs are in inter frequency hard handover situation. And even dual receiver UE also cannot avoid this problem.

The current specification did not fully consider above problems, so in order to improve the performance of inter-frequency hard handover, we propose to make a work item for the enhancement of inter-frequency hard handover for Release 5 specifications or to deal with this item in the existing "improvement of inter-frequency and inter-system measurements" work item (RP-0016).

[Reference]

[1] Siemens AG, "Neighbor Cell SFN detection for Handover preparation"; TSG-RAN WG1 meeting #13; Tdoc R1-00-0689, Tokyo, Japan, May 22-25, 2000

[2] TSG RAN WG1, "Draft LS on "Neighbor Cell SFN detection for", TSG-RAN WG1 meeting #13; Tdoc R1-00-0798; Tokyo, Japan, May 22-25, 2000

[3] TSG RAN WG2, "Response to LS (R1-000798) on Neighbor Cell SFN detection for Handover", Tdoc R2-00-1284, Oahu, HI, USA, May 22-26, 2000.

[4] TSG RAN WG3, "LS on CFN handing during hard handover", Tdoc R3-00-1949, Helsinki, Finland, 3-7 July, 2000.

[5] TSG RAN WG4, "Response on LS on neighbor cell SFN detection for handover", Tdoc R4-00-537, Paris, France, July 3-7, 2000.

[6] TS25.402 V3.5.0, "Synchronization in UTRAN Stage2"

[7] TS25.214 V3.6.0, "Physical Layer Procedures (FDD)"

Appendix: Conditions for uplink handover searcher performance analysis

The search algorithm used in the analysis was double dwell search algorithm using parallel correlator.

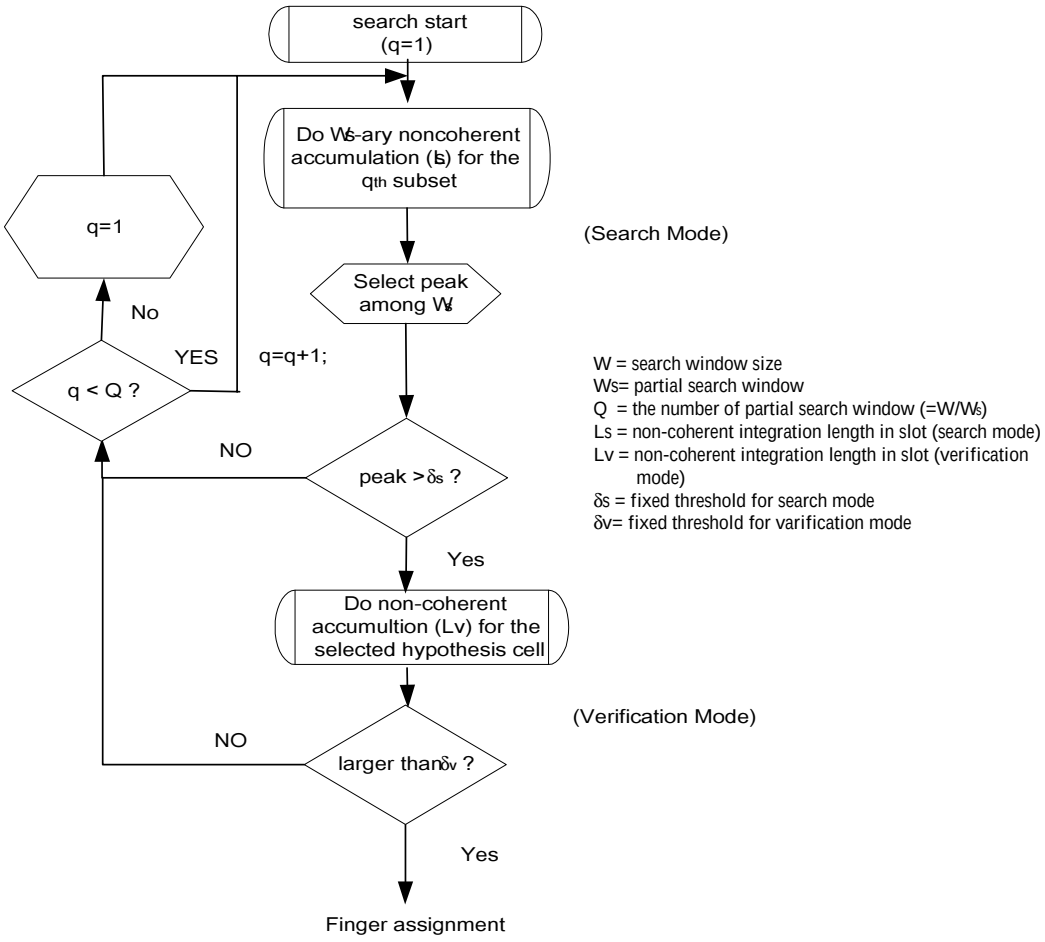

Figure 4. Double dwell hybrid search algorithm

In the search mode, *W* search window is divided into Q subset and the number of test cell in one subset is *W*s (we assume 1 sample per chip, and optimal sampling in this analysis). In the search mode, *W*s test cells are tested simultaneously using *W*s-ary parallel correlator and the time to test one subset is Ts*Ls. Where Ts is the duration of one slot (0.667 msec) and Ls is the non-coherent accumulation length in slot for search mode. In the search mode, the peak is selected among *W*s correlator outputs and then compared with predetermined threshold (δ_s) for search mode.

In the verification mode, verification is performed for the test cell, which passed the hypothesis test in the search mode. The time for the verification is Ts*Lv and where Lv is the non-coherent accumulation length in slot for the verification mode.

If the non-coherently accumulated value via Lv slot is larger than the threshold (δ_v) for the verification mode, search done interrupt is generated and a demodulation finger is assigned for the test cell. And the handover search mode is changed for multipath search mode. The detection threshold for the search mode and verification mode can be transferred for received DPCCH SNR/chip.

State diagram

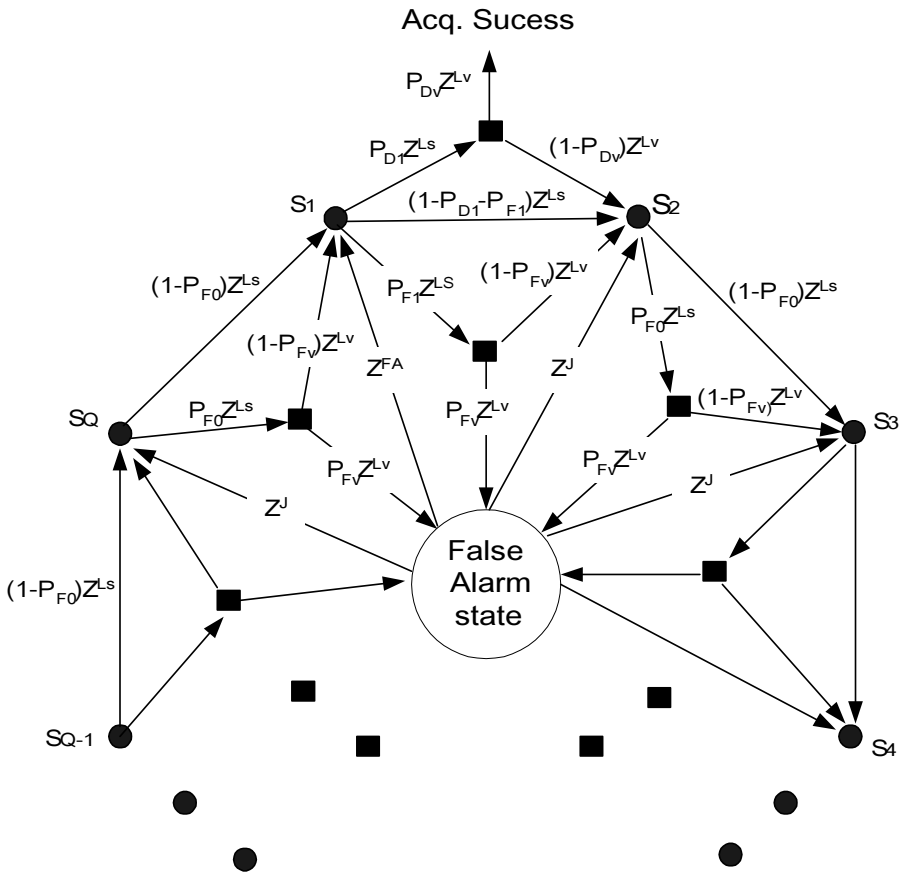

Figure 5. The state diagram for the search algorithm of figure 4

Figure 5 is the state diagram for the search algorithm of figure 4. In the figure, each node, that is, S_1, S_2, . . . , S_Q, represents each hypothesis subset. And the labels on branchs between nodes indicate the probability of the particular transition, multiplide by a power of variable Z. The power is used to indicate the hypothesis testing time periods and basic unit is 1 slot.

The detection and false alarm probability are heavily influenced by L_S, L_V, δ_s, δ_v and the average search time of the handover searcher depends on these probabilities. After all the performance of handover searcher depends on the parameters.

Detection, miss, false alarm probability

Let's define the subset in which the signal exists as H_1 subset and the one in which the signal doesn't exist as H_0 subset. Then as we can see from figure 5, there are following probability, which can influence to the performance of handover searcher.

P_{D1} : Detection Probability of Search Mode in H_1 subset
P_{F1} : False Alarm Probability of Search Mode in H_1 subset
P_{F0} : False Alarm Probability of Search Mode in H_0 subset
P_{Dv} : Detection Probability of Verification Mode
P_{Fv} : False Alarm Probability of verification Mode

Besides the detection and false alarm probability, there is miss probability in the search mode. The miss probability is the probability of the event that both of detection and false alarm do not occur in H_1 subset and equals with $1-P_{D1}-P_{F1}$.

Firstly, by using simulation, we analyzed the detection and false alarm probability of search mode and verification mode according to the SNR/chip and previously mentioned parameters. We assumed 1 sample per chip and optimal sampling. In the simulation, estimated SNR/chip for a selected path was compared with the threshold. And single path fading channel (V=120 Km/hr) with frequency offset of 400 Hz was used.
The pilot field for the DPCCH as 5 bits was used. And the correlator in the searcher utilized the pilot field as well as non-pilot field (that is, TPC, TFCI, FBI field). The coherent integration interval for the pilot field was 5x256 chips and that for non-pilot field was 256 chips. And these values were non-coherently accumulated with optimal weighting factor according to each coherent integration length via Ls slots for search mode, and Lv slots for verification mode.
Figure 6 and 7 shows the detection and false alarm probabilities of search mode for various δ_s values when Ls are 3 slots and 5 slots, respectively.
Figure 8 and 9 shows the detection and false alarm probabilities of verification mode for various δ_v values when Lv are 5 slots and 7 slots, respectively.

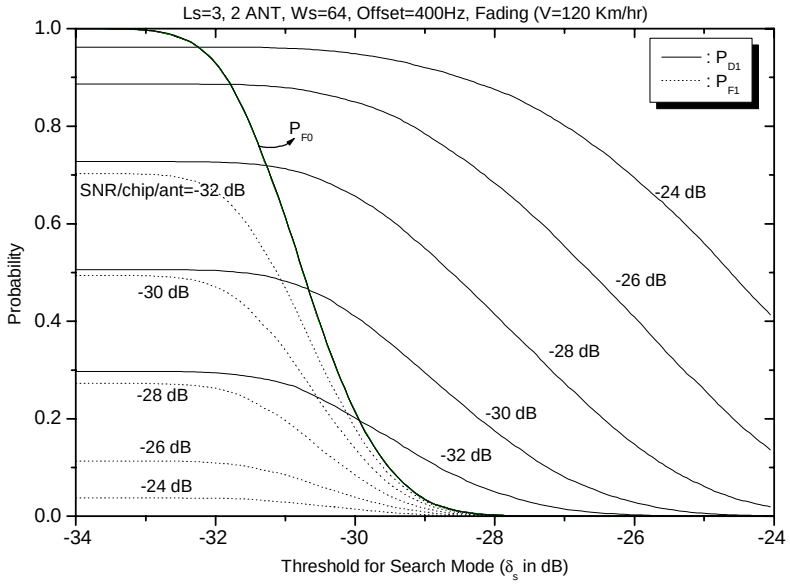

Figure 6. Detection and false alarm probability of search mode (Ls=3)

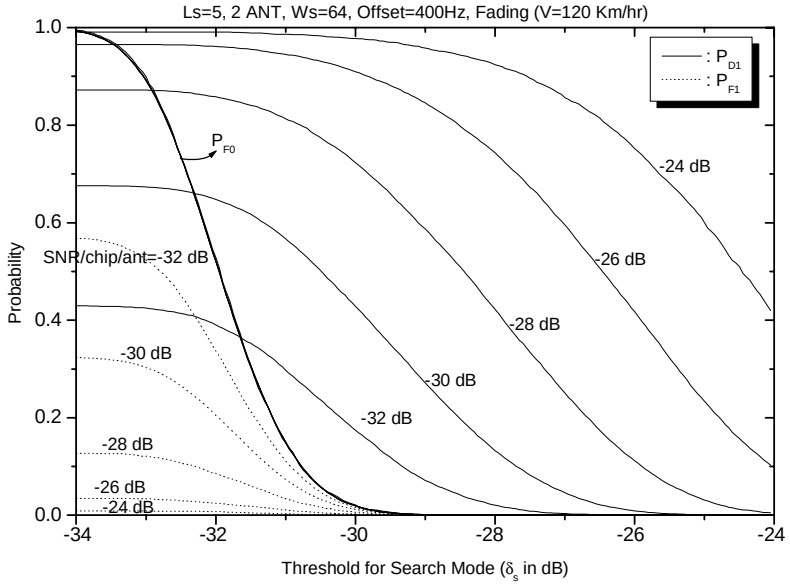

Figure 7. Detection and false alarm probability of search mode (Ls=5)

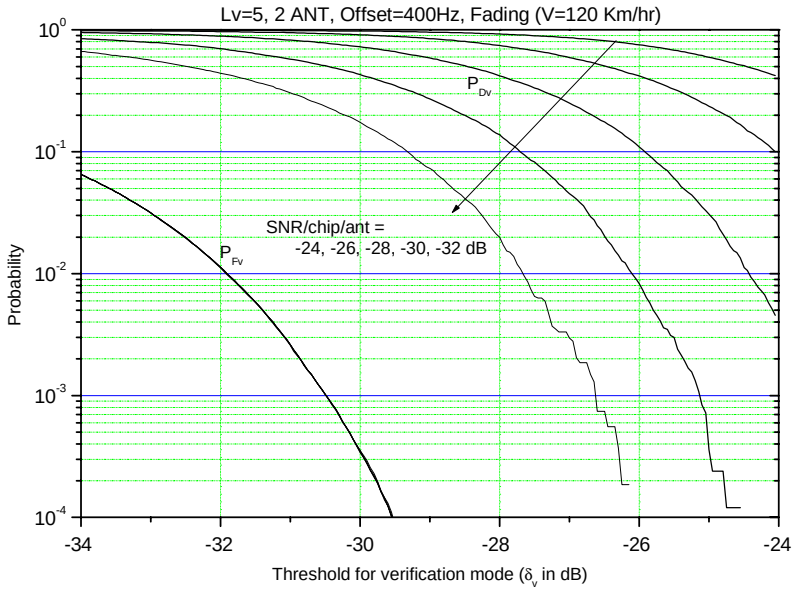

Figure 8. Detection and false alarm probability of verification mode (Lv=5)

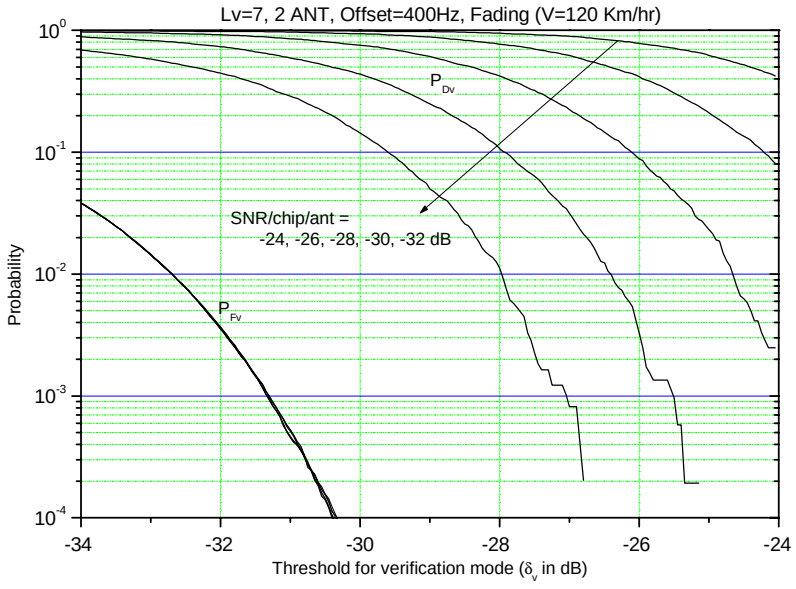

Figure 9. Detection and false alarm probability of verification mode (Lv=7)

Mean Acquisition Time

The mean acquisition time in the figure 2 and figure 3 were based on equation (1) and this equation can be driven from the state diagram of figure 5.

$$E[T_{ACQ}] = \left[\frac{QH_D^{'} + \frac{1}{2}Q(Q-1)H_0^{'}H_D}{QH_D} + \frac{H_M^{'} + (Q-1)H_M H_0^{'}}{1-H_M} \right] \cdot T_s \qquad (1)$$

where

$$H_D = P_{D1}P_{Dv}$$

$$H_D^{'} = (Ls + Lv)P_{D1}P_{Dv}$$

$$H_M = 1 - P_{D1}P_{Dv}$$

$$H_M^{'} = L_s + L_v(P_{D1} + P_{Dv}) - (Ls + L_v)P_{D1}P_{Dv} + JP_{F1}P_{Fv}$$

$$H_0^{'} = L_s + L_v P_{F0} + JP_{F0}P_{Fv}$$

We assumed the false alarm probability for verification mode (P_{Fv}) as 10^{-4} and false alarm penalty time (J) as 300 msec. (when the false alarm is 10^{-4}, the influence of false alarm penalty time to average search time is negligible)