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Agenda Item: **AH24: High Speed Downlink Packet Transmission**
Source: **Sony Corporation**
Title: **Consideration for restriction on H-ARQ processing**
Document for: **Discussion**

1 Introduction

This contribution discusses an issue of memory requirement needed for the support of H-ARQ N-SAW channel structure. It is proposed that additional restriction on resource allocation for H-ARQ SAW channel is applied so that Node-B ensures that buffer over-flow does not occur at UE side. It is also proposed to add H-ARQ buffer memory size as UE capability parameter.

2 H-ARQ Sub-channel Structures

Figure 1 illustrates examples for H-ARQ N-SAW structures with different TTI. From UE implementation point of view, it is preferable to choose a solution with one and only one TTI (Fixed TTI) in a system with smaller TTI length than Release 99. On the other hand, in view of more network flexibility, re-use of R99 architecture, and progressive introduction of HSDPA, multiple TTI in semi-static manner may need to be defined with TTI=15-slot of release 99 being the basis [1]. In general, the memory requirement for H-ARQ increases as TTI becomes larger and H-ARQ memory requirement is burdened by longest TTI defined in a system. If TTI=15-slot is to be defined, impact on memory requirement becomes unpractical if all N-SAW channels need to be decoded/buffered for all TTI with same multi-code capability.

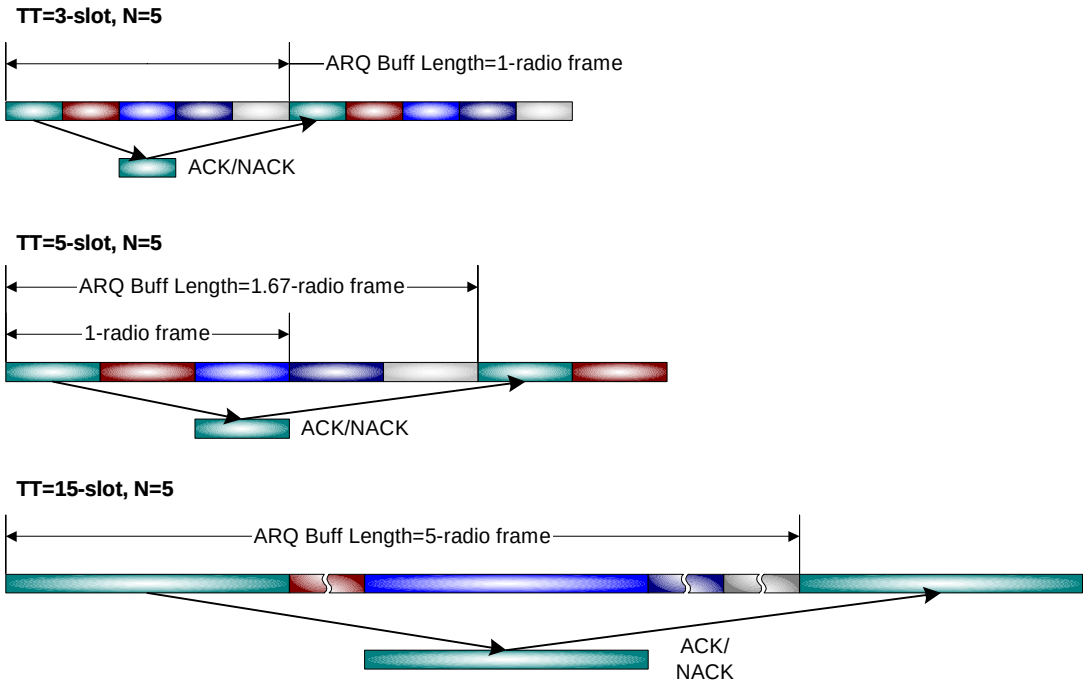

Figure 1 H-ARQ N-SAW channel structures with various TTI

3 Restriction on HS-DSCH resource allocation when using N-SAW H-ARQ channels

If Node-B has explicit knowledge of UE's H-ARQ memory size, its scheduling mechanism can be made to control the HS-DSCH resource allocation so that memory restriction of UE is always met. Rather than UE to require all possible combination of N-SAW H-ARQ processing, it is left for Node-B to assure that data is sent in manner such that UE H-ARQ buffer does not over-flow. Objective here is to avoid excessive memory requirement on UE by allowing to limit UE functionality so that only subset of N-SAW H-AQR processing is done for certain physical layer configuration.

Following two mechanisms can be applied by Node-B to implement the restriction.

- Limiting the maximum number of multi-code

  Maximum number of multi-code used is made TTI dependent. Figure 2 illustrates the basic idea of a scheme. Maximum number of multi-code is reduced as use of longer TTI consumes more H-ARQ buffer memory to support full N-SAW channel.

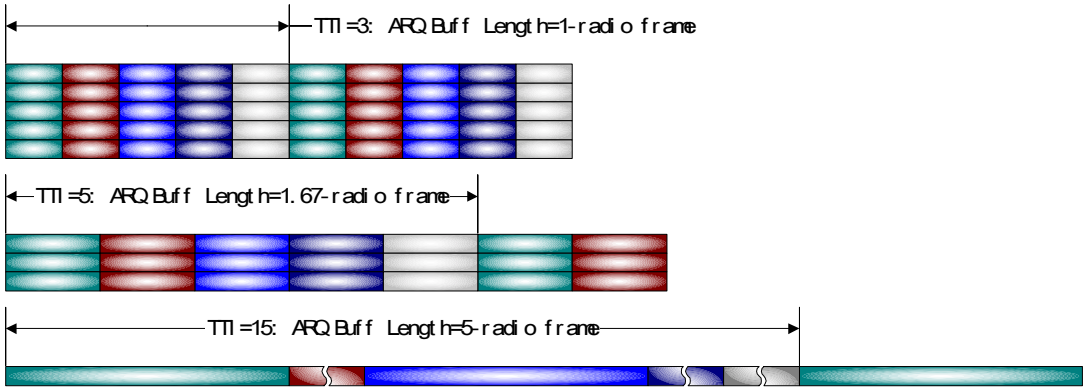

Figure 2 TTI dependent multi-code utilization

- Limiting the use of N-SAW channel

  Resource allocation on sub-channels takes into account for H-ARQ buffer memory capability. Figure 3 illustrates the basic idea of the scheme. Maximum number of sub-channel is reduced as use of longer TTI consumes more H-ARQ buffer memory to support same number of multi-code.

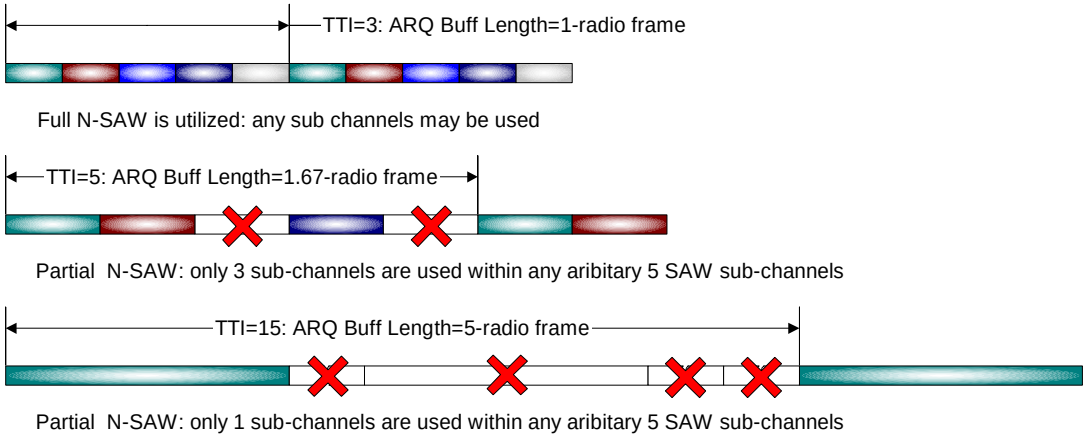

Figure 3 TTI dependent sub-channel utilization

Note that UE does not need to be aware of which mechanism are applied by Node-B as long as H-ARQ memory criteria is met. Node -B is free to choose (or combine) the mechanism to meet the UE's memory criteria. Consequence of adding this restriction is that depending on the TTI being used in a system, peak

rate supported by UE may change--e.g. Longer the TTI, lower the peak rate. However, we do not see disparity in UE capability concept, as this is already the case for release 99.

4 Conclusion

In the case where HSDPA supports multiple TTI (in a semi-static way), it is proposed to add UE capability parameter to indicate H-ARQ memory size. Using this parameter, additional restriction is put on resource allocation by Node-B to ensure that H-ARQ buffer over-flow does not occur in UE. The introduction of this parameter and restriction on resource allocation gives enough freedom for UE implementation so that H-ARQ memory requirement is not necessary dominated or burdened by the longest TTI configuration supported in the system.

5 References

[1] Nortel: “Discussion on Transmission Time Intervals for HS-DSCH”, A12(01)0039: April, 2001

[2] Nokia: “Further buffer complexity and processing time consideration on HSDPA”, A12(01)0003: April, 2001