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To: TSG-RAN WG1

Cc:

Title: Response to LS on DL transmit power setting during UL out-of-synch, TSGR1#19(01)0431

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RAN WG3 would like to thank RAN WG1 for their liaison on DL transmit power setting during UL out-of-sync.

We identified two cases which need to be discussed:

1) UL out of sync before initial synchronisation.

2) UL synchronisation is lost for an RL Set.

Case 1: UL out of sync before initial sync

WG3 has currently specified the DL power setting in case the UL has not obtained initial sync yet. The current specifications indicate that the DL power shall remain constant until the UL sync is achieved and the innerloop is started or until DL power balancing is activated. As a result, some form of power ramping is already supported by activating the power balancing before UL sync is achieved. Note that this ramping will not stop at UL sync detection.

There is sympathy in WG3 for specifying a slow configurable DL power increase (before UL sync is achieved) since the UE might temporarily be in a fading dip and UL sync is expected to be achieved soon. If we see this "automatic power ramping" (in contrast with an explicitly requested ramping based on power balancing commands) as an optimisation, such an automatic ramping could be added e.g. in Release 5 and optionally activated by a Node-B if supported. WG3 would appreciate further input on the relevance of such a solution from WG1. Note that the automatic ramping should only be activated if it concerns a First RL/RL Set to the UE (*First RLS Indicator* IE on NBAP/RNSAP).

Case 2: UL out of sync due to sync loss

~~WG3 have currently not specified the DL - power behaviour in case the UL becomes out of sync.~~ The current WG3 specifications do not specify the behaviour of the DL power when the synchronisation is lost. Since the concerning formulas in WG1 (e.g. 25.214 , subclause 5.2.1.2.2) , do no not indicate any correction of the DL power due to UL sync loss, the understanding in WG3 is that no special corrections (in addition to power balancing) are made in such situations. WG3 believes that power ramping should not be performed in this situation. This because it would increase the load of the Uu interface unnecessarily with RL Sets increasing their DL power in-between UL sync loss and RL_DELETION. The difference with the first situation (UL out of

sync before initial sync) being the fact that in many cases there is no valid expectation of obtaining UL sync soon, e.g. UE has moved away from the cell.

Same is also applied to the TDD in the both cases above.