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Agenda Item: AH22

Source: Nokia and Samsung

Title: Revision of TR25.840 Terminal Power Saving Features including changes to transport channel multiplexing chains during basic gating period

Document for: Discussion and Approval

In this revised TR 25.840 it is proposed further clarifications to multiplexing chains in TS 25.212 in order to guarantee proper operation of OLPC during basic gating period. Namely, we propose a solution which consists of new parameters for rate matching both in uplink and downlink and modification of 2nd interleaving operation. In addition, some minor editorial corrections are made.

7 Impacts to WGs

In this subclause, the technical specifications of each WG that may be impacted by each solution for terminal power saving features are listed.

7.1 Gated DPCCH Transmission Scheme

7.1.1 WG1

TS25.212

7.1.1.1 Changes needed in the transport channel multiplexing chains in TS 25.212

7.1.1.1.1 Physical channel mapping

It is defined in sections 4.2.12.1 and 4.2.12.2, physical channel mapping for uplink and downlink, that during compressed mode, bits are mapped only to certain slots of the frame. Consequently, similar kind of addition is needed for gating, saying that during gating, bits are mapped only to certain slots of the frame. In uplink :

- during basic gating period, the bits are mapped only to those slots, where DPCCH is also transmitted.
- during embedded data period, the bits are mapped to all slots in the frame

In downlink:

- during basic gating period the bits are mapped only to those slots where TPC is also transmitted
- during embedded data period, the bits are mapped to all slots in the frame

Here : basic gating period = frames where only CRCs with zero length TrCH block(s) is (are) transmitted

embedded data period = frames where at least one non-zero length TrCH block is transmitted

This means that during RX gating [5,6], in every Kth frame UE receiver needs to decode the TFCI, before it knows that in what slots the bits are mapped to. If TFCI defines that there are only zero length transport blocks in the frame, then UE knows that the bits are mapped to only certain slots of the frame. And if TFCI defines that there is at least one non-zero length transport block in the frame, then UE knows that the bits are mapped to all slots in the frame.

The similar procedure is required from Node B in uplink, in every frame. Node B has to use pilot energy comparison to detect whether the frame is in basic gating period or in embedded data period. In embedded data period all the pilot fieldsexist. If it detects that the frame is in basic gating period, it knows that DPDCH is transmitted in the same slots as DPCCH. If it detects that the frame is in embedded data period, then it decodes the TFCI, and decodes the data from all slots in the frame.

7.1.1.1.2 2nd Insertion of DTX indication bits in downlink

Presently it is defined in section 4.2.9.2. "2nd insertion of DTX indication bits " that:

- S is the number of bits from TrCH multiplexing
- P is the number of PhCHs ~~bits~~
- R is the number of bits in one radio frame ~~-~~, including DTX indication bits, for each PhCH

Required changes:

1) In embedded data period, the same definition can be used as before. So no changes are needed.

2) During basic gating period, R needs to be replaced by Rgating, where:

- Rgating=R/3 if gating rate=1/3

- Rgating=R/5 if gating rate=1/5

7.1.1.1.3 Rate matching in uplink and downlink

- In uplink:

  In normal gating mode, $N_{data,j}$ needs to be replaced by $N_{data,j}^{gating}$, where:

  $N_{data,j}^{gating} = N_{data,j} / Gating\_rate$,

  where $N_{data,j}$ is the total number of bits that are available for the CCTrCH in a radio frame with transport format combination j.

  $$N_{i,j}^{gating} = \lceil N_{i,j} \times Gating\_rate \rceil \times Channel\_coding\_rate \rceil \times (Channel\_coding\_rate)^{-1},$$

  where $N_{i,j}$ is the number of bits in a radio frame before rate matching on TrCH i with transport format combination j and is an intermediate calculation variable for downlink. By calculating $N_{i,j}^{gating}$ as described above, the number of bits before channel coding, including dummy bits, is guaranteed to be an integer number.

- In downlink:

  In normal gating mode, $N_{data,*}$ needs to be replaced by $N_{data,*}^{gating}$, where:

  $N_{data,*}^{gating} = N_{data,*} / Gating\_rate$,

  where $N_{data,*}$ is the total number of bits that are available for the CCTrCH in a radio frame.

  $$N_{i,l}^{TTI,gating} = \lceil N_{i,l}^{TTI} \times Gating\_rate \rceil \times Channel\_coding\_rate \rceil \times (Channel\_coding\_rate)^{-1},$$

  where $N_{i,l}^{TTI}$ is the number of bits in a transmission time interval before rate matching on TrCH i with transport format l and is used in downlink only. By calculating $N_{i,l}^{TTI,gating}$ as described above, the number of bits before channel coding, including dummy bits, is guaranteed to be an integer number.

- Calculate the number of dummy bits to be attached to CRC bits so that the number of bits after channel coding of "dummy bits + CRC + Tail" will be $N_{i,j}^{gating}$ and $N_{i,l}^{TTI,gating}$ in uplink and downlink, respectively. These dummy bits will be transmitted during switch on time slots in basic gating period.

- In uplink, perform rate matching based on $N_{i,j}^{gating}$ and $N_{data,j}^{gating}$. In downlink, perform rate matching based on $N_{i,l}^{TTI,gating}$ and $N_{data,*}^{gating} \times P \times Rgating$, where P is the number of PhCHs.

The method described above can prevent the unnecessarily large amount of repetition of encoded CRC bits by adding dummy bits.

During embedded data period, the same rate matching for uplink and downlink can be used as when gating is not used.

7.1.1.1.4 2nd interleaving

2nd interleaving operation is modified to guarantee the mapping of encoded CRC bits to the switched on time slots during basic gating period as follows.

- The number of columns of 2nd interleaving matrix is C2 = 30, which is the same as when gating is not used.
- Regarding the calculation of number of rows of 2nd interleaving matrix, it is noted that, during basic gating period, the number of bits in one radio frame for one PhCH, *U*, is 1/3 or 1/5 times of that in normal transmission, according to gating rate. To use currently defined 2nd interleaving matrix with the guarantee that encoded CRC bits are mapped to the switched-on time slots, calculation of the number of rows of 2nd interleaving matrix, R2, is modified as follows: Find the minimum integer R2 such that

$$U \cdot (\text{Gating rate})^{-1} \le R2 \cdot C2$$

  The calculation of R2 described above takes into account the fact that dummy bits are added to the columns of 2nd interleaving matrix that will not be transmitted during basic gating period after inter-column permutation, which is described below.
- From the Table 7 "Inter-column permutation pattern" in section 4.2.11 of TS 25.212, we can know which columns among the columns of 2nd interleaving matrix will be mapped to the switched-on time slots after inter-column permutation.
- Then, write the bits input to the 2nd interleaving row by row only into the columns of 2nd interleaving matrix that will be mapped to the switched-on time slots after inter-column permutation.
- Dummy bits are written into the other columns of 2nd interleaving matrix.
- Additional dummy bits are padded to fill the last row of 2nd interleaving matrix.
- The output of the block interleaver is the bit sequence read out column by column from the inter-column permuted 2nd interleaving matrix. The output is pruned by deleting the dummy bits that were added in the 2nd interleaving.

The modification of 2nd interleaving described above can guarantee that encoded CRC bits are mapped to the switched-on time slots during basic gating period after inter-column permutation, and hence can guarantee the proper operation of 2nd interleaving.

During embedded data period, the same 2nd interleaving can be used as when gating is not used.

~~Presently it is defined in section 4.2.7. "Rate matching" that:~~

~~- $N_{data,j}$ is the total number of bits that are available for the CCTrCH in a radio frame with transport format combination j.~~

~~Required changes:~~

~~1) In embedded data period, the same definition can be used as before. So no changes needed.~~

~~2) In basic gating period, $N_{data,j}$ needs to be replaced by $N_{data,j}^{gating}$, where:~~

~~- $N_{data,j}^{gating} = N_{data,j}/3$ if gating rate=1/3~~

~~$N_{data,j}^{gating} = N_{data,j}/5$ if gating rate=1/5~~

TS 25.214

TS 25.215

7.1.2 WG2

TS 25.301

TS 25.302

TS 25.331

7.1.3 WG3

The impacts of gating to WG3 are described in [2].

7.1.4 WG4

TS 25.101

TS 25.133

8 Performance

8.1 Gated DPCCH Transmission Scheme

8.1.1 Uplink Interference Reduction Gain [3]

In gating, the following transmission cases are possible.

- DPCCH only transmission
- DPDCH and DPCCH transmission