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Title: Further clarifications to outer loop power control during DPCCH gating
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1. Introduction

During the last WG1 meeting outer loop power control modifications during basic gating period were approved [1]. It was proposed that outer loop power control based on CRC attached to zero transport block will be used also during DPCCH gating. This is because DPCCH BER will not offer good enough performance for outer loop. Consequently, this requires changes in multiplexing definitions in the TS 25.212. However, the current implementation of changes in TS 25.212 is not fully optimal. The purpose of this contribution is to further clarify the effects of outer loop power control to multiplexing chains.

2. Clarifications to changes needed in the multiplexing chains in TS 25.212

Regarding the change in 25.212 for gating, the current TR proposes to define new parameters for basic gating period as follows:

- In 2nd insertion of DTX indication bits in downlink:
  - Rgating=R/3 if gating rate=1/3, where R is the number of bits in one radio frame including DTX indication bits
  - Rgating=R/5 if gating rate=1/5

- In rate matching in uplink:
  - $N_{data,j}^{gating} = N_{data,j,}/3$ if gating rate=1/3, where $N_{data,j}$ is the total number of bits that are available for the CCTrCH in a radio frame with transport format combination j.
  - $N_{data,j}^{gating} = N_{data,j}/5$ if gating rate=1/5

However, when employing these definitions the encoded CRC bits are unnecessarily repeated too much, since the number of encoded CRC bits is very small compared to the number of DPDCH bits available in the switch-on time slots during basic gating period. The drawback of this solution is the fact that the unnecessarily large amount of repetition may reduce target SIR in OLPC too much. Thus, the changes presented above do not seem to guarantee the proper operation of the OLPC whose purpose is to prevent the discontinuity in outer loop power control during basic gating period, and hence to guarantee the fast recovery of power control after basic gating period is terminated. In addition, because the current 2nd interleaving is designed assuming that all of 15 slots in a frame are transmitted, the encoded CRC bits for outer loop power control may be allocated to the time slots that are switched off during basic gating period. This also may result in failure of OLPC during basic gating period. To solve the problems described above, we propose a solution which consists of new parameters for rate matching both in uplink and downlink and modification of 2nd interleaving operation.

Firstly, we propose to define new parameters for rate matching and to add dummy bits to CRC.

- Newly defined parameters for rate matching
  - In uplink:

    $N_{i,j}^{gating} = \lfloor N_{i,j} \times Gating\_rate \rfloor \times Channel\_coding\_rate \times (Channel\_coding\_rate)^{-1}$,

    where $N_{i,j}$ is the number of bits in a radio frame before rate matching on TrCH i with transport format combination j and is an intermediate calculation variable for downlink. By calculating $N_{i,j}^{gating}$ as described above, the number of bits before channel coding, including dummy bits, is guaranteed to be an integer number.

  - In downlink:

    $N_{i,l}^{TTI,gating} = \lfloor N_{i,l}^{TTI} \times Gating\_rate \rfloor \times Channel\_coding\_rate \times (Channel\_coding\_rate)^{-1}$,

    where $N_{i,l}^{TTI}$ is the number of bits in a transmission time interval before rate matching on TrCH i with transport format l and is used in downlink only. By calculating $N_{i,l}^{TTI,gating}$ as described above, the number of bits before channel coding, including dummy bits, is guaranteed to be an integer number.

  - Calculate the number of dummy bits to be attached to CRC bits so that the number of bits after channel coding of "dummy bits + CRC + Tail" will be $N_{i,j}^{gating}$ and $N_{i,l}^{TTI,gating}$ in uplink and downlink, respectively. These dummy bits will be transmitted during switch on time slots in basic gating period.

  - In uplink, perform rate matching based on $N_{i,j}^{gating}$ and $N_{data,j}^{gating}$. In downlink, perform rate matching based on $N_{i,l}^{TTI,gating}$ and $N_{data,*}^{gating} \times P \times Rgating$, where P is the number of PhCHs.

The proposed method can prevent the unnecessarily large amount of repetition of encoded CRC bits by adding dummy bits. Secondly, we propose to modify the 2nd interleaving operation to guarantee the mapping of encoded CRC bits to the switched on time slots during basic gating period as follows:

- The number of columns of 2nd interleaving matrix is C2 = 30, which is the same as when gating is not used.
- Regarding the calculation of number of rows of 2nd interleaving matrix, it is noted that, during basic gating period, the number of bits in one radio frame for one PhCH, U, is 1/3 or 1/5 times of that in normal transmission, according to gating rate. To use currently defined 2nd interleaving matrix with the guarantee that encoded CRC bits are mapped to the switched-on time slots, calculation of the number of rows of 2nd interleaving matrix, R2, is modified as follows: Find the minimum integer R2 such that

  $U \times (\text{Gating rate})^{-1} \times R2 \times C2$

  The calculation of R2 described above takes into account the fact that dummy bits are added to the columns of 2nd interleaving matrix that will not be transmitted during basic gating period after inter-column permutation, which is described below.

- From the Table 7 "Inter-column permutation pattern" in section 4.2.11 of 25.212, we can know which columns among the columns of 2nd interleaving matrix will be mapped to the switched-on time slots after inter-column permutation.

- Then, write the bits input to the 2nd interleaving row by row only into the columns of 2nd interleaving matrix that will be mapped to the switched-on time slots after inter-column permutation.

- Dummy bits are written into the other columns of 2nd interleaving matrix.
- Additional dummy bits are padded to fill the last row of 2nd interleaving matrix.
- The output of the block interleaver is the bit sequence read out column by column from the inter-column permuted 2nd interleaving matrix. The output is pruned by deleting the dummy bits that were added in the 2nd interleaving.

We think that the proposed solution guarantees that the encoded CRC bits are mapped only to the switched-on time slots, and hence guarantees the proper operation of OLPC.

5. Conclusion and proposal

In this contribution it is proposed further clarifications to multiplexing chains in TS 25.212 in order to guarantee proper operation of OLPC during basic gating period. Namely, we propose a solution which consists of new parameters for rate matching both in uplink and downlink and modification of 2nd interleaving operation.

The proposed TR text on this issue is given in a separate contribution, R1-01-0337.

References

[1] R1-01-0009, Nokia, " Further clarifications to outer loop power control during DPCCH gating" , Boston, U.S.A. , January 15-18, 2001.