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Title: Text Proposal for performance of MPIC in TR25.841
Agenda Item: AH24 (HSDPA)
Document for: Discussion

1. Introduction

In last TSG RAN WG1 meeting, we introduced MPIC which mitigate severe multipath interference [1]. In the document, it was concluded that multi-level data modulation such as 16QAM and 64QAM could be effective in the throughput performance of HSDPA by employing a high performance receiver such as MPIC. Based on the document this contribution shows the text proposal of the simulation results of MPIC for TR25.848. The intentions of these descriptions are to show an example of possible solutions to combat severe multipath interference and to indicate the effectiveness of multi-level data modulation such as 64QAM. Note that it is out of our intention to show the detailed algorithm of MPIC since MPIC algorithm is an implementation matter.

(We will also introduce the complexity analysis for the MPIC in this meeting [2].)

2. Text proposal for TR25.848

7.1.2 Complexity Evaluation

7.1.2.1.1 Complexity impacts to UE

7.1.2.1.1.1 Introduction

7.1.2.1.1.2 Detection of MCS applied by Node-B

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7.1.2.1.2.5 Measurement/Reporting delay

7.1.2.1.1.6 Advanced Technologies

7.1.2.1.1.6.1 Interference Canceller and Equalizers for Higher Modulation

In an actual propagation channel, multipath (frequency-selective) fading appears in a 5-MHz bandwidth. Although the multipath interference (MPI) of HS-DSCH is suppressed to $1/PG$ on average (PG denotes process gain), severe MPI degrades the SIR, and consequently the throughput performance since the PG must be nearly 1 to achieve throughput higher than 10 Mbps. Interference canceller and Equalizers are known as possible solutions to mitigate the severe multipath interference. In WG1, throughput performance of the MPIC was evaluated as an example of this type of receiver. Table 1 shows the simulation conditions.

Table 1. simulation conditions

Spreading Factor	32
Number of codes for HS-DSCH	20
Modulation	16QAM (MCS 1), 64QAM (MCS 2)
HSDPA TTI length	0.667 ms
CPICH E_c/I_{or}	-9.54 dB (11% of I_{or})
DSCH E_c/I_{or}	-0.51 dB (89% of I_{or})
Antenna diversity	2-branch
Channel model	1 or 2-path Rayleigh
MPIC structure	1) Perform despreading and rake combining for

	each code. (If iterated 4 times, then stop these process and output to turbo decoder) 2) Generate interference replica for each code by using hard-decision data sequence and each spreading code. 3) Remove the replica from received signal 4) Go to 1)
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Figure 1 shows the throughput performance as a function of $I_{or}/(I_{oc}+N_0)$ in 1- and 2-path fading channel. In 2-path fading channel, throughput performance with and without 4-stage MPIC were plotted. In single-path channel, MCS2 which employs 64QAM can achieve higher maximum throughput compared with MCS1 with 16QAM in enough high $I_{or}/(I_{oc}+N_0)$ region. However in 2-path fading channel, throughput with MCS2 were severely degraded due to the severe MPI of its own channel without MPIC. As a result, MCS2 cannot improve throughput compared to that with MCS1 in any $I_{or}/(I_{oc}+N_0)$ region without MPIC in 2-path fading channel. On the other hand, when MPIC was applied, almost the same or higher throughput can be obtained in 2-path fading channel compared to that in single-path channel owing to accurate MPI cancelling and Rake diversity effect. Therefore 64QAM data modulation combined with MPIC can increase the maximum throughput even in multipath fading channels.

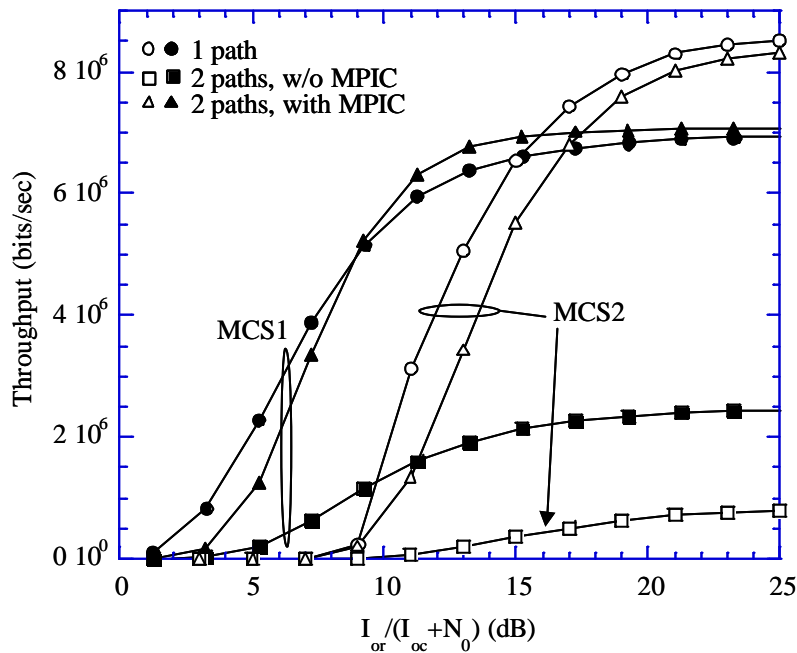


Fig. 1 Throughput performance

3. Conclusion

In this contribution the text proposal of the simulation results of MPIC for TR25.848 are described. The intentions of these descriptions are to show an example of possible solutions to combat severe multipath interference and to indicate the effectiveness of multi-level data modulation such as 64QAM.

References

- [1] R1-01-0102, NTT DoCoMo, "Multipath Interference Canceller (MPIC) for HSDPA and Effect of 64 QAM Data Modulation," Boston, USA, January 15-18, 2001.
- [2] R1-01-0329, NTT DoCoMo, "Complexity Analysis on MPIC for HSDPA," Las Vegas, USA, Feb 27th -Mar 2nd, 2001.