TSG-RAN Working Group 1 meeting #19 *TSGR1-01-0328*

Las Vegas, USA, February 27th - March 2nd, 2001

Agenda Item: **Plenary (Release 99)**

Source: **Panasonic**

Title: **Downlink channelization code phase**

Document for: **Discussion**

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1. Introduction

This document looks at the downlink channelization code phase, which seems not clearly described in TS25.213. The channelization code phase is aligned to 256 chip boundary is specified. Hence only SF=512 case has an issue. There seems two understanding of the current specification. One is aligned to the CPICH frame timing. The other is aligned to the DPCH frame timing, i.e. each channelization code has a frame offset. It seems both understanding does not make any contradiction, but we should make the decision with little impact to other parts. We would like to invite the discussion about this.

2. Downlink channelization code phase

There seems two understanding of downlink channelization code phase.

1) Aligned to data frame timing
   This comes from the assumption of the symbol phase are aligned to channelization code phase.

2) Aligned to CPICH frame timing
   This comes from the assumption of downlink chip phase is always aligned to CPICH frame boundary. This has a possibility of node-B implementation a little easy because channelization code part does not have to have offset to each DPCH.

Note that S-CCPCH does not have the format of SF=512. So only DPCH with SF=512 has an issue. SF=512 already does not have orthogonal if 256 chip frame offset is used. Current limitation treated as [1] in SF=512 does not impact on this discussion.

3. The impacts to the implementation

The channelization processing parts may be implemented by the hardware. LSI modification cost. We look to the possible impact of the implemented products.

Downlink SF=512 is option in the UE and the NodeB. The manufacture which does not implement SF=512 is not a problem. If SF=512 is implemented based on the one of above understanding and if the discussion conclude other side, following modification may save from the hardware modification.

"If the frame offset is not multiple of 512 chips and the channelization code is odd number, the data symbol should be transmitted as reversed, e.g. 1 is transmitted -1 and -1 is transmitted 1."

If channelization code is an even number, first 256 chips and last 256 chips are same. So this does not bring the modification. The channelization code of odd number consists of first 256 chips and the reversed first 256 chips. If the specification is settled to the opposite understanding, in the case the frame offset is not multiple of 512 chips, reversed parts comes first and non-reversed parts comes last. This can compensated by the data symbol is transmitted/received as reversed symbol.

5. Conclusions

We looked at the downlink channelization code phase and pointed out two possibility of the understanding. We also look to the impact to the implementation. We invite the discussion in RAN1 to settle this issue.

Reference

[1] R1-01-0247CR25.213-038, Clarification of channelization codes when SF=512, Siemens and Panasonic