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Source: Lucent Technologies

Title: Further results on the impact of code block size on HSDPA performance

Document for: Discussion

1 Introduction

Reference [1] studies the impact of code block size on HSDPA performance. The conclusion drawn there is that at high Block Error Rate (BLER), there is negligible difference between different code block sizes. At BLER values in the 1% range, the difference between block size of 640 bits and 5120 bits is around 0.5 dB. It is further concluded in [1] that the difference in throughput between the code block sizes for the cases considered there is small. This document presents modified results from [2] and some additional results on the effect of code block size.

2 Effect of Code Block Size

2.1 Turbo code performance

We present here modified results from that presented in [2], which used a different Turbo interleaver than that specified by 3GPP. Upon making this modification, with all other assumptions staying the same as in [2] (repeated here in Table 1), the results of Figure 1 are obtained for QPSK and an effective code rate of 0.1 (Turbo coding and repetition). Comparing the results of Figure 1 with that of [1], we find that the results agree fairly closely.

Table 1. Simulation parameters

Parameter	Value
Channel Model	AWGN
Overhead Power Allocation (CPICH+P-CCPCH+S-CCPCH+SCH+PICH…)	20% (-7dB)
Max Traffic Channel Power Allocation	-1dB
$\hat{I}_{or}/I_{oc}$	Variable
No of iterations for Turbo Codes	8
Metric for Turbo Code	Max
Turbo Code Rates	0.2-0.8
Input to Turbo Decoder	Soft
CRC	16 bits
Tail bits	6
Turbo Interleaver	As per 3GPP (modified to handle higher data rates)

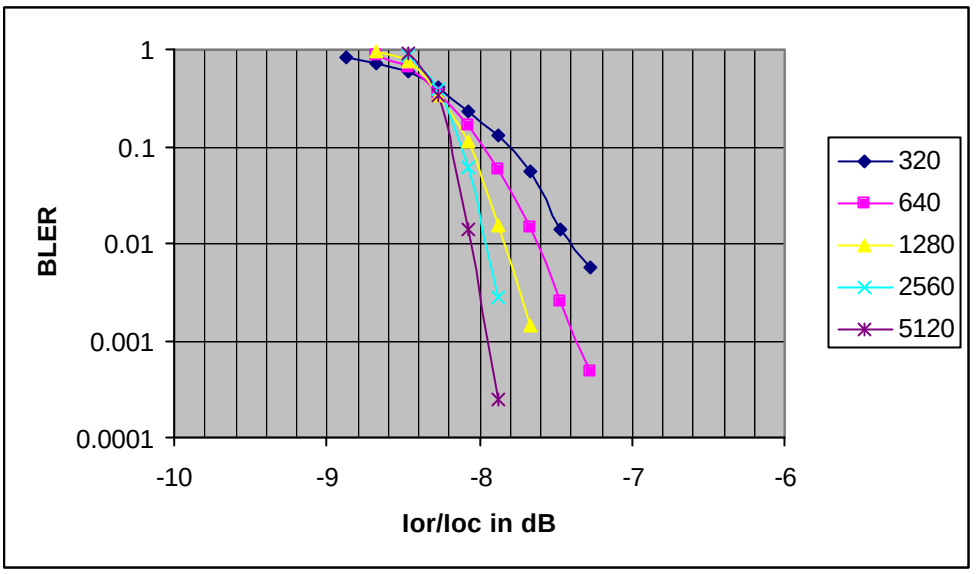

Figure 1: BLER vs. Ior/Ioc for MCS4 from [2] (QPSK, effective code rate of 0.1) and different code block sizes (in bits).

A comparison similar to that of Figure 1 is shown in Figure 2 for the case of MCS2 of [2] (QPSK with effective code rate of 0.025). This corresponds to a bit-rate of 120Kbps and therefore, with a fixed TTI of 1 slot, a code block size of 80 bits would be used [3]. The comparison shows that at a BLER of 1%, 80 bits code block would require about 1.3dB higher Ior/Ioc as compared to a code block size of 1280 bits.

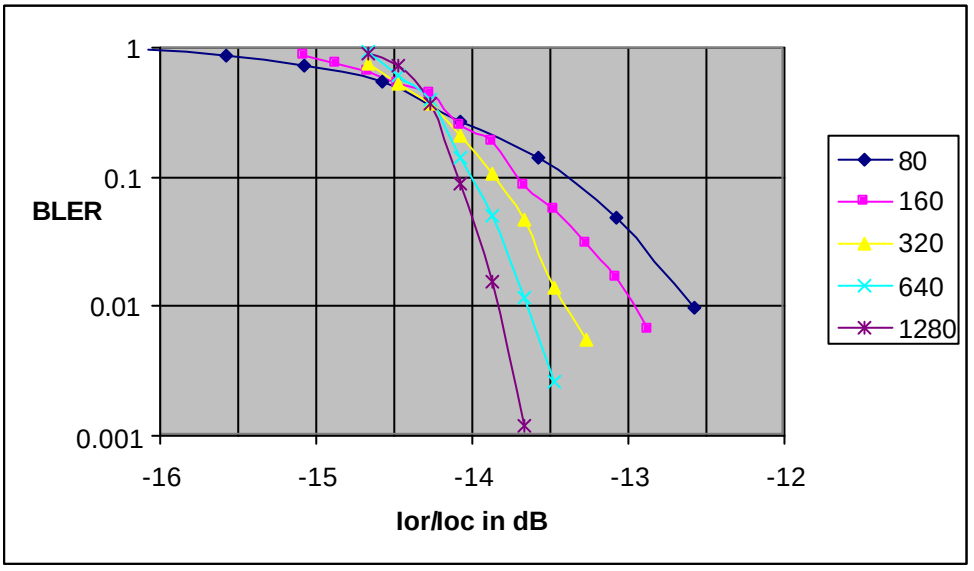

Figure 2: BLER vs Ior/Ioc for MCS2 from [2] (QPSK, effective code rate of 0.025) for different code block sizes.

While it is true that with HARQ the targeted BLER for initial transmission will be high, the throughput performance for a given MCS level depends additionally on

a) residual BLER at which we operate and

b) steepness of the BLER vs. Ior/Ioc curve between the initial BLER and the targeted residual BLER for the different code block sizes.

Note that for a given MCS level as the code block size decreases the BLER vs. Ior/Ioc curve becomes less steep (as seen in Figure 1 and Figure 2).

For the block sizes and MCS levels considered in [1] the difference in throughput was pointed out to be small. It is important to compare the throughput performance in the Ior/Ioc region where the MCS is likely to be chosen. Here, we have shown a throughput comparison between a block size of 160 bits and a block size of 2560 bits for MCS3 in [2] (QPSK modulation with an effective code rate of 0.05 for a resultant bit-rate of 240Kbps). The choice of such a low MCS level is not unlikely especially in cases when the power fraction available for the HS-DSCH channel (left over from serving dedicated channel users) is small. Fixed TTI schemes with single slot TTI would Turbo encode 160 bits and transmit the coded bits over duration of 0.667ms. The variable TTI scheme outlined in [2] would Turbo encode 2560 bits and transmit the block over 16 slots. Figure 3 shows a comparison of the BLER vs. Ior/Ioc for the two code block sizes considered and the resultant throughput performance is shown in Figure 4. It should be pointed out that with small code block sizes the percentage overhead due to CRC, tail bits etc. becomes large as compared to the case of using large code block sizes. Therefore, the throughput curves reflect the overhead due to CRC (16 bits) and tail bits (6 bits). As can be seen, in the Ior/Ioc region of -11.5dB to –10dB (where this MCS will likely be selected), there is noticeable degradation in performance with the smaller code block size.

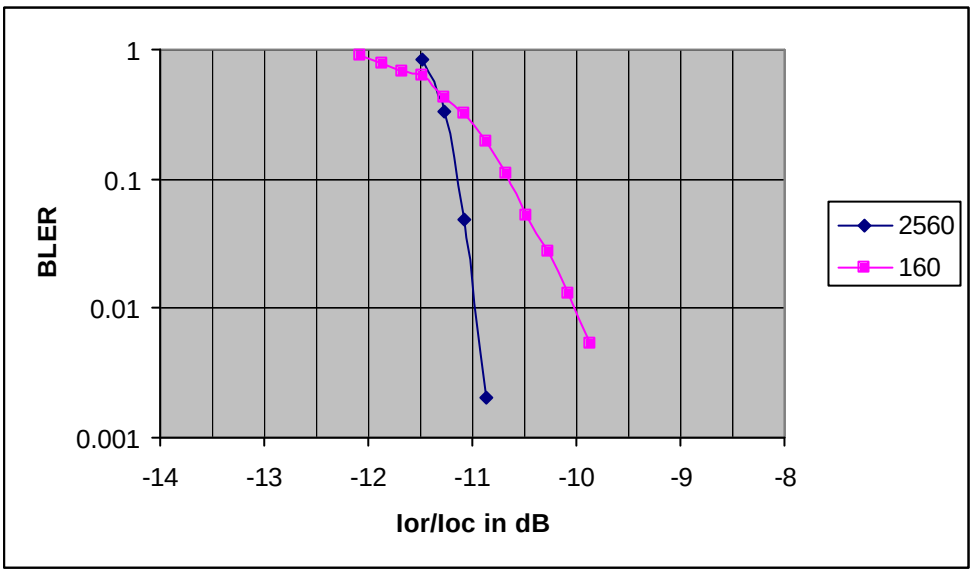

Figure 3: BLER vs. Ior/Ioc for MCS 3 from [2] (QPSK and code rate=0.05) for two different code block sizes.

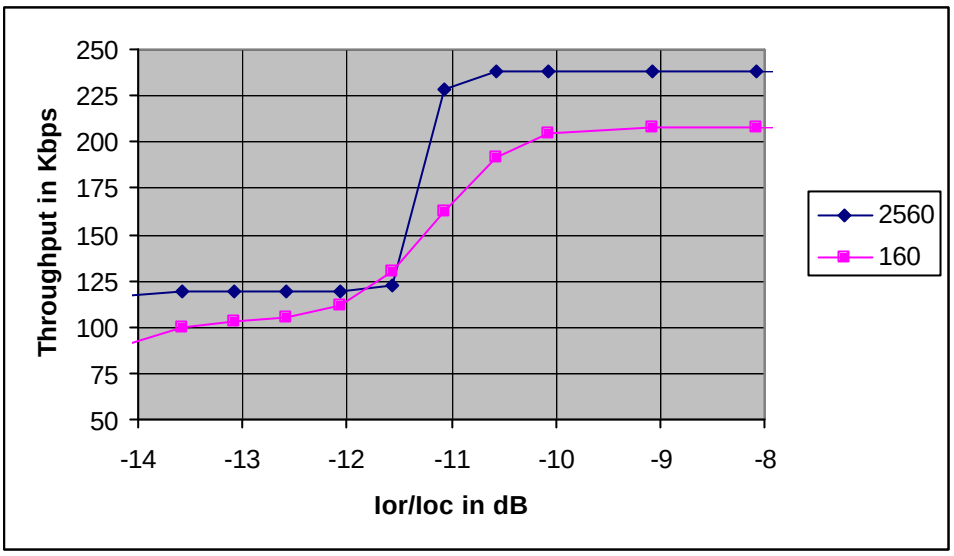

Figure 4: Throughput comparison of two different code block sizes using MCS3 (QPSK and effective code rate of 0.05).

Such a comparison of code block sizes must be performed for fading channels as well before final conclusions are made.

The effect of code block size on BLER was also studied for high MCS levels and the difference in required Ior/Ioc (for a given power fraction) for small versus large code block sizes increases. Table 2 shows the difference in Ior/Ioc for different MCS levels at 1% BLER.

Table 2: Comparison of required Ior/Ioc for different MCS levels and code block sizes.

MCS	Modulation	Effective Coding rate (coding and repetition)	Ior/Ioc in dB at 1%BLER	
			Code Block 640 bits	Code Block 5120 bits
5	QPSK	0.2	-4.5	-4.9
7	QPSK	0.8	4.6	3.8
8	16-QAM	0.8	11.1	10.4

2.2 Signalling overhead

The performance of smaller versus larger code blocks will also depend upon the signalling overhead. For HSDPA operation, following signalling will be necessary per code block [3]:

?? identifying the UE(s) to which HSDPA data is transmitted in a given HSDPA TTI.

?? identifying which HSDPA codes are assigned to a UE in a given HSDPA TTI (if sharing in the code domain, i.e. code multiplexing is to be supported for HSDPA transmission)

?? identifying modulation and coding scheme used for HSDPA transmission in a given HSDPA TTI.

?? identifying relative CPICH to DSCH power ratio for a HSDPA transmission in a given HSDPA TTI (specifically for QAM modulation).

?? identifying or setting current states of fast Hybrid ARQ

For small code block sizes the overhead per information bit will be higher compared to large code block sizes. For example, this overhead will be 16 times greater for 160 bits code block compared to 2560 bits long code block. In addition, the signalling information will not have the benefit of HARQ and consequently have to be transmitted at a much higher reliability (higher E_b/N_o).

3 Conclusions

Simulation results comparing the performance of Turbo code block sizes have been presented. These results are modified from those shown in [2] and do agree with the results of [1]. It is further pointed out that when very small code block sizes are used (as may be required with fixed and small TTI values to support small enough bit-rates), there is noticeable throughput degradation as compared to large code block sizes. Moreover, it should be noted that the percentage overhead with smaller code block sizes is large as compared to large code block sizes. It was also found that the difference in Ior/Ioc required for small code block size versus large code block size increases with MCS level.

The variable TTI approach provides the flexibility to operate with a large code block size even at low data rates. In addition, the variable TTI approach provides other benefits such as adapting MCS for retransmissions, low signalling overhead and selecting the code block size (for a given MCS level) based on backlog to reduce frame fill inefficiency as outlined in [2].

4 References

[1] "Impact of block length on Turbo-code performance for HSDPA", TSG-RAN #19(01) 0244, Ericsson.

[2] "Variable TTI proposal for HSDPA", TSG-RAN1#18 (00), R1-01-0079, Lucent Technologies.

[3] "Physical Layer Aspects of UTRA High Speed Downlink Packet Access" TR25.848 V0.5.0, R1-01-0186.