3GPP TSG-RAN WG1 Meeting 19th ***Tdoc R1-01-0266***
Las Vegas, U.S.A, Feb 27 – Mar 2, 2001

Agenda item:	**REL-4 CRs**
Source:	**Samsung and Nokia**
Title:	**TS 25.214 CR, Addition of general description of gated DPCCH transmission to TS 25.214**
Document for:	**Approval**

Introduction

This contribution introduces the CR for addition of general description of gated DPCCH transmission to TS 25.214 which is based on TR 25.840 "Terminal Power Saving Features" v2.2.0 (R1-01-0296).

Summary of Changes

First, the operation of gated DPCCH transmission is described in chapter 9 (new chapter) as follows.

- Section 9.1 describes the basic concept of gated DPCCH transmission (gating).
- Section 9.2 describes parameters for gating.
- Section 9.3 describes operation of gating in detail.
- Section 9.4 describes how to detect DPDCH data during gating.
- Section 9.5 describes in which time slots DPCCH transmission is turned on.

Secondly, an informative annex is added which includes two figures that conceptually illustrate the operation of gating.

Contact Person

Ju Ho Lee : juholee@samsung.com
Sungoh Hwang : sungoh@samsung.com
Markku Tarkiainen: markku.tarkiainen@nokia.com

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CR-Form-v3

CHANGE REQUEST

✍ **25.214**	**CR**	**CR-0151** ✍	rev **-** ✍	Current version:	**3.5.0** ✍

*For **HELP** on using this form, see bottom of this page or look at the pop-up text over the ✍ symbols.*

Proposed change affects: ✍ (U)SIM [ ] ME/UE [X] Radio Access Network [X] Core Network [ ]

Title: ✍	Addition of general description of gated DPCCH transmission to TS 25.214		
Source: ✍	Samsung and Nokia		
Work item code: ✍	RlnImp-TPS	***Date:*** ✍	March 2, 2001
Category: ✍	**B**	***Release:*** ✍	REL-4
	Use one of the following categories: ***F*** *(essential correction)* ***A*** *(corresponds to a correction in an earlier release)* ***B*** *(Addition of feature),* ***C*** *(Functional modification of feature)* ***D*** *(Editorial modification)* Detailed explanations of the above categories can be found in 3GPP TR 21.900.		*Use one of the following releases:* *2 (GSM Phase 2)* *R96 (Release 1996)* *R97 (Release 1997)* *R98 (Release 1998)* *R99 (Release 1999)* *REL-4 (Release 4)* *REL-5 (Release 5)*

Reason for change: ✍	Addition of general description of gated DPCCH transmission scheme in order to include gated DPCCH transmission in REL-4 specification.
Summary of change: ✍	The operation of gated DPCCH transmission scheme is described in chapter 9 of TS 25.214 as new chapter. An informative annex is added to present the conceptual illustrations of gated DPCCH transmission.
Consequences if not approved: ✍	Further improvement in UE battery life and interference reduction can not be achieved in REL-4.

Clauses affected: ✍	9 (new chapter), New informative annex	
Other specs Affected: ✍	[ ] Other core specifications [ ] Test specifications [ ] O&M Specifications	✍
Other comments: ✍		

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8 Idle periods for IPDL location method

8.1 General

To support time difference measurements for location services, idle periods can be created in the downlink (hence the name IPDL) during which time transmission of all channels from a Node B is temporarily seized. During these idle periods the visibility of neighbour cells from the UE is improved.

The idle periods are arranged in a predetermined pseudo random fashion according to higher layer parameters. Idle periods differ from compressed mode in that they are shorter in duration, all channels are silent simultaneously, and no attempt is made to prevent data loss.

In general there are two modes for these idle periods:

- Continuous mode, and
- Burst mode.

In continuous mode the idle periods are active all the time. In burst mode the idle periods are arranged in bursts where each burst contains enough idle periods to allow a UE to make sufficient measurements for its location to be calculated. The bursts are separated by a period where no idle periods occur.

8.2 Parameters of IPDL

The following parameters are signalled to the UE via higher layers:

IP_Status: This is a logic value that indicates if the idle periods are arranged in continuous or burst mode.

IP_Spacing: The number of 10 ms radio frames between the start of a radio frame that contains an idle period and the next radio frame that contains an idle period. Note that there is at most one idle period in a radio frame.

IP_Length: The length of the idle periods, expressed in symbols of the CPICH.

IP_Offset: A cell specific offset that can be used to synchronise idle periods from different sectors within a Node B.

Seed: Seed for the pseudo random number generator.

Additionally in the case of burst mode operation the following parameters are also communicated to the UE.

Burst_Start: The SFN where the first burst of idle periods starts.

Burst_Length: The number of idle periods in a burst of idle periods.

Burst_Freq: The number of radio frames of the primary CPICH between the start of a burst and the start of the next burst.

8.3 Calculation of idle period position

In burst mode, the first burst starts in the radio frame with SFN = Burst_Start. The *n*:th burst starts in the radio frame with SFN = Burst_Start + *n*? Burst_Freq. The sequence of bursts according to this formula continues up to and including the radio frame with SFN = 4095. At the start of the radio frame with SFN = 0, the burst sequence is terminated (no idle periods are generated) and at SFN = Burst_Start the burst sequence is restarted with the first burst followed by the second burst etc., as described above.

Continuous mode is equivalent to burst mode, with only one burst spanning the whole SFN cycle of 4096 radio frames, this burst starting in the radio frame with SFN = 0.

Assume that IP_Position(*x*) is the position of idle period number *x* within a burst, where *x* = 1, 2, …, and IP_Position(*x*) is measured in number of CPICH symbols from the start of the first radio frame of the burst.

The positions of the idle periods within each burst are then given by the following equation:

IP_Position(*x*) = (*x* ? IP_Spacing ? 150) + (rand(*x* modulo 64) modulo (150 – IP_Length)) + IP_Offset;

where rand(*n*) is a pseudo random generator defined as follows:

rand(0) = Seed;

rand(*n*) = (106? rand(*n* – 1) + 1283) modulo 6075, *n* = 1, 2, 3, ….

Note that *x* is reset to *x* = 1 for the first idle period in every burst.

Figure 6 below illustrates the idle periods for the burst mode case.

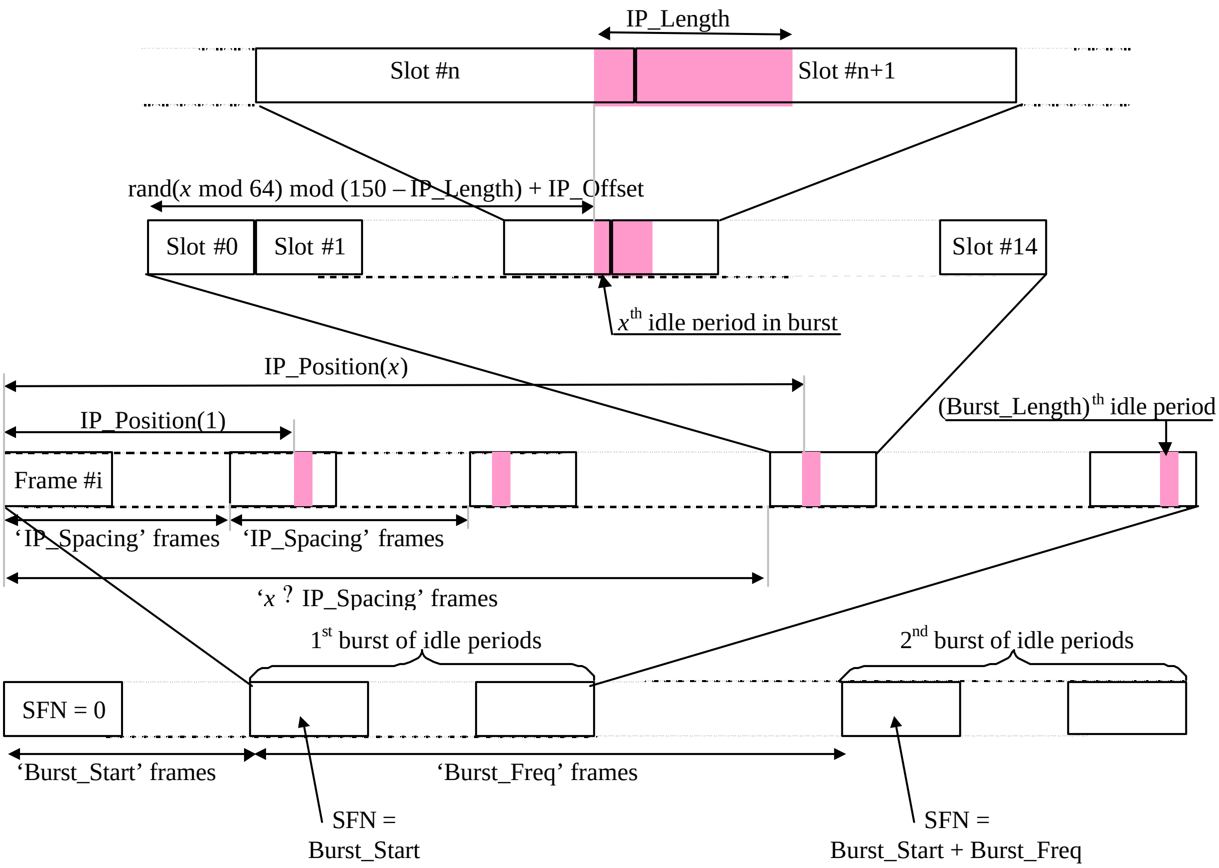

Figure 6: Idle Period placement in the case of burst mode operation

9 Gated DPCCH Transmission

9.1 General

Gated DPCCH transmission (hereafter, called gating except for the section title) is basically reduced power control rate operation to get power saving and interference reduction by turning off transmission intermittently. Gating can be applied when UTRAN and UE support gating, DSCH and associated DPCH in downlink and DPCH in uplink are set-up between UTRAN and UE, but there is no data to transmit on both uplink and downlink for a while.

UTRAN determines whether gating is initiated or terminated. Gating is initiated and terminated by higher layer signalling. If a new radio link is set up during gating and the Node B of the newly added radio link does not support gating, then the gating shall be terminated.

There are two kinds of period in gating depending on the transmission of data on DPDCH during gating. In Basic Gating Period, both DPCCH and DPDCH will contain transmitted bits only in certain slots of the frame. DPDCH is sent in the slots, where DPCCH is also transmitted, due to the fact that CRC is attached to zero length transport block to facilitate adequate performance for outer loop power control. If there is no CRC transmitted, i.e., only DPCCH is transmitted, then the outer loop power control target is considered frozen with basic DPCCH only gating. This period is described in section 9.3.1. However, even during gating, non-zero length transport block can be transmitted on DPDCH without terminating the gating exceptionally for the data with restricted TFCS. This Embedded Data Period is described in section 9.3.2.

In addition, the network signals to the UE the 'RX gating DRX cycle', which defines in which frames transmission of non-zero length transport block can start again in downlink during gating. The transmission of non-zero length transport block can start again in radio frame CFN, which fulfils both of the two following relations:

a) CFN mod (RX gating DRX cycle) = 0.

b) CFN mod Fi = 0, where Fi is the number of radio frames in one TTI of the TrCHi carrying a non-zero length transport block [TS25.212].

If 'RX gating DRX cycle' >1, it is known beforehand that UTRAN is not transmitting neither DPDCH or DPCCH for the UE in certain slots in the frame that does not fulfil the above condition. Hence, it is possible to achieve battery saving also from the UE RX side by turning off the receiver during those slots

9.2 Related Parameters

When the call is set up, UTRAN and UE negotiate the gating capability and parameters. The parameters controlling the gating operation are as follows:

Table T1. Gating Parameters

Gating Rate	1	1/3	1/5
Gating Mode	Downlink Only	Uplink and Downlink	
TFCS restrictions in downlink	Given by higher layer signalling		
TFCS restrictions in uplink	Given by higher layer signalling		
RX gating DRX cycle	1	2	4

Gating rate is the ratio of the number of turn-on time slots to the number of time slots in frames. For example, gating rate of 1/3 means that 5 slots are transmitted during a frame interval of 15 slots. Gating mode indicates that gating is applied to downlink only or to both uplink and downlink.

9.3 Operation in Gated DPCCH Transmission

This section describes in detail gated DPCCH transmission scheme. The transmitter operation during basic gating period and embedded data period is explained in sections 9.3.1 and 9.3.2, respectively. In Annex X, Figures X.1 and X.2 show the conceptual diagrams of "uplink and downlink gating" and "downlink only gating", respectively.

9.3.1 Basic Gating Period

9.3.1.1 Uplink and Downlink Gating

In Basic Gating Period in uplink, the DPCCH is transmitted intermittently together with DPDCH consisting of encoded CRC bits if CRC is attached to zero length transport block. UE shall turn its transmitter on only for the time slots specified in Table T4 and turn its transmitter off in all other time slots.

In Basic Gating Period in downlink, UTRAN shall turn on the transmission of TPC and PILOT fields only for the time slots specified in Table T2. And, UTRAN also shall turn on the transmission of DPDCH consisting of encoded CRC bits, if CRC is attached to zero length transport block, only for the time slots in which TPC is transmitted.

In Basic Gating Period in downlink, transmission of TFCI in downlink will depend on the CFN and 'RX gating DRX cycle' value. UTRAN shall turn on the transmission of TFCI

- in all the time slots in the radio frames where CFN mod (RX gating DRX cycle) = 0.
- in only those time slots specified in Table T2 in the radio frames where CFN mod (RX gating DRX cycle) ? 0.

UTRAN shall turn off the transmission in the remaining part.

9.3.1.2 Downlink Only Gating

In Basic Gating Period in downlink only gating, UE shall always turn on its transmitter and transmit all the DPCCH fields (PILOT, TFCI, TPC, FBI) together with DPDCH consisting of encoded CRC bits if CRC is attached to zero length transport block. However, because TPC field in uplink can be updated only for the associated downlink turn-on time slot, downlink power control rate is lower than non-gating operation. Similarly, uplink power control rate is also lower than non-gating operation.

In Basic Gating Period, UTRAN shall turn on the transmission of TPC and PILOT only for the time slots specified in Table T2. And, UTRAN also shall turn on the transmission of DPDCH consisting of encoded CRC bits, if CRC is attached to zero length transport block, only for the time slots in which TPC is transmitted.

In Basic Gating Period, transmission of TFCI in downlink will depend on the CFN and 'RX gating DRX cycle' value. UTRAN shall turn on the transmission of TFCI

- in all the time slots in the radio frames where CFN mod (RX gating DRX cycle) = 0.
- in only those time slots specified in Table T2 in the radio frames where CFN mod (RX gating DRX cycle) ? 0.

UTRAN shall turn off the transmission in the remaining part.

9.3.2 Embedded Data Period

In Embedded Data Period, non-zero length transport block can be transmitted on DPDCH for the data with restricted TFCS.

TTI of TrCH carrying data transmitted during Embedded Data Period in downlink may only start in a radio frame where CFN is fulfilling both of two following relations:

- CFN mod (RX gating DRX cycle) = 0, and

- CFN mod Fi = 0 , where Fi is the number of radio frames in one TTI of the TrCHi carrying the data [TS25.212].

In Embedded Data Period in downlink, UTRAN transmits non-zero length transport block as well as DPCCH. In Embedded Data Period in downlink, UTRAN shall turn its transmission on in all the time slots and transmit all the DPCCH fields (PILOT, TFCI, TPC) as specified in Table T3, but TPC shall be updated only for the time slots specified in Table T2.

In Embedded Data Period in uplink, UE transmits non-zero length transport block as well as DPCCH. In Embedded data period in uplink, UE shall turn its transmitter on in all the time slots and transmit all the DPCCH fields (PILOT, TFCI, TPC, FBI) as specified in Table T5, but TPC shall be updated only at the time slot specified in Table T4.

9.4 Detection of DPDCH Frame during Gating

During gating, data with restricted TFCS can be transmitted in uplink or downlink DPDCH frame, but receiver should detect the transmission of non-zero length transport block because the receiver does not know when the transmission exists. UE can determine the existence of downlink transmission of non-zero length transport block by decoding downlink TFCI in the frames defined by RX gating DRX cycle because downlink TFCI field is always transmitted in the frames defined by RX gating DRX cycle length coefficient. In uplink, UTRAN shall not use TFCI to detect the uplink DPDCH frame, since part of uplink TFCI in a frame may not be transmitted. Since pilot bits are transmitted over the whole frame in which complete TFCI is transmitted, one possible solution for the frame detection in UTRAN is the pilot energy comparison. Pilot energy in the uplink time slots that do not contain pilot during gating is compared to pilot energy in those slots that contain pilot during gating. If this is above threshold, then UTRAN decodes the uplink TFCI and uplink DPDCH frame.

9.5 DPCCH Switch-On Time Slot

9.5.1 Downlink DPCCH Switch-On Time Slot

Table T2 and Table T3 show in which time slots UTRAN shall turn on the DPCCH fields in downlink in basic gating period and in embedded data period, respectively. Furthermore, DPDCH carrying encoded CRC bits is mapped to those slots where TPC bits are transmitted if CRC is attached to zero length transport block.

In the table, the CFN of the radio frame is denoted by i, and the range of the gating group number j defined in subclause 9.5.3 is j = 0, 1, 2, 3, 4 for gating rate 1/3, and j = 0, 1, 2 for gating rate 1/5. The function $s(i,j)$ used for the reference pattern is defined in subclause 9.5.3.

Table T2. Switched-on Time Slots for downlink DPCCH in basic gating period.

CFN	Gating Rate	Switched-on Time Slots for downlink DPCCH fields		
		Pilot	TPC	TFCI
CFN mod (RX gating DRX cycle) = 0	1	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)
	1/3	*j* ? 3 + *s*(*i*,*j*) – 1	*j* ? 3 + *s*(*i*,*j*)	All slots (0, 1, …, 14)
	1/5	*j* ? 5 + *s*(*i*,*j*) – 1	*j* ? 5 + *s*(*i*,*j*)	All slots (0, 1, …, 14)
CFN mod (RX gating DRX cycle) ? 0	1	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)
	1/3	*j* ? 3 + *s*(*i*,*j*) – 1	*j* ? 3 + *s*(*i*,*j*)	*j* ? 3 + *s*(*i*,*j*)
	1/5	*j* ? 5 + *s*(*i*,*j*) – 1	*j* ? 5 + *s*(*i*,*j*)	*j* ? 5 + *s*(*i*,*j*)

Table T3. Switched-on Time Slots for downlink DPCCH in embedded data period.

Gating Rate	Switched-on Time Slots for downlink DPCCH fields		
	Pilot	TPC	TFCI
1	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)
1/3	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)
1/5	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)	All slots (0, 1, …, 14)

9.5.2 Uplink DPCCH Switch-On Time Slot

Table T4 and Table T5 show in which time slots UE shall turn on the transmission of DPCCH fields in basic gating period and in embedded data period, respectively. In addition, DPDCH carrying encoded CRC bits is mapped to those slots, where DPCCH is also transmitted if CRC is attached to zero length transport block.

Table T4. Switched-on Time Slots for uplink DPCCH in basic gating period.

Gating Rate	Switched-on Time Slots for uplink DPCCH fields Pilot, TFCI, FBI, TPC
1	All slots (0, 1, …, 14)
1/3	*j* ? 3 + *s*(*i*,*j*)
1/5	*j* ? 5 + *s*(*i*,*j*)

Table T5. Switched-on Time Slots for uplink DPCCH in embedded data period.

Gating Rate	Switched-on Time Slots for uplink DPCCH fields Pilot, TFCI, FBI, TPC
1	All slots (0, 1, …, 14)
1/3	All slots (0, 1, …, 14)
1/5	All slots (0, 1, …, 14)

9.5.3 Reference Pattern

15 slots of the radio frame are divided into *N* gating groups, each group consists of *S* consecutive slots. For gating rate 1/3, *N* = 5 and *S* = 3, and for gating rate 1/5, *N* = 3 and *S* = 5. Denote the CFN of the current radio frame by *i*, *i* = 0, 1, 2, …, 255. Further define the 19 bit sequence $(a_{18}, a_{17}, \ldots, a_0)$ = (1, 0, 0, 1, 0, 1, 1, 1, 0, 1, 1, 0, 0, 1, 0, 1, 1, 0, 1).

Table T6. Summary of Reference Pattern *s(i, j)*

Parameter	Value	
CFN	0, 1, …, 255 (8bits)	
$a_{18}, a_{17}, \ldots, a_0$	1, 0, 0, 1, 0, 1, 1, 1, 0, 1, 1, 0, 0, 1, 0, 1, 1, 0, 1	
gating rate	1/3	1/5
Number of gating group (*N*)	5	3
Gating group size (*S*)	3	5

For CFN *i*, *i* = 0, 1, 2, …, 255, concatenated CFN $C_i = i \times 256 + i$, and gating group *j*, the function *s*(*i*, *j*) is defined as

$$s(i,j) = \begin{cases} (A_j \oplus C_i)_{10} \bmod (S-1) + 1, & j = 0 \\ (A_j \oplus C_i)_{10} \bmod S, & j = 1,\ldots,N-2 \\ S-1, & j = N-1 \end{cases}, \quad i = 0,1,\ldots,255$$

where $(X)_{10}$ represents the decimal representation of the number *X*, and $X \oplus Y$ denotes bit-wise modulo 2 addition of the binary representation of the numbers *X* and *Y*. And $A_j = \sum_{k=j}^{j+15} 2^{k-j} a_k$, *j*=0,1,...,*N*-2.

Annex X (Informative): Conceptual illustration of gated DPCCH transmission

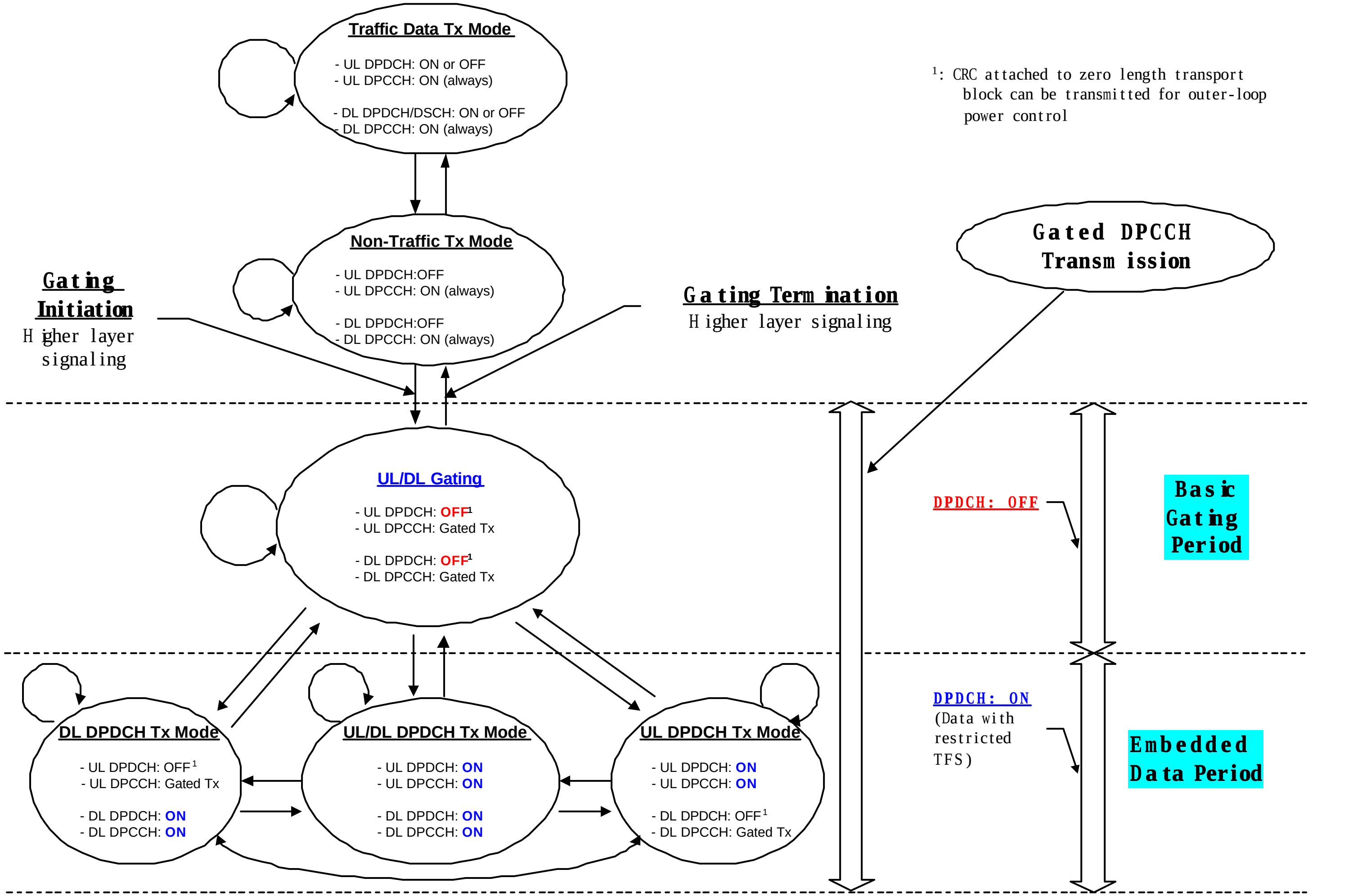

Figure X.1: Conceptual Transition Diagram of Gating: Uplink and Downlink Gating

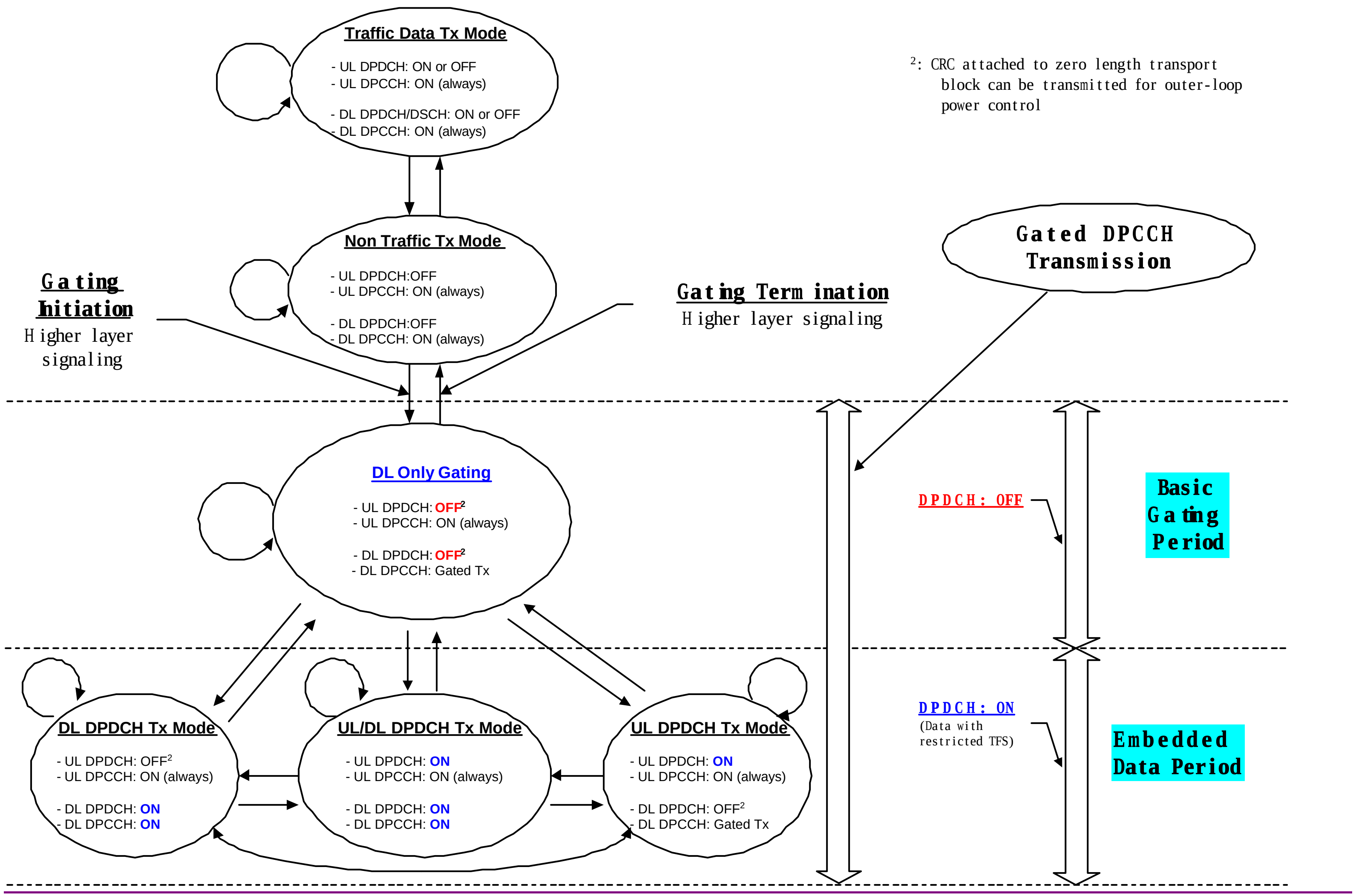

Figure X.2: Conceptual Transition Diagram of Gating: Downlink Only Gating