CR-Form-v3

CHANGE REQUEST

✎   **25.211 CR 094**   ✎ rev **-** ✎ Current version: **3.5.0** ✎

*For **HELP** on using this form, see bottom of this page or look at the pop-up text over the ✎ symbols.*

Proposed change affects: ✎   (U)SIM ☐   ME/UE **X**   Radio Access Network **X**   Core Network ☐

Title: ✎	Clarification on PICH and S-CCPCH timing relation
Source: ✎	CWTS/Huawei
Work item code: ✎	**Date:** ✎
Category: ✎ **F**	**Release:** ✎ R99,REL-4

Use <u>one</u> of the following categories:
F (essential correction)
A (corresponds to a correction in an earlier release)
B (Addition of feature),
C (Functional modification of feature)
D (Editorial modification)
Detailed explanations of the above categories can be found in 3GPP TR 21.900.

Use <u>one</u> of the following releases:
2   (GSM Phase 2)
R96   (Release 1996)
R97   (Release 1997)
R98   (Release 1998)
R99   (Release 1999)
REL-4 (Release 4)
REL-5 (Release 5)

Reason for change: ✎	The figure used for PICH and S-CCPCH timing relation does not show their correct timing relation.
Summary of change: ✎	Timing relation between PICH and S-CCPCH shown in Fig29 has been changed.
Consequences if not approved: ✎	Timing relation will be imperfect.

Clauses affected: ✎	7.1
Other specs affected: ✎	☐ Other core specifications ✎
	☐ Test specifications
	☐ O&M Specifications
Other comments: ✎	

7.1 General

The P-CCPCH, on which the cell SFN is transmitted, is used as timing reference for all the physical channels, directly for downlink and indirectly for uplink.

Figure 29 below describes the frame timing of the downlink physical channels. For the AICH the access slot timing is included. Transmission timing for uplink physical channels is given by the received timing of downlink physical channels, as described in the following subclauses.
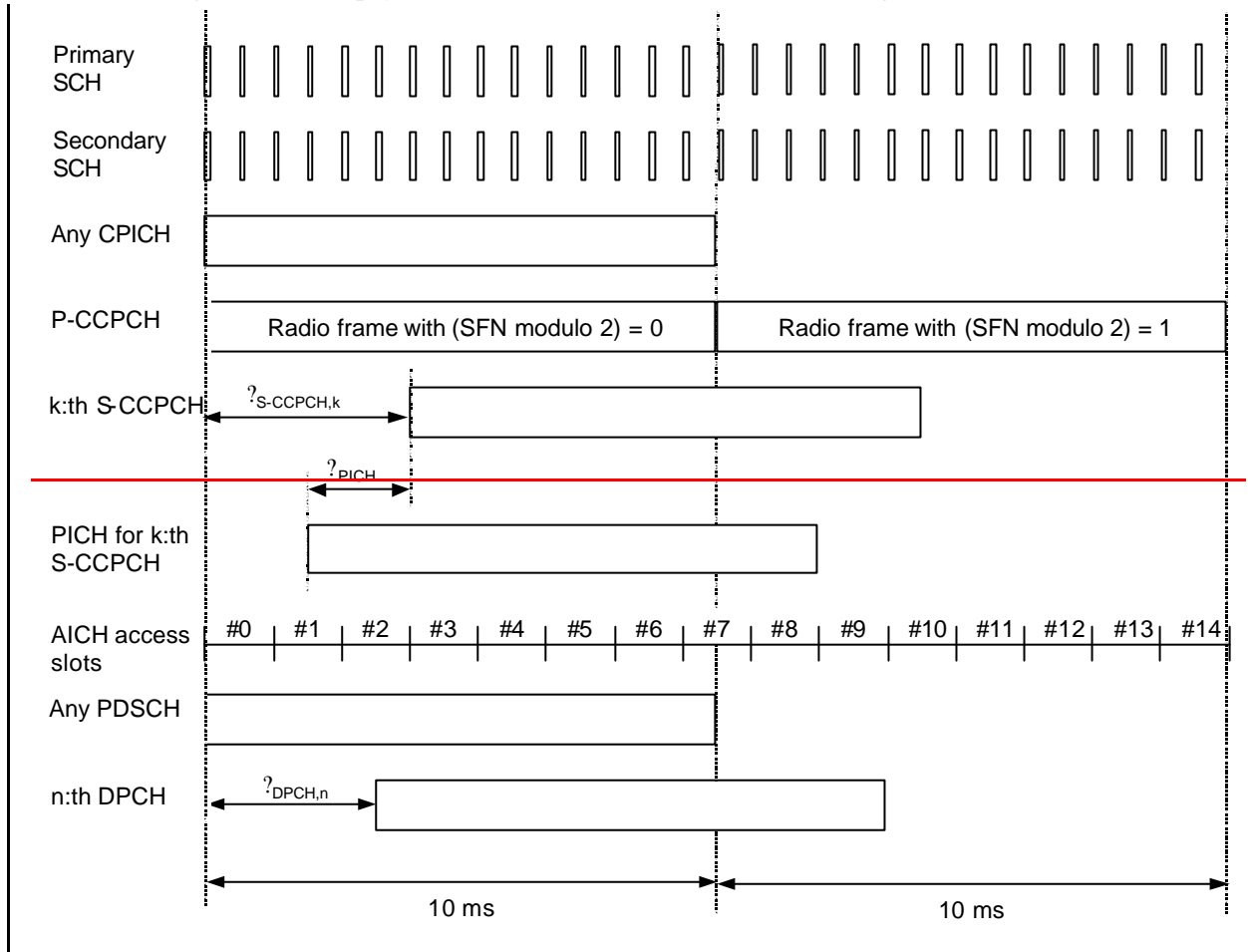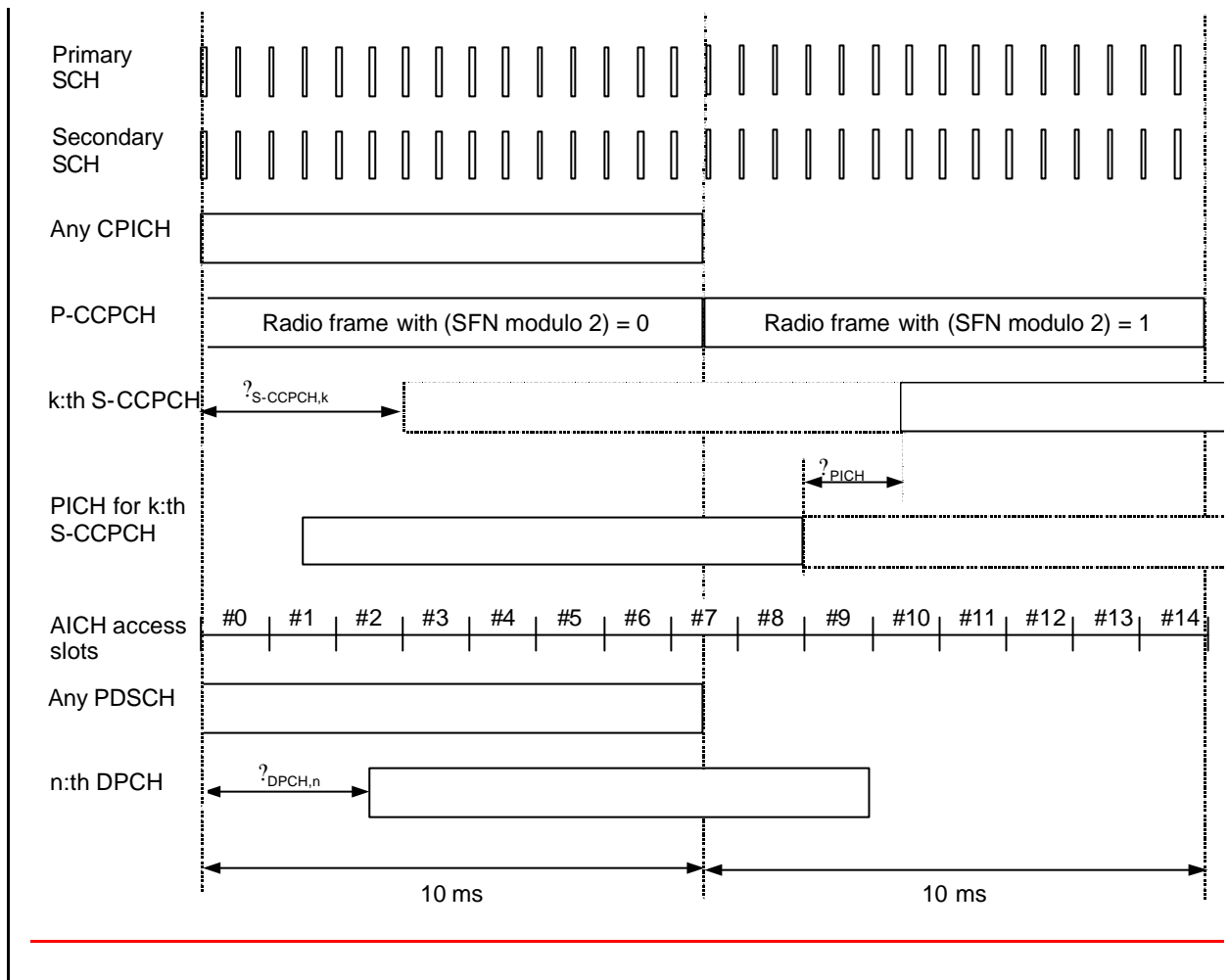
Figure 29: Radio frame timing and access slot timing of downlink physical channels

The following applies:

-? SCH (primary and secondary), CPICH (primary and secondary), P-CCPCH, and PDSCH have identical frame timings.

- The S-CCPCH timing may be different for different S-CCPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{\text{S-CCPCH,k}} = T_k \cdot 256$ chip, $T_k \in \{0, 1, \dots, 149\}$.

-? The PICH timing is $\tau_{\text{PICH}} = 7680$ chips prior to its corresponding S-CCPCH frame timing, i.e. the timing of the S-CCPCH carrying the PCH transport channel with the corresponding paging information, see also subclause 7.2.

- AICH access slots #0 starts the same time as P-CCPCH frames with (SFN modulo 2) = 0. The AICH/PRACH and AICH/PCPCH timing is described in subclauses 7.3 and 7.4 respectively.

- The relative timing of associated PDSCH and DPCH is described in subclause 7.5.

-? The DPCH timing may be different for different DPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{\text{DPCH,n}} = T_n \cdot 256$ chip, $T_n \in \{0, 1, \dots, 149\}$. The DPCH (DPCCH/DPDCH) timing relation with uplink DPCCH/DPDCHs is described in subclause 7.6.