TSG-RAN Working Group 1 meeting #19 ***TSGR1 (01) 0214***

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Agenda Item: AH21
Source: CWTS/CATT
To: TSG RAN WG1
Title: Monitoring GSM from 1.28Mcps TDD under high data rate traffic
Document for: Approval

1. Summary

'Monitoring GSM from 1.28Mcps TDD under low data rate traffic using 1 uplink and 1 downlink time slot' has been described in 1.28Mcps TDD Working CR for TS25.225. When more than 1 uplink and/or 1 downlink TDD timeslot are used for high data rate traffic in 1.28Mcps TDD, UE can still use the remained idle time slots to track the FCCH burst of GSM cells. The following section gives the calculation result of FCCH detection time of a single synthesizer UE under high data rate traffic.

2. Proposal

We propose to include the following paragraphs in the working CR for the TS25.225 section Annex A.2.1 High data rate traffic using more than 1 uplink and/or 1 downlink TDD time slot (for 1.28Mcps TDD).

---------- Changes to working cr of 25.225 begin ----------

A.2.1 Higher data rate traffic using more than 1 uplink and/or 1 downlink TDD timeslot (for 1.28Mcps TDD)

The minimum idle time to detect a complete FCCH burst for all possible alignments between the GSM and the 1.28Mcps TDD frame structure (called 'guaranteed FCCH detection'), assuming that monitoring happens every sub-frame, can be calculated as follows (t_{FCCH} = one GSM slot):

$$t_{\min,\ guaranteed} = 2 \cdot t_{synth} + t_{FCCH} + \frac{5\,\text{ms}}{13} = 2 \cdot t_{synth} + \frac{25\,\text{ms}}{26}$$

- (e.g for t_{synth} =0ms: 2 1.28Mcps TDD **consecutive** idle timeslots needed, for t_{synth} =0.3ms: 3 slots (or 2 slots and the DwPTS+GP+UpPTS), for t_{synth} =0.5ms: 3 slots, for t_{synth} =0.8ms: 4 slots). Under this conditions the FCCH detection time can never exceed the time of 660ms.

- (For a more general consideration t_{synth} may be considered as a sum of all delays before starting monitoring is possible).

- For detecting SCH instead of FCCH (for a parallel search) the same equation applies.

- In the equation before the dual synthesiser UE is included if the synthesiser switching time is 0ms.

Table : FCCH detection time for a single synthesizer UE monitoring GSM from 1.28Mcps TDD every sub-frame

Occupied Slots	Cases	**AVERAGE** FCCH detection time in ms	**MAXIMUM** FCCH detection time in ms
2	21	136.625	660.785
3	35	188.451	660.785
4	35	231.115	660.785
5	21	-	-
6	7	-	-
7	1	-	-

The result in the above table is based on the following assumption:

- A single synthesizer is used.
- A [0.5] ms period is supposed to be required to perform a frequency jump from 1.28Mcps TDD to GSM and vice versa.
- For a given number of occupied slots in the TDD mode all possible cases of distributions of these occupied TDD slots are considered (see 'cases'). For every case arbitrary alignments of the TDD and the GSM frame structure are taken into account for calculating the average FCCH detection time (only these cases are used which guarantee FCCH detection for all alignments; only the non-parallel FCCH search is reflected by the detection times in the above table).

The term 'occupied slots' means that the UE is not able to monitor in these TDD slots.

For a synthesiser switching time of one or one half TDD timeslot the number of needed consecutive idle TDD timeslots is summarized in the table below:

Table : Link between the synthesiser performance and the number of free consecutive Timeslots for guaranteed FCCH detection, needed for GSM monitoring

One-way switching time for the synthesiser	Number of free consecutive 1.28Mcps TDD timeslots needed in the sub-frame for a guaranteed FCCH detection
1 Timeslot (=864 chips)	4
0.5 Timeslot (=432 chips)	3
0 (dual synthesiser)	2

---------- Changes to working CR 25.225 end ----------