TSG-RAN Working Group 1 Meeting #19 **_TSGR1#19(01)0205_**

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Source:	**Panasonic**
Title:	**Clarification of simulation results of type-III HARQ bit mapping proposal**
Agenda Item:	**AH24 (HSDPA)**
Document for:	**Approval**

1. Introduction

This contribution follows up on a proposal of bit mapping method of type-III HARQ [1] and responds to a comment which pointed out that there is no difference between so-called symbol combining and conventional combining in QPSK case. The comment is described in Tdoc R1-01-0188[2], chapter 7.1.2 Reviewal of T-docs related HSDPA, pp.18, note (*28).
The simulation result of this contribution shows that there is no performance difference between proposed and conventional methods.

We conclude that we should use conventional mapping method for QPSK, because the proposed scheme achieves the same performance and requires the same size buffer as the conventional one.
We propose that we should use the proposal mapping method for 16QAM or higher-level modulation, which can reduce receiver's buffer size and achieve the same performance as the conventional method.

This clarification of this contribution has been expected to be discussed on e-mail reflector. After the approval of this clarification, we will make a Text Proposal for TR 25.848 and submit it before the next WG1 meeting.

2. Proposed method

- Node B maps systematic information and parity information on separated symbols

  Fig. 2 shows the packet format of the proposed HARQ. Systematic bits set S is sent in each retransmission and Parity bits set Podd and Peven are sent alternately in each packet. In this figure Podd and Peven are selected as different parity information for rate 1/2 turbo code. When rate 3/4 turbo code is used, four different types of parity information are generated and sent on each retransmission.

  One symbol for systematic bits includes systematic bits only. One symbol for parity bits includes parity bits only. No symbol includes systematic bits and parity bits simultaneously. With this procedure systematic bits and parity bits are mapped on symbols separately.

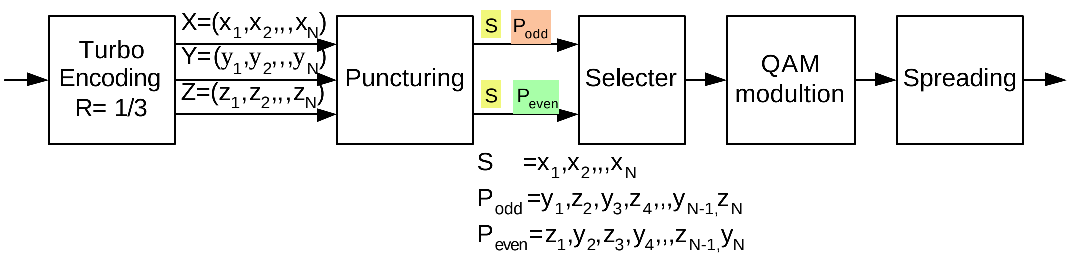


Fig. 1 Sender structure of proposed type-III HARQ mapping(R=1/2)

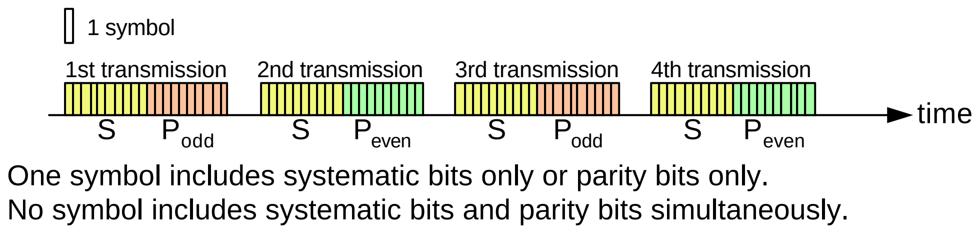


Fig. 2 Packet format of proposed type-III HARQ(R=1/2)

✍ Symbol combining of systematic information at UE can reduce the UE's buffer

Receiver combines every packet's systematic symbols before turbo decoding. Receiver also combines plural received Podd packet symbols and Peven packet symbols respectively before turbo decoding. Log-likelihood ratio (LLR) of each bit is calculated after the symbol combination. The buffer size for systematic information of the proposed scheme is only the size of one packet symbols. This can reduce the receiver's buffer size

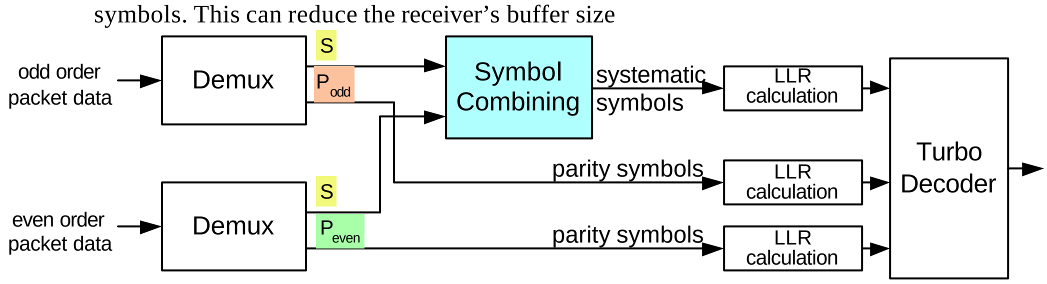


Fig. 3 Receiver structure of PROPOSED type-III HARQ(R=1/2)

3. Simulation results

✍ The proposed method can achieve the same performance as the conventional method

The simulation results are shown in Annex A and the simulation assumptions are shown in Annex B. The simulation results show that there is no performance difference between the proposed method and the conventional method. This can be explained by the consideration that the log likelihood calculation used in the proposed method doesn't have performance gain compared to the conventional log likelihood calculation.

Therefore there results show that **the proposal method can reduce the receiver's buffer size without any performance degradation with introducing type-III HARQ**.

4. Conclusion

The simulation result of this contribution showed that there is no performance difference between proposed and conventional methods.

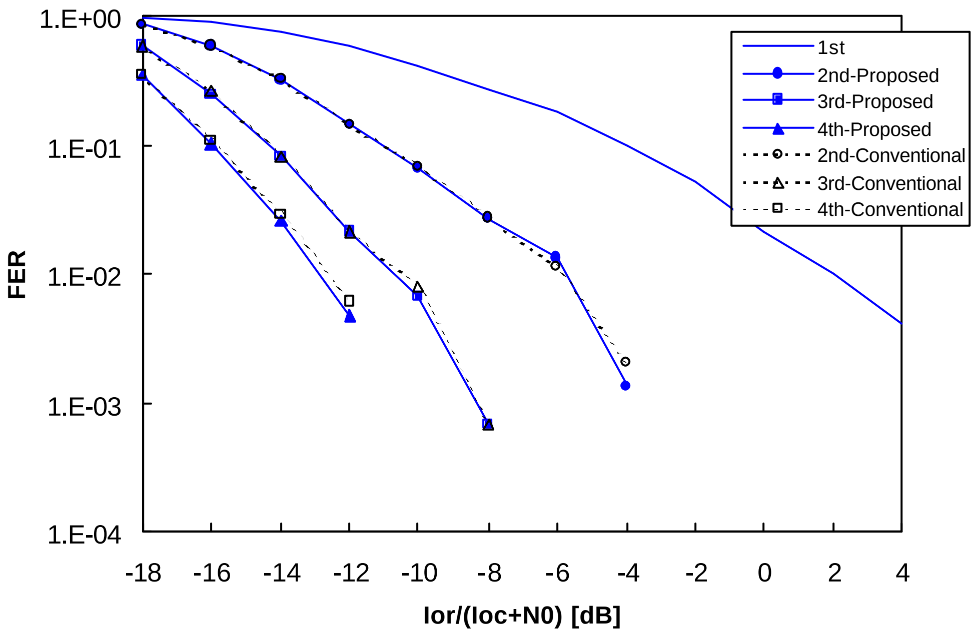
We conclude that we should use conventional mapping method for QPSK, because the proposed scheme achieves the same performance and requires the same size buffer as the conventional one.

We propose the usage of proposal mapping method for 16QAM or higher-level modulation, which can reduce receiver's buffer size and achieve the same performance as the conventional method.

This clarification of this contribution has been expected to be discussed on e-mail reflector. After the approval of this clarification, we will make a Text Proposal for TR 25.848 and submit it before the next WG1 meeting.

5. References

[1] R1-01-0031, Panasonic “Proposal of bit mapping for type-III HARQ” Boston, USA, January 15-18, 2001
[2] R1-01-0188, Secretary “Draft minutes of WG1 #18 meeting” Las Vegas, USA, Feburary27-March2, 2001
[3] R1-00-1093, Ericsson, Motorola and Nokia “Link Evaluation Methods for High Speed Downlink Packet Access (HSDPA)” Berlin, Germany, August 21-24, 2000.



Annex A. Simulation results

Fig. 4 Frame error rate QPSK R=1/2 1 -path Rayleigh fading channel

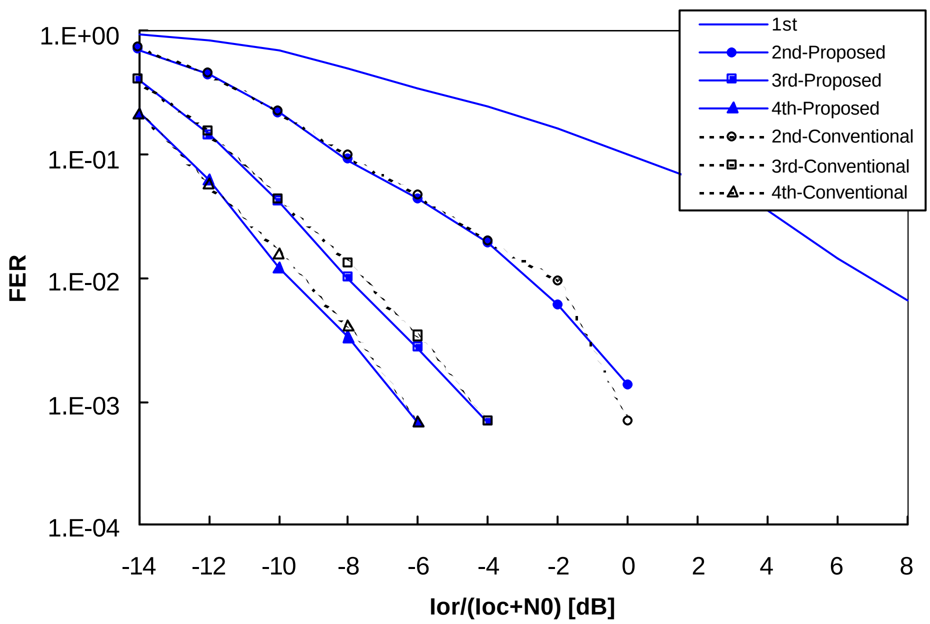


Fig. 5 Frame error rate QPSK R=3/4 1 -path Rayleigh fading channel

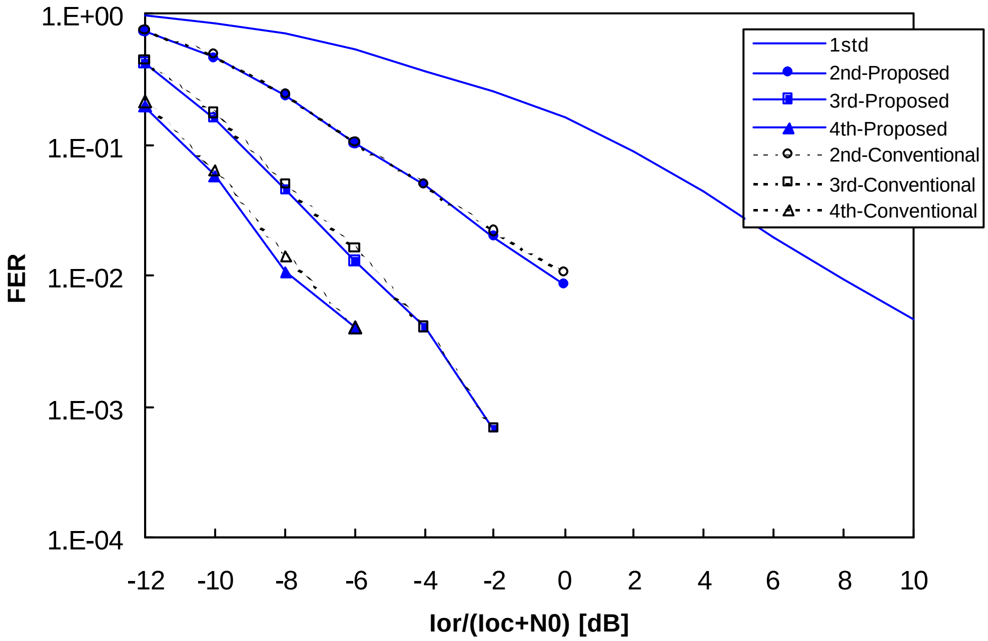


Fig. 6 Frame error rate 16QAM R=1/2 1-path Rayleigh fading channel

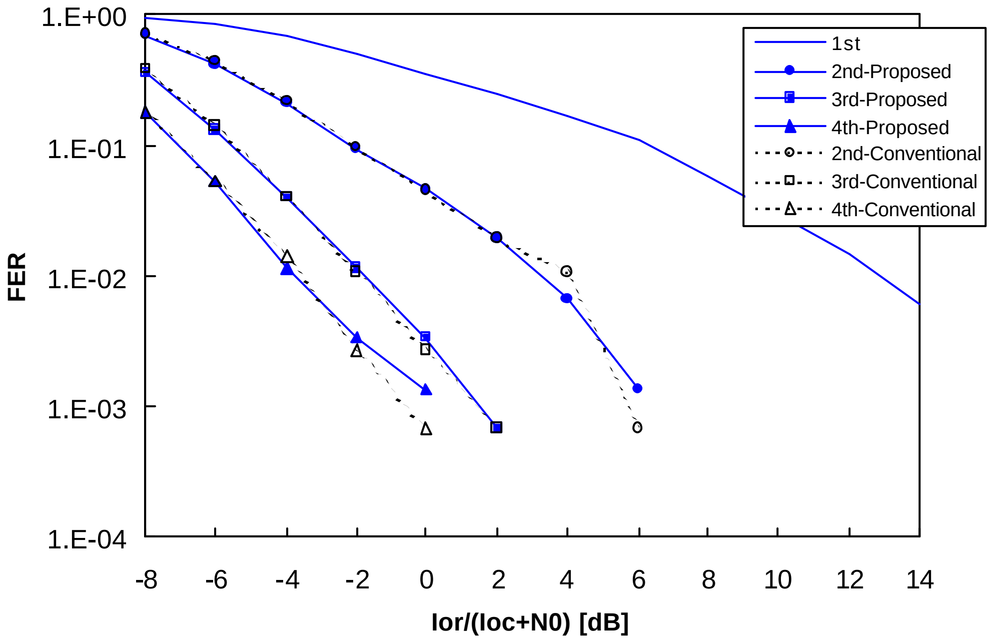


Fig. 7 Frame error rate 16QAM R=3/4 1-path Rayleigh fading channel

Annex B. Detailed simulation assumptions

These simulation assumptions are same as common assumptions. [3]

Table. 1

Parameter	Value	Comment
Chip-rate	3.84Mcps	
Spreading Factor Number of code for HS-DSCH	32 1	
TPC	Off	
CPICH Ec/Ior	-10dB(10% of Ior)	
DSCH Ec/Ior	-1dB (80% of Ior)	
Channel Model	1-path Rayleigh fd = 56.6Hz	
Channel Estimation	Ideal	
HSDPA Frame Length	3.33ms(5 slots)	transmission unit interval.
Number of CRC bits	16	
Tail bits	6	in each transmission unit.
Max Number of Iterations for Turbo Decoding	8	
Metric for Turbo Code	Max	
HARQ structure	Dual Stop and Wait	
Number of maximum retransmission	10	
STTD	Off	
Channel Interleaver	Bit interleaver and Symbol interleaver	
Code Rate	1/2,3/4	in each transmission unit. Generated from rate 1/3 Turbo Code.