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Title: **Text proposal on HARQ complexity to TR25.848, Rev. 1**

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7.2 Hybrid ARQ (H-ARQ)

7.2.1 Performance evaluation <throughput, delay>

7.2.2 Complexity evaluation <UE and RNS impacts>

7.2.2.1 N-channel stop-and-wait H-ARQ

7.2.2.1.1 Introduction

The complexity of H-ARQ mechanisms when employed for link adaptation in HSDPA transmission depends on the H-ARQ scheme selected as well as on where the retransmission functionality is located in the UTRAN. Dual-channel stop-and-wait (SAW) protocol has been proposed as the retransmission functionality for HDSPA. A complexity evaluation on SAW H-ARQ is presented in this section. In this complexity evaluation it is further assumed that H-ARQ retransmission protocol operates in Node B.

7.2.2.1.2 UE buffering complexity

The principle of hybrid ARQ is to buffer HSDPA TTIs that were not received correctly and consequently combine the buffered data with retransmissions. The actual method of doing soft combining depends on the H-ARQ combining scheme selected. In Chase combining scheme the receiver always comb ines the full retransmission of the failed HSDPA TTI, i.e. the amount of data in the receiver buffer remains the same. In the incremental redundancy schemes the receiver buffers coded symbols, which introduce new information to the HSDPA TTI transmitted first, i.e. the amount of data to be buffered increases with consecutive retransmissions. However, probably in practice the buffer in the receiver needs to be dimensioned considering the maximum size of the HSDPA TTI after all the incremental redundancy has been introduced. Regardless of the H-ARQ combining scheme soft combining is done on L1 before the decoding stage of FEC. Prior to decoding these symbols are soft-valued, i.e. each symbol is represented by two or more bits.

Regardless of the location of retransmission functionality in the RNS the number of symbols to be buffered in L1 receiver can be estimated generally as follows:

$$buffer = coded\ bits_{PDU} \times failed\ PDUs\ in\ TTI \times (latency_{retransmit} + latency_{NACK})$$

where it is assumed for the sake of clarity that an integer number of PDUs fit into one HSDPA TTI. The latencies are also considered as multiples of a HSDPA TTI. For dual channel stop-and-wait H-ARQ the buffer size estimation is considerably simplified since no new PDUs are transmitted on a subchannel before the previous packet is acknowledged. The receiver has to buffer one HSDPA TTI from both subchannels. The next transmission is either a new packet or a retransmission of an erroneous packet. In either case, the maximum buffering need is two HSDPA TTIs. The actual size of the buffer needed for each HSDPA TTI depends on the H-ARQ combining scheme as described above. The receiver buffering complexity estimate can be easily extended to *n*-channel stop-and-wait protocol, where at maximum *n* HSDPA TTIs would be buffered at any given time. Thus, for *n*-channel stop-and-wait ARQ the L1 buffering can be expressed as:

$buffer\ ?\ ?coded\ bits_{TTI}\ ?\ n?$

However, it must be noted that the size of HSDPA TTI may change when the number of subchannels changes, i.e. TTI length for n-channel SAW HARQ can be shorter than one for dual channel SAW HARQ. Average receiver buffer sizes for dual channel HARQ for some bit rates are depicted in Figure 1.

Naturally, the number of subchannels in stop-and-wait ARQ is reflected in the amount of acknowledgment signaling needed to be sent to the transmitter. The complexity impact on RNS is mainly concentrated on Node B where the H-ARQ retransmission resides according to the current proposal. However, packet buffering is not as much an issue in Node B hardware.

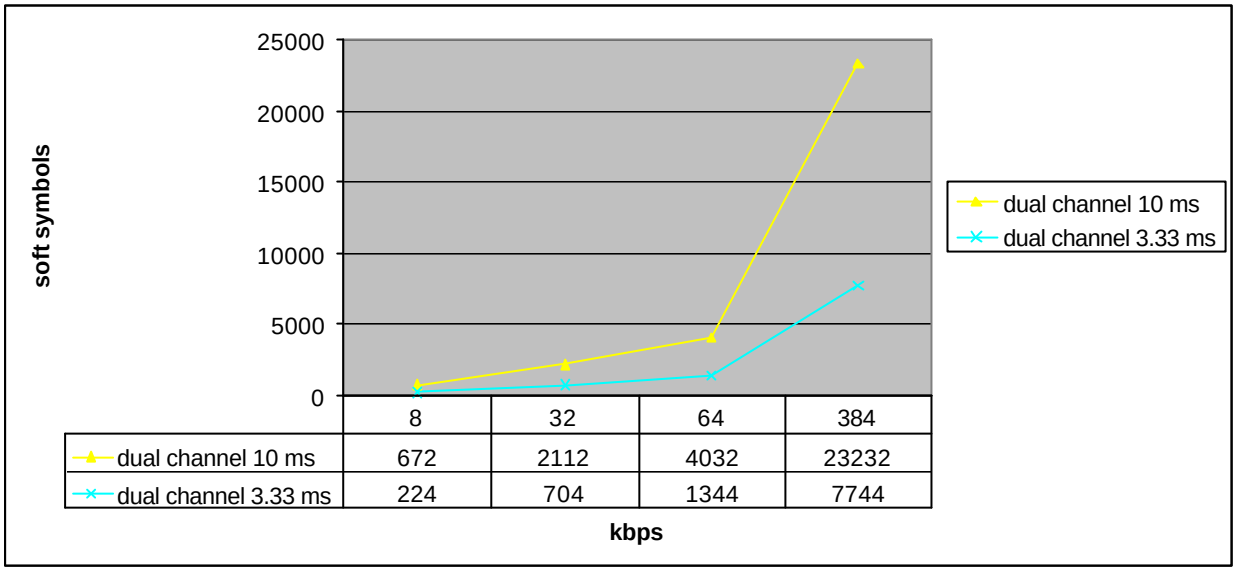

Figure 1. Receiver L1 buffer size for dual channel SAW HARQ

As an example, tables 1-12 show maximum estimated receiver buffer sizes for 4-channel SAW HARQ. Chase combining, i.e. retransmission of a complete HSDPA TTI (one CRC per TTI, included in the bit rate) and SF = 16 or SF = 32 are assumed. In Tables 1-6 retransmitted TTIs are combined at modulation symbol level. It can be seen that the memory size does not increase with modulation since there are only two values to be buffered: I and Q.

Table 1. Buffer at soft combining stage for 1 code channel, HSDPA TTI = 3 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 2.0 ms frame, modulation symbols (I,Q pairs) buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM
16, 1 code channel or 32, 2 code channels	3.8 (max 480 kbps)	3.8 (max 720 kbps)	3.8 (max 960 kbps)	3.8 (max 1.44 Mbps)

Table 2. Buffer at soft combining stage for 10 code channels, HSDPA TTI = 3 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 2.0 ms frame, modulation symbols (I,Q pairs) buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channels or 32, 20 code channels	38.4 (max 4.8 Mbps)	38.4 (max 7.2 Mbps)	38.4 (max 9.6 Mbps)	38.4 (max 14.4 Mbps)

Table 3. Buffer at soft combining stage for 1 code channel, HSDPA TTI = 5 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 3.33 ms frame, modulation symbols (I,Q pairs) buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM

16, 1 code channel or 32, 2 code channels	6.4 (max 480 kbps)	6.4 (max 720 kbps)	6.4 (max 960 kbps)	6.4 (max 1.44 Mbps)

Table 4. Buffer at soft combining stage for 10 code channels, HSDPA TTI = 5 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 3.33 ms frame, modulation symbols (I,Q pairs) buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channels or 32, 20 code channels	64 (max 4.8 Mbps)	64 (max 7.2 Mbps)	64 (max 9.6 Mbps)	64 (max 14.4 Mbps)

Table 5. Buffer at soft combining stage for 1 code channel, HSDPA TTI = 15 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 10.0 ms frame, modulation symbols (I,Q pairs) buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM
16, 1 code channel or 32, 2 code channels	19.2 (max 480 kbps)	19.2 (max 720 kbps)	19.2 (max 960 kbps)	19.2 (max 1.44 Mbps)

Table 6. Buffer at soft combining stage for 10 code channels, HSDPA TTI = 15 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 10.0 ms frame, modulation symbols (I,Q pairs) buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channels or 32, 20 code channels	192 (max 4.8 Mbps)	192 (max 7.2 Mbps)	192 (max 9.6 Mbps)	192 (max 14.4 Mbps)

Tables 7-12 show the memory size at the input of the turbo decoder, i.e. demodulated baseband symbols. These values express the required memory should buffering be done on demodulated symbols. The memory size for QPSK is the same as for modulation symbol level combining (there is one symbol in I branch and one in Q branch). However, for higher modulation alphabets the memory size becomes clearly bigger. Note that these values are valid for Chase combining. For incremental redundancy HARQ more memory is required (if N different redundancy versions of similar size are transmitted the memory estimates have to be multiplied by N).

Table 7. Memory at the input of turbo decoder for 1 code channel, HSDPA TTI = 3 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 2.0 ms frame, baseband symbols buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM
16, 1 code channel or 32, 2 code channels	3.8 (max 480 kbps)	5.8 (max 720 kbps)	7.7 (max 960 kbps)	11.5 (max 1.44 Mbps)

Table 8. Memory at the input of turbo decoder for 10 code channels, HSDPA TTI = 3 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 2.0 ms frame, baseband symbols buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channels or 32, 20 code channels	38.4 (max 4.8 Mbps)	57.6 (max 7.2 Mbps)	76.8 (max 9.6 Mbps)	115 (max 14.4 Mbps)

Table 9. Memory at the input of turbo decoder for 1 code channel, HSDPA TTI = 5 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 3.33 ms frame, baseband symbols buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM

16, 1 code channel or 32, 2 code channels	6.4 (max 480 kbps)	9.6 (max 720 kbps)	12.8 (max 960 kbps)	19.2 (max 1.44 Mbps)

Table 10. Memory at the input of turbo decoder for 10 code channels, HSDPA TTI = 5 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 3.33 ms frame, baseband symbols buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channel or 32, 20 code channels	64 (max 4.8 Mbps)	96 (max 7.2 Mbps)	128 (max 9.6 Mbps)	192 (max 14.4 Mbps)

Table 11. Memory at the input of turbo decoder for 1 code channel, HSDPA TTI = 15 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 10.0 ms frame, baseband symbols buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM
16, 1 code channel or 32, 2 code channels	19.2 (max 480 kbps)	28.8 (max 720 kbps)	38.4 (max 960 kbps)	57.6 (max 1.44 Mbps)

Table 12. Memory at the input of turbo decoder for 10 code channels, HSDPA TTI = 15 slots

	Maximum buffer size for N-channel SAW HARQ, N=4, 10.0 ms frame, baseband symbols buffered (Ksymbols)			
SF	QPSK	8-PSK	16-QAM	64-QAM
16, 10 code channel or 32, 20 code channels	192 (max 4.8 Mbps)	288 (max 7.2 Mbps)	384 (max 9.6 Mbps)	576 (max 14.4 Mbps)

7.2.2.1.3 Encoding/decoding and rate matching complexity

In order to facilitate incremental redundancy it is likely that the FEC encoder rate has to be lowered, i.e. instead of a 1/3 rate encoder, a 1/5 or even lower rate encoder would be employed. For example, as proposed this far, by puncturing different symbols out of the output code word, different redundancy information is generated for soft combining. A mother code of lower rate does increase the complexity of both encoding and decoding stage. However, it is not necessary to add new constituent encoders to a turbo coder in order to lower the coding rate. More advanced methods that output more than one symbol per bit per branch could be utilized. Furthermore, investigations are needed to check whether the existing rate matching algorithm of Rel –99 can be used in conjunction with incremental redundancy or whether modification of either the rate matching or the encoder are necessary.

7.2.2.1.4 UE and RNS processing time considerations

Stop-and-wait HARQ introduces several tasks for UE and RNS to process in order to have the uplink and downlink transmissions consistent.

Node B processing tasks prior to sending data in the HS-DSCH

?? Decode the ACK/NACK transmitted in uplink
?? Make a scheduling decision on which UE is due to receive data among the UEs having data in the transmission buffer
?? Set TFCI and other information fields on downlink control channels

UE processing tasks

?? Decode TFCI, HSDPA TTI sequence info etc.
?? Despreading and demodulation
?? Soft combine retransmitted HSDPA TTI in the receiver buffer for the correct subchannel
?? Decode HSDPA TTI for the subchannel
?? Check CRC to decide whether the HSDPA TTI was received correctly
?? Generate ACK/NACK signaling for uplink

The time required for processing the tasks depends on the number of timeslots in the HSPDA TTI (number of bits to be processed). On the other hand, the time available for finishing the tasks also depends on these same

factors. Figures 2 and 3 show the general sequence of UE and RNS processing with two and four HARQ subchannels, respectively. In the figures T_{prop} depicts the propagation time, T_{UEP} the processing time in UE, T_{ACK} the duration of ACK/NACK message, and T_{NBP} the processing time in Node B.

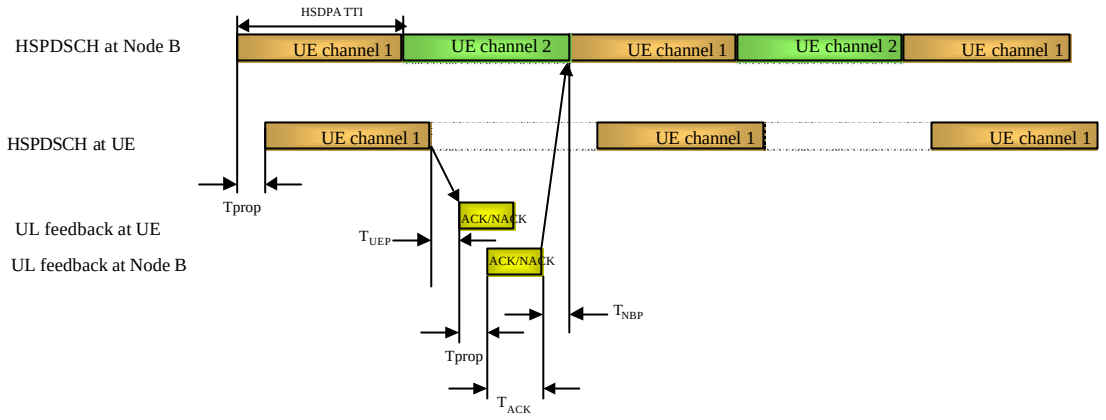

Figure 2. Timing relations for 2-channel HARQ process

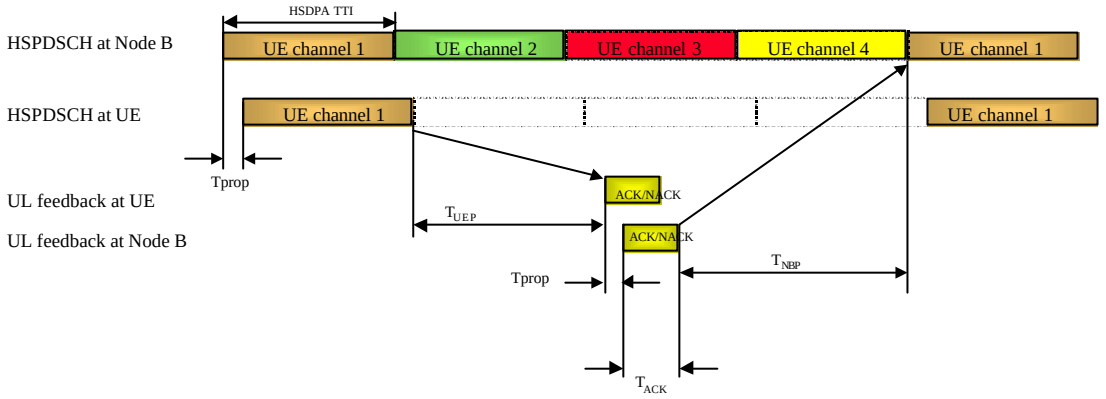

Figure 3. Timing relations for 4-channel HARQ process

The total time $T_{process}$ available for UE and RNS processing can be expressed as:

$$T_{UEP} + T_{NBP} + (N - 1) \cdot TTI + T_{ACK} + 2 \cdot T_{prop}$$

The processing time can be roughly evaluated as in Table 13. The effect of propagation time can be considered negligible and it is not shown in the figures. It is assumed that T_{ACK} duration is one slot.

Table 13. Approximate time for UE and RNS processing with SAW HARQ

	2 subchannels				4 subchannels			
Parameter	1-slot TTI	3-slot TTI	5-slot TTI	15-slot TTI	1-slot TTI	3-slot TTI	5-slot TTI	15-slot TTI
$T_{process}$	0 ms	1.33 ms	2.67 ms	9.33 ms	1.33 ms	5.33 ms	9.33 ms	29.33 ms

The shorter the HSDPA TTI the less time there is available for processing. On the other hand, shorter TTI length reduces the time required for turbo decoding stage. The reduced processing time from shorter TTI length can be offset by increasing the number of subchannels. The actual amount of time required for processing is naturally implementation dependent. By making a rough assumption that both the UE and Node B use the same period of time, an estimate for the processing time can be made by dividing the figures in Table 13 by two.

In practice, there is some control/signal information transmitted by the Node B related to the data sent on HSPDSCH. Among other things this message could inform the UE of whether there is something sent to it during the particular HSDPA TTI, e,g, whether to read a control channel. This control/signal information could be transmitted at the same time as the respective TTI on HSPDSCH, which requires buffering the TTI at the UE. On the other hand, if this kind of information is sent prior to the respective HSDPA TTI, it is easier for the UE to know from which Node B the transmission is coming from and buffering TTIs possibly from several Node Bs is

not needed. Sending the control/signal information early, however, reduces the Node B processing time T_{NBP}. This effect is depicted in Figure 4 where T_{CTRL} is the time needed for sending control/signal information.

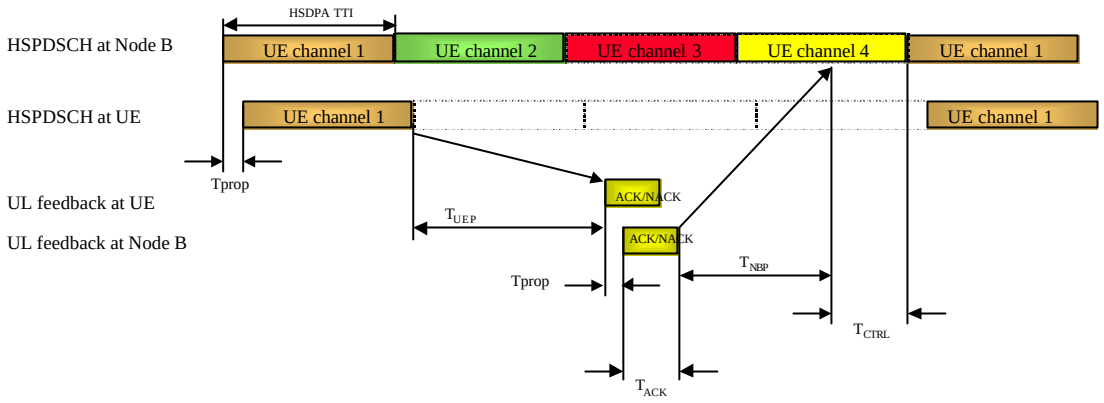

Figure 4. Timing relations for 4-channel HARQ process with downlink control/signal information prior to HSPDSCH transmission

7.2.2.1.5 Conclusions

Based on the complexity considerations presented above SAW HARQ is a feasible concept for HSDPA system, and it can be implemented. However, care must be taken with regard to processing time. The effect of HSDPA TTI length and the numb er of HARQ subchannels directly impact the available processing time in UE and RNS.