TSG-RAN Working Group 1 Meeting #18 **TSG*R1#18(01)0059***

Boston, MA., USA
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Agenda Item:	**AH24: High Speed Downlink Packet Transmission**
Source:	**SONY Corporation**
Title:	**UE complexity for AMCS**
Document for:	**Discussion**

1. Introduction

The link adaptation mechanism proposed for HSDPA utilizes adaptive modulation and coding scheme (AMCS). To achieve this, UE is expected to

?? Demodulate and decode AMCS

?? Estimate and Report Downlink Channel Quality to UTRAN

This contribution looks into some UE complexity issues to achieve these functionalities. In particular, performance degradation due to chip sample timing and phase/amplitude estimation error, and accuracy for downlink channel quality measurement are investigated.

2. AMCS Demodulation and Decoding

Adaptive modulation and coding scheme proposed for HSDPA utilizes higher order modulation (8-PSK, 16-QAM and 64-QAM) and different coding rate (R=1/4, 1/2, 3/4 TC) than the current Release99 scheme. Following technical issues that may influence UE complexity are investigated.

2.1. Sampling Timing

Non-ideal sampling point will increase interference seen at the receiver due to inter symbol interference (ISI) caused by Rx base-band filter. It is expected that higher order modulation with lower processing gain are more susceptible to ISI.

Figure 1 shows the increase in required Ec/Ior as the amount of sampling error increases. It can be seen that 64QAM with R=3/4 coding is extremely sensitive to sampling timing error compared to current R99 DSCH with SF=32. More sophisticated chip synchronization tracking mechanism and higher over-sampling rate may be required for 64QAM receiver to achieve reasonable performance.

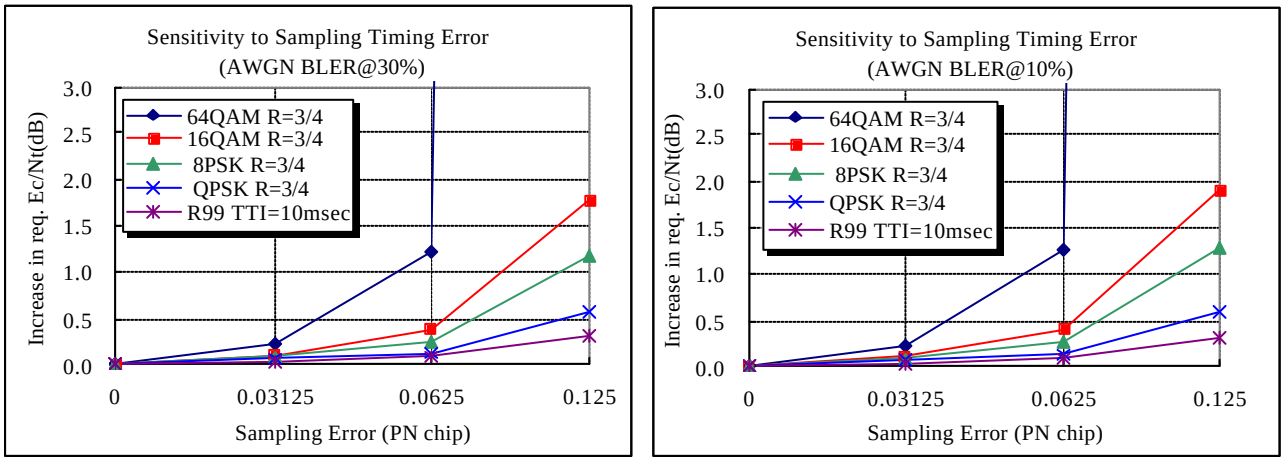

Figure 1. Sensitivity to sampling timing error (BLER@30%, 10%)

2.2. Phase/Amplitude Estimation

Both phase and amplitude references need to be estimated at UE for QAM demodulation. It is assumed that a phase reference is obtained from CPICH as in QPSK demodulation and amplitude reference is obtained from converting CPICH power measurement to DSCH power as shown below.

$$amplitude\_ref \;?\; k \,?\, \frac{G\_dsch}{G\_pilot} \,?\, \frac{SF\_dsch}{SF\_pilot} \,?\, pow\_pilot$$

Here, pow_pilot is estimated CPICH power, $\frac{G\_dsch}{G\_pilot}$ is a gain ratio for DSCH and CPICH and expected be signaled from UTRAN, and k is a constant dependent on modulation order.

Estimation error is categorized into:

?? CPICH estimation error (phase and CPICH power of above equation) due to noise added in a channel

?? Amplitude reference error due to quantization error, rounding error, and Tx-power setting granularity (Includes Node-B contribution).

Sensitivity to each components of estimation error is investigated in the following

2.2.1. CPICH estimation error

Figure 3 and Figure 3 shows the influence of non-ideal channel estimation. The evaluation is done under the worst-case condition by setting DSCH_Ec/Ior to –1dB so that under given Ec/Nt, noise on CPICH is large. Although QAM modulation is more sensitive to channel estimation error, degradation is small enough under slow/medium fading conditions since noise on CPICH is small for the operation range (DSCH_Ec/Nt) of higher order modulation. On the other hand, for fast fading condition, a large degradation is observed for 64QAM. UE under the fast fading may need to adjust CPICH filtering length to obtain reasonable performance for QAM modulation.

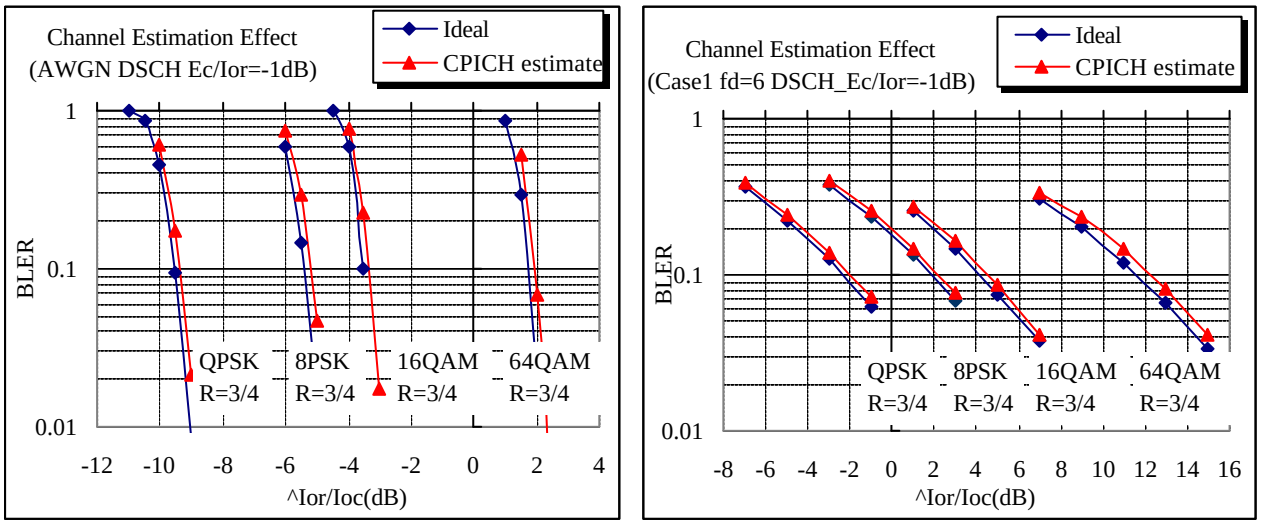

Figure 2 Sensitivity to CPICH estimation error (AWGN, case 1fd=6Hz)

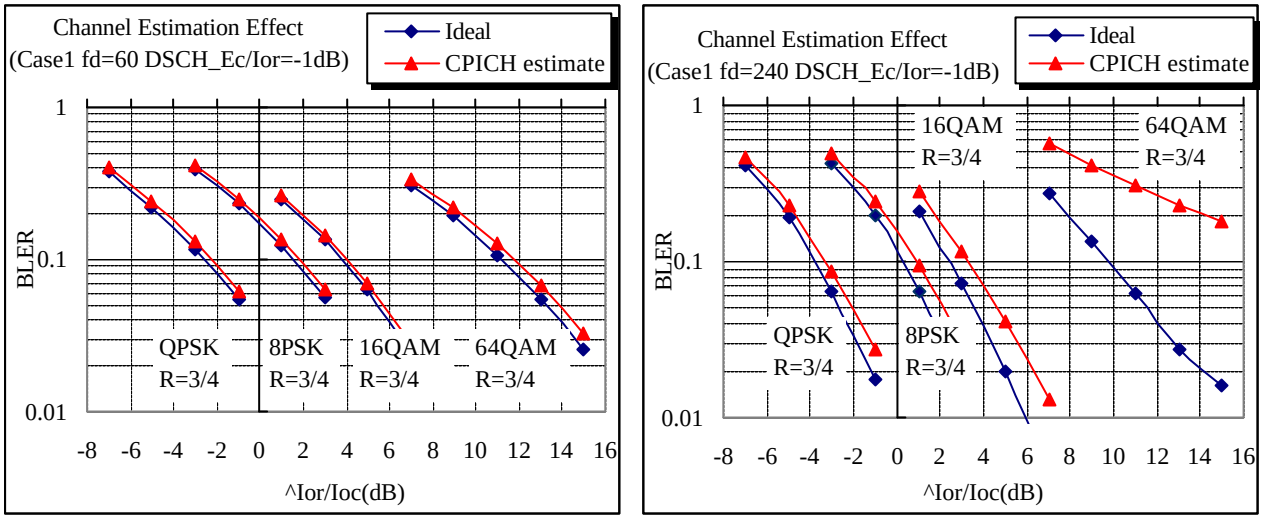

Figure 3 Sensitivity to CPICH estimation error (fd=60,240Hz)

2.2.2. Amplitude reference calculation error

Although not only UE complexity issue, influence of error on DSCP/CPICH power used to calculate amplitude reference for QAM demodulation is investigated. An error in DSCH/CPICH power can be caused by quantization of power offset information, non-perfect Tx-power setting, and limited precision of fixed-point calculation. Accumulated error is modeled as power offset from ideal amplitude reference. Influence of error on CPICH power estimate is not considered here and assumed ideal as it is already considered in 2.2.1.

Figure 4 shows the increase in required Ec/Nt when power offset error is present (BLER=10,30%). As expected, 64QAM mode is more sensitive to power offset error. However, keeping quantization error and accuracy under sufficient level (e.g. 0.5dB) will not be a large factor for an UE with current signal processing capability. Difference between reported DSCH/CPICH power offset and actual transmitted power may need to be considered for Node-B complexity issue.

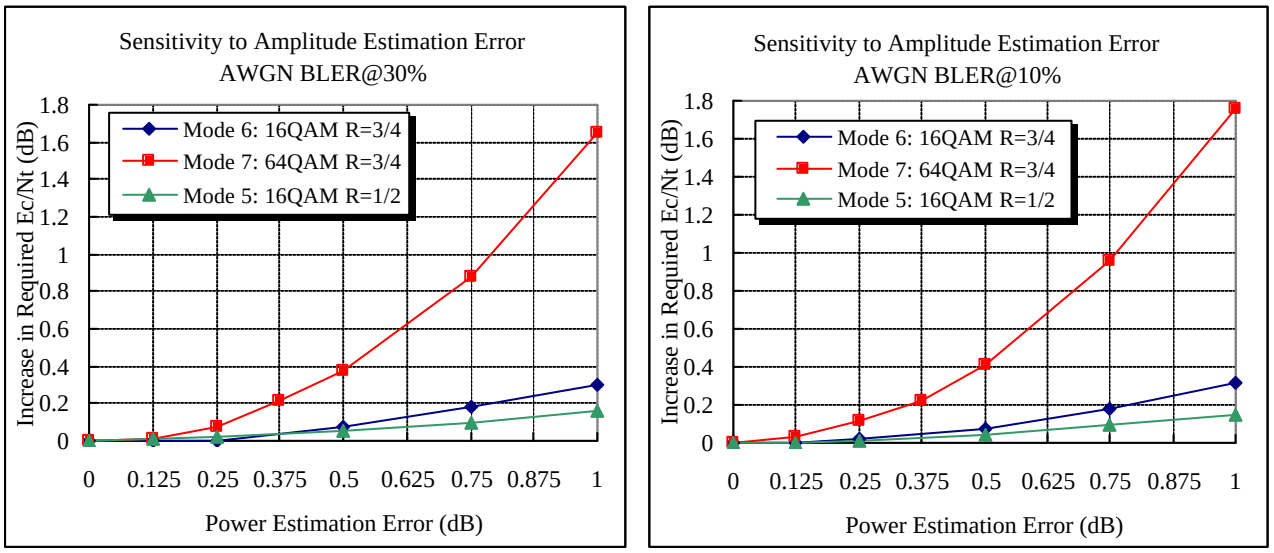

Figure 4 Increase in required Ec/Nt due to amplitude estimation error (BLER@30%, 10%)

3. Downlink Channel Quality Report

In order to assist link adaptation decision criteria by Node-B, UE may be required to report downlink channel quality to UTRAN. Although it has not been decided what is to be measured and reported by UE as a downlink channel quality, one proposal is to use CPICH_RSCP/ISCP measure that has direct link to received data quality. Since CPICH demodulation is anyway needed for other purposes (DPCH demodulation, FCS), additional complexity required at UE is for its calculation. Calculation complexity is relatively small considering that CPICH_RSCP/ISCP is only needed for primary Node-B among all active set. With continuously transmitted CPICH, sufficient accuracy of the measure (less than 1dB) can be established with minimal averaging (No average) as shown in Figure 5. It must be noted that delay associated with reporting (and averaging) has larger impacts on accuracy than a measurement itself [4].

Node-B may also use transmit power control commands (TPC) for DSCH associated DPCH to estimate the downlink channel quality [5]. A use of TPC commands is not expected to influence UE complexity, as the transmission of TPC for associated DPCH is already available for R99 terminals.

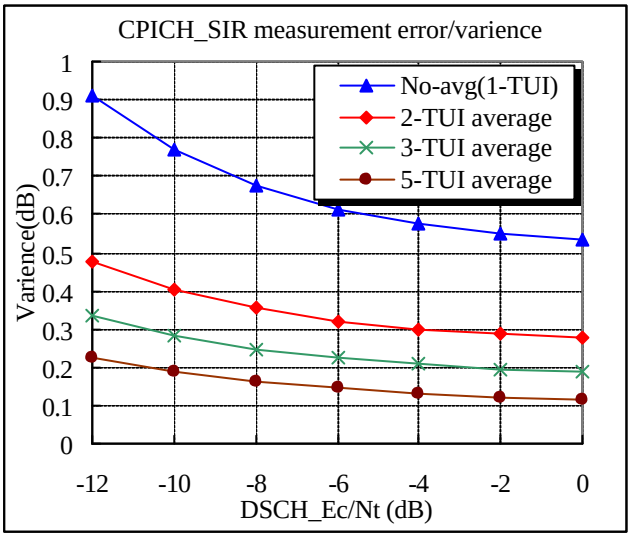

Figure 5 CPCH_RSCP/ISCP estimation accuracy

4. Conclusion

It is recommended that the results presented here be reflected in AMCS complexity evaluation section of TR25.848.

5. References

[1] Motorola: "High Speed Packet Access", TSGR1#13(00)0727, May. 2000
[2] Qualcomm: "Issues for consideration in the HSDPA", TSGR1#15 R1-00-1120, Aug. 2000
[3] Ericsson, Motorola, Nokia: "Link Evaluation Methods for HSDPA" TSGR1#15(00)1093, Aug. 2000
[4] SONY: "Simulation results for E-DSCH", TSGR1#16(00)1238, Oct. 2000
[5] SONY: "Delay on Control Information for HS-DSCH",TSGR1#17(00)1378, Nov, 2000
[6] TR25.HSPA, "Physical Layer Aspects of UTRA High Speed Downlink Packet Access", TSGR1#16(00)1316, Oct. 2000

Annex A: Simulation assumptions

For Sample Timing Error evaluation

Tx-parameter	Modulation	QPSK, 8PSK, 16QAM, 64QAM
	Coding	TC R=1/3, 3/4
	Transmit Unit Interval	5-slot (3.33msec)
	DSCH_Ec/Ior	-14dB per code
	OCNS	To make Ior=1; Only 1-QPSK modulated code is used
	Tx-diversity	OFF
	ARQ	Not applied
Channel	Channel Condition	AWGN
Rx Parameter	ADC/AGC	Ideal
	Base band filter	RRC (tap=16xoversampling rate : a =0.22)
	Over sampling rate	32
	Number of rake fingers	Same as number of path allocated (1)
	Channel Estimation	Ideal
	TC decoder	Max-log

For channel Estimation Error evaluation

Tx-parameter	Modulation	QPSK, 8PSK, 16QAM, 64QAM
	Coding	TC R=1/3, 1/2, 3/4
	Transmit Unit Interval	5-slot (3.33msec)
	DSCH_Ec/Ior	-1dB per code;
	OCNS	To make Ior=1; Only 1-QPSK modulated code is used
	Tx-diversity	OFF
	ARQ	Not applied
Channel	Channel Condition	AWGN, 2-path fd=6,60, 120Hz (modified case 1 TS25.101)
Rx Parameter	ADC/AGC	Ideal
	Base band filter	None
	Over sampling rate	1
	Number of rake fingers	Same as number of path allocated
	Channel Estimation	From CPICH symbols
	TC decoder	Max-log

Appendix B: Additional Simulation Results for Sampling Timing Error

The BLER degradation due to sampling timing error is shown in figures below. A large degradation is shown for 64QAM R=3/4 mode as it was not able to achieve BLER less than 30% under the condition where there is 0.125 PN chip timing error at a receiver.

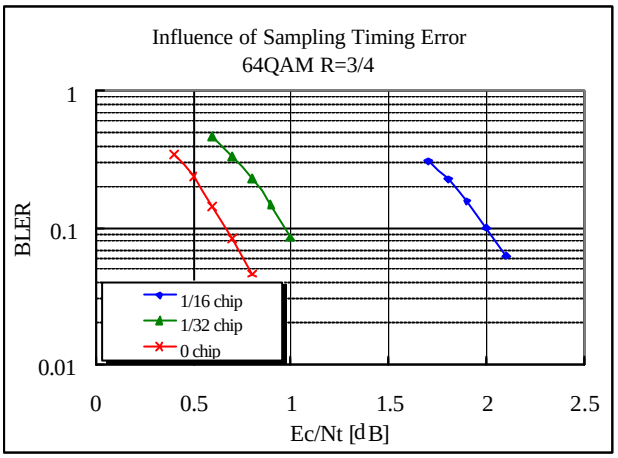

Figure 6 64QAM R=3/4

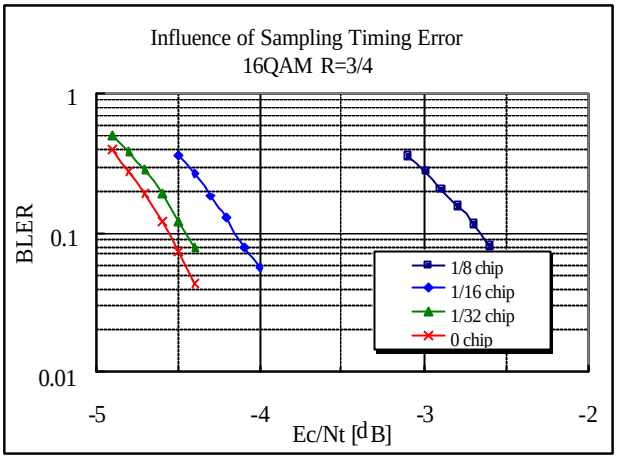

Figure 7 16QAM R=3/4

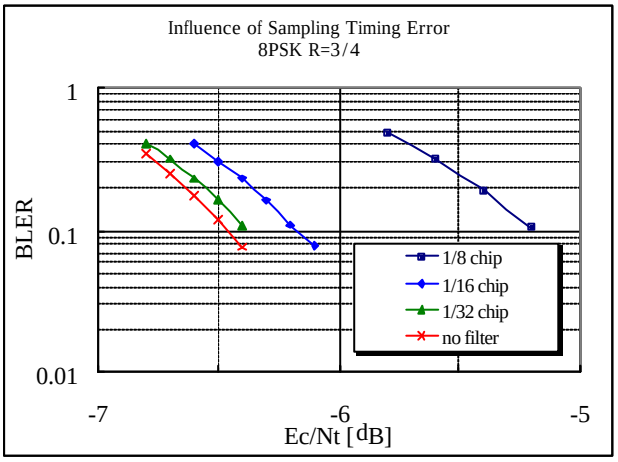

Figure 8 8PSK R=3/4

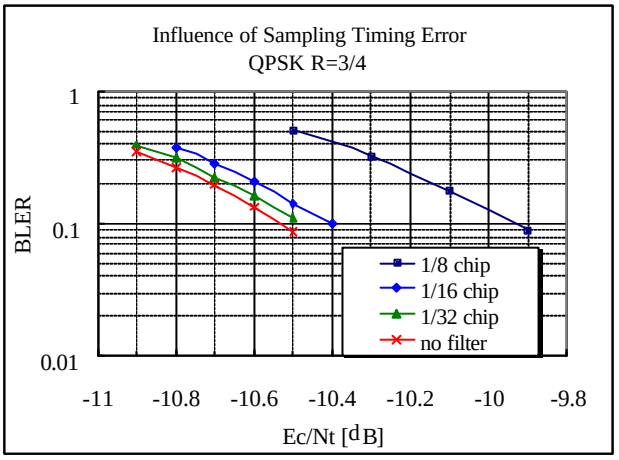

Figure 9 QPSK R=3/4