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Agenda Item : 1.28 Mcps TDD Ad hoc

Source : Samsung Electronics Co., Ltd

Title : TFCI Coding Scheme for 8PSK in low chip rate TDD Option

Document for : Discussion and Approval

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1. INTRODUCTION

In this contribution, we propose a TFCI coding scheme for 1.28 Mcps TDD option when 8PSK modulation is used.

In 1.28 Mcps TDD option, when QPSK modulation is used, the current TFCI coding scheme is the same as that of 3.84 Mcps TDD option; depending on the number of TFCI bits, repetition, bi-orthogonal, or the second order Reed-Muller codes are used for TFCI encoding. When 8PSK modulation is used, the odd bits of these encoded bits are repeated to obtain a TFCI encoding for 8PSK [1].

In this paper, we propose TFCI coding schemes for 1.28 Mcps TDD option when 8PSK modulation is used. The proposed schemes have minimum distance $d_{min} = 12$ when the number of TFCI bits are 3 – 5, and minimum distance $d_{min} = 18$ when the number of TFCI bits are 6 – 10, which improves the current TFCI coding scheme by 4 and 2, respectively. In fact, $d_{min} = 12$ is the optimal bound for (24,5) linear block code. Since minimum distance determines error-detecting and error-correcting capabilities of a code, the improvement by 4 and 2 is significant. Simulation results for AWGN and fading channels are provided to show the coding gain of the proposed TFCI coding scheme over the current scheme.

In Section 2, the current TFCI coding scheme is described. In section 3, the proposed TFCI coding scheme is described and compared with the current coding scheme. In Section 4, hardware complexity issue is discussed. As discussed in Section 4, the proposed scheme achieves a significant coding gain with little added hardware complexity. In Section 5, simulation result is presented. Section 6 concludes this paper.

2. The Current TFCI Coding Scheme.

The TFCI coding scheme for 1.28 Mcps TDD option is the same as that of 3.84 Mcps TDD option when QPSK modulation is used. For 8PSK modulation, odd-bit repetition of the encoded TFCI code word is used. The description of the current TFCI coding scheme in [1] is as follows.

"Encoding of the TFCI bits depends on the number of them and the mode of modulation applied. When the modulation of QPSK is deployed, encoding of the TFCI bits is the same as it in the high chip rate option. That is to say, if there are 6-10 bits of TFCI, the TFCI bits are encoded using a

(32,10) sub-code of the second order Reed-Muller code. If the number of TFCI bits is in the range 3 to 5, the TFCI bits are encoded using a (16, 5) bi-orthogonal (or first order Reed-Muller) code. If the number of TFCI bits is 1 or 2, then repetition will be used for coding. In this case each bit is repeated to a total of 4 times giving 4-bit transmission (NTFCI=4) for a single TFCI bit and 8-bit transmission (NTFCI=8) for 2 TFCI bits. When 8PSK service is transmitted, the modulation of 8PSK is applied in low chip rate option. In this case of 8PSK service, the odd bits of the encoded TFCI bits from the TFCI coder are repeated (e.g. the input is b0, b1, b2, b3, b4… the output will be b0, b1, b1, b2, b3, b3, b4…). Thus the amount of encoded bits of TFCI in this case will be 48, 24, 12, 6 respectively for the 6-10, 3-5, 2, 1 TFCI bits. The same TFCI lengths like in WB-TDD are supported (0, 4, 8, 16, 32)."

Table 1 summarizes the current TFCI coding scheme.

The number of TFCI bits	Modulation Scheme	
	QPSK	8 PSK
1	4 times Repetition Code	6 times Repetition Code
2	4 times Repetition Code	Odd bit Repetition
3 – 5	(16,5) Bi-orthogonal Code	(24,5) odd-bit repeated Bi-orthogonal Code
6 – 10	(32,10) the second order Reed-Muller code	(48,10) odd-bit repeated the second order Reed-Muller code

Table 1. Current TFCI coding scheme.

3. The Proposed TFCI Coding Schemes

The TFCI coding scheme is different depending on the modulation in use and the number of TFCI bits. When QPSK modulation is used, the proposed TFCI coding scheme uses the same coding scheme as described in TR 25.928. For 8PSK modulation, new TFCI coding schemes are proposed.

3.1. Coding of Long TFCI Lengths for 8PSK Modulation

Figure 1 and 2 illustrates the current and proposed TFCI coding schemes, respectively, when the number of TFCI bits are 6 – 10 bits. As shown in Figure 1, the current TFCI coding scheme consists

of two blocks. The first one is a generator block and the second one is a repetition block. In the generator block, a sub-code of second order of Read-Muller code of length 32 is generated from 6 – 10 bits of TFCI bits, and the odd bits of the 32 bit code word is repeated to obtain a 48 bit TFCI encoding in the second block. The current TFCI coding scheme has minimum distance $d_{min} = 16$.

The proposed TFCI coding scheme in Figure 2 also consists of two blocks. The first one is a (64,10) sub-code of the second order Reed Muller code generator, and the second one is a puncturing block that punctures 16 bits out of 64 bits according to a predetermined puncturing pattern to obtain 48 bit TFCI code word. The proposed TFCI coding scheme renders a minimum distance $d_{min} = 18$.

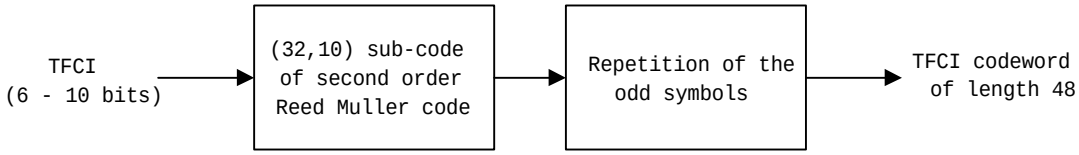

Fig 1. The current TFCI coding scheme

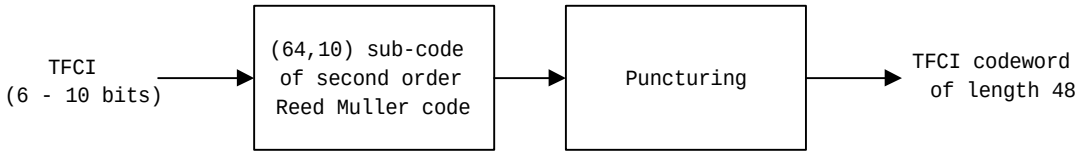

Fig 2. The proposed TFCI coding scheme

Even though the two schemes illustrated in Figure 1 and 2 are similar in structure, they have a couple of differences. First, in the second block, the current scheme uses repetition and the proposed scheme uses puncturing. Secondly, the base code length is different; the current scheme uses (32,10) second order Reed-Muller code, while the proposed scheme uses (64,10) second order Reed-Muller code. Except for these differences, the operation of the two schemes is exactly the same. Since the encoding schemes have the similar structure, the decoders of the two schemes share the same structure, too. Both schemes can use Inverse Fast Hadamard Transform (IFHT), which is quite simple and efficient, to decode the code words. Thus, the proposed scheme achieves a performance enhancement with negligible additional hardware complexity. See Section 4 for more discussion of the hardware complexity. The characteristics of the proposed scheme are summarised as follows.

- Base code: (64,10) sub-code of second order Reed Muller code
- Puncturing to maximize the d_{min} ($d_{min} = 18 > 16$)
- IFHT can be used to decode

The structure of the encoder and decoder for TFCI coding is an implementation issue. However, an example of the structure of the encoder block in Figure 2 (a (64,10) sub-code of second order Reed-Muller code generator) is depicted in Figure 3, where the encoder consists of punctured Walsh codes, all 1's sequences, and masks shown in Table 2.

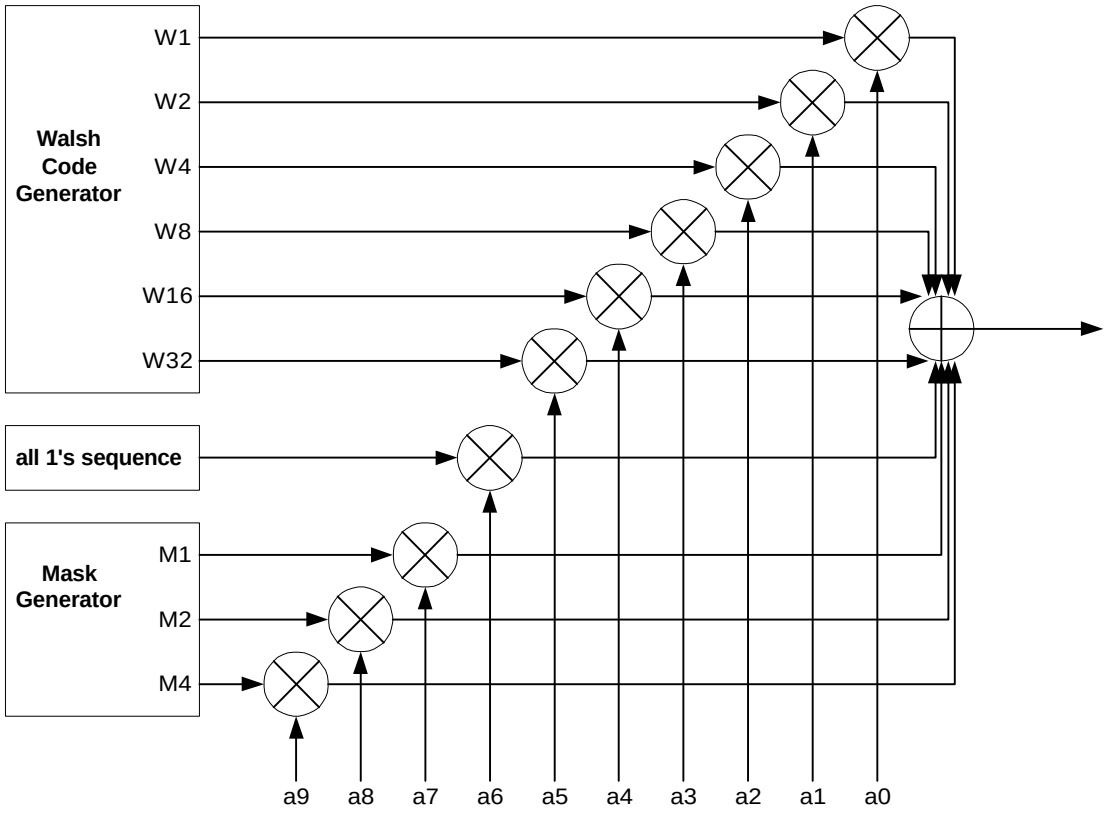

Fig 3. An example of the structure of the (64,10) sub-code of the second order Reed-Muller Code genertor.

Name	Values
W1	10110110100110110101001001101100110101011011001001
W2	01101101101101101100100100100101101100100100101101 1
W4	00011100011100011100011100011100011100011100011100 0111
W8	00000011111100000011111100000011111100000011111
W16	00000000000011111111111100000000000011111111111
W32	00000000000000000000000011111111111111111111111
M1	01110111011101001100001111101000101110111110000 1
M2	10011110100111010101110101110100101011100111110 0

M4	00100011001110110011001010111111110101100110011 0
Puncturing pattern	0, 4, 8, 13, 16, 20, 27, 31, 34, 38, 41, 44, 50, 54, 57, 61

Table 2. Punctured Walsh codes and masks, and the puncturing pattern.

3.2. Coding of Short TFCI Lengths for 8PSK modulation

3.2.1 Coding of very short TFCIs

When the number of TFCI bits is 1 or 2, then repetition will be used for the coding. In this case, each bit is repeated to a total of 6 times giving 6-bit transmission (NTFCI = 6) for a single TFCI bit and 12-bit transmission (NTFCI = 12) for 2 TFCI bits. For a single TFCI bit b_0, the TFCI code word shall be $\{b_0, b_0, b_0, b_0, b_0, b_0\}$. For TFCI bits b_0 and b_1, the TFCI code word shall be $\{b_0, b_1, b_0, b_1, b_0, b_1, b_0, b_1, b_0, b_1, b_0, b_1\}$.

3.2.1 Coding of short TFCIs

Figure 4 and 5 illustrates the current and proposed TFCI coding schemes, respectively, when 8PSK modulation is used and the number of TFCI bits are 3 – 5 bits. As in the case of long TFCI, both TFCI coding schemes consist of two blocks. The differences between the long and short TFCI cases are as follows.

1. In the first block, instead of second order Reed-Muller code, (16,5) bi-orthogonal code and (32,5) first order Reed-Muller codes are used for the current and proposed TFCI coding schemes, respectively.

2. In the proposed TFCI coding scheme, the puncturing pattern is different.

The current TFCI coding scheme has minimum distance $d_{min} = 8$ while the proposed scheme has minimum distance $d_{min} = 12$, which is the optimal bound for (24,5) linear block code and an improvement of the current scheme by 4. Since the two schemes have the same structure, this improvement comes without any extra hardware complexity. The Inverse Fast Hadamard Transform can be used for decoding. The hardware complexity issue is discussed in section 4.

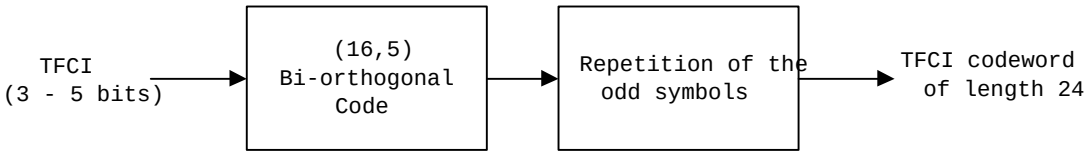

Fig 4. The current TFCI coding scheme

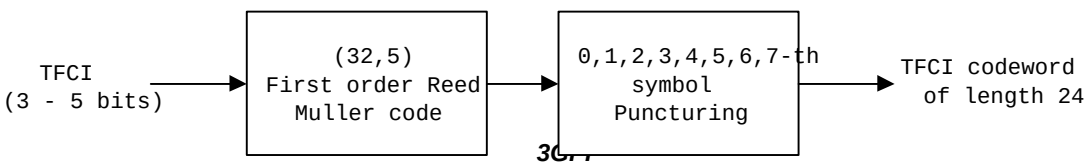

Fig 5. The proposed TFCI coding scheme

Table 3 shows the mapping between the information bits 'I' and the code words 'C' of a (32,5) first order Reed-Muller code generator. Note that the gray shade means the puncturing position.

I	C	I	C
00000	0000 0000 0000 0000 0000 0000 0000 0000	10000	0000 0000 0000 0000 1111 1111 1111 1111
00001	0101 0101 0101 0101 0101 0101 0101 0101	10001	0101 0101 0101 0101 1010 1010 1010 1010
00010	0011 0011 0011 0011 0011 0011 0011 0011	10010	0011 0011 0011 0011 1100 1100 1100 1100
00011	0110 0110 0110 0110 0110 0110 0110 0110	10011	0110 0110 0110 0110 1001 1001 1001 1001
00100	0000 1111 0000 1111 0000 1111 0000 1111	10100	0000 1111 0000 1111 1111 0000 1111 0000
00101	0101 1010 0101 1010 0101 1010 0101 1010	10101	0101 1010 0101 1010 1010 0101 1010 0101
00110	0011 1100 0011 1100 0011 1100 0011 1100	10110	0011 1100 0011 1100 1100 0011 1100 0011
00111	0110 1001 0110 1001 0110 1001 0110 1001	10111	0110 1001 0110 1001 1001 0110 1001 0110
01000	0000 0000 1111 1111 0000 0000 1111 1111	11000	0000 0000 1111 1111 1111 1111 0000 0000
01001	0101 0101 1010 1010 0101 0101 1010 1010	11001	0101 0101 1010 1010 1010 1010 0101 0101
01010	0011 0011 1100 1100 0011 0011 1100 1100	11010	0011 0011 1100 1100 1100 1100 0011 0011
01011	0110 0110 1001 1001 0110 0110 1001 1001	11011	0110 0110 1001 1001 1001 1001 0110 0110
01100	0000 1111 1111 0000 0000 1111 1111 0000	11100	0000 1111 1111 0000 1111 0000 0000 1111
01101	0101 1010 1010 0101 0101 1010 1010 0101	11101	0101 1010 1010 0101 1010 0101 0101 1010
01110	0011 1100 1100 0011 0011 1100 1100 0011	11110	0011 1100 1100 0011 1100 0011 0011 1100
01111	0110 1001 1001 0110 0110 1001 1001 0110	11111	0110 1001 1001 0110 1001 0110 0110 1001

Table 3. Code words of the (32,5) First order Reed Muller Code.

The characteristics of the proposed scheme are summarised as follows.

- Base code: (32,5) sub-code of second order Reed Muller code
- Puncturing to maximize the d_{min} ($d_{min} = 12 > 8$)
- IFHT can be used for decoding

4. H/W Complexity

In this section, the hardware complexities of the proposed schemes are considered. Since, the proposed schemes have similar structures to those of the current schemes, the extra hardware necessary for the proposed TFCI coding schemes are minimal to none.

4.1 H/W complexity of the proposed TFCI coding scheme for long TFCI

Note that the proposed scheme uses the same sub-code of the second order Reed-Muller code. The additional hardware for the encoder and decoder for the proposed scheme is summarised as follows.

- Encoder : Memory for Masks used for the generation of TFCI code words.
- Decoder : Memory for Masks used for the decoding of TFCI code words. The 6^{th} stage of IFHT for the decoding of TFCI code word whose length is 64.

4.1.1 Encoder Structure of the Proposed TFCI Coding Scheme for Long TFCI

The TFCI encoder of the proposed TFCI coding scheme can share the same hardware for QPSK and 8PSK modulations as in the case of the current scheme.

Figure 6 depicts an example of the encoder structure of the proposed TFCI coding scheme when $N_{TFCI} = 6 – 10$. The encoder has two mask generators; the mask generator 1 is for (64,10) sub-code of the second order Reed-Muller code when 8PSK is used, and the other is for (32,10) sub-code of the second order Reed-Muller code when QPSK is used. Note that the masks in mask generator 1 is different from the masks in mask generator 2. The encoder can encode the TFCI bits for QPSK or 8PSK modulation by switching the switches in Figure 6.

As shown in Figure 6, the only extra hardware needed is the mask generator for the generation of the (64,10) Reed-Muller code or the memory to store the masks.

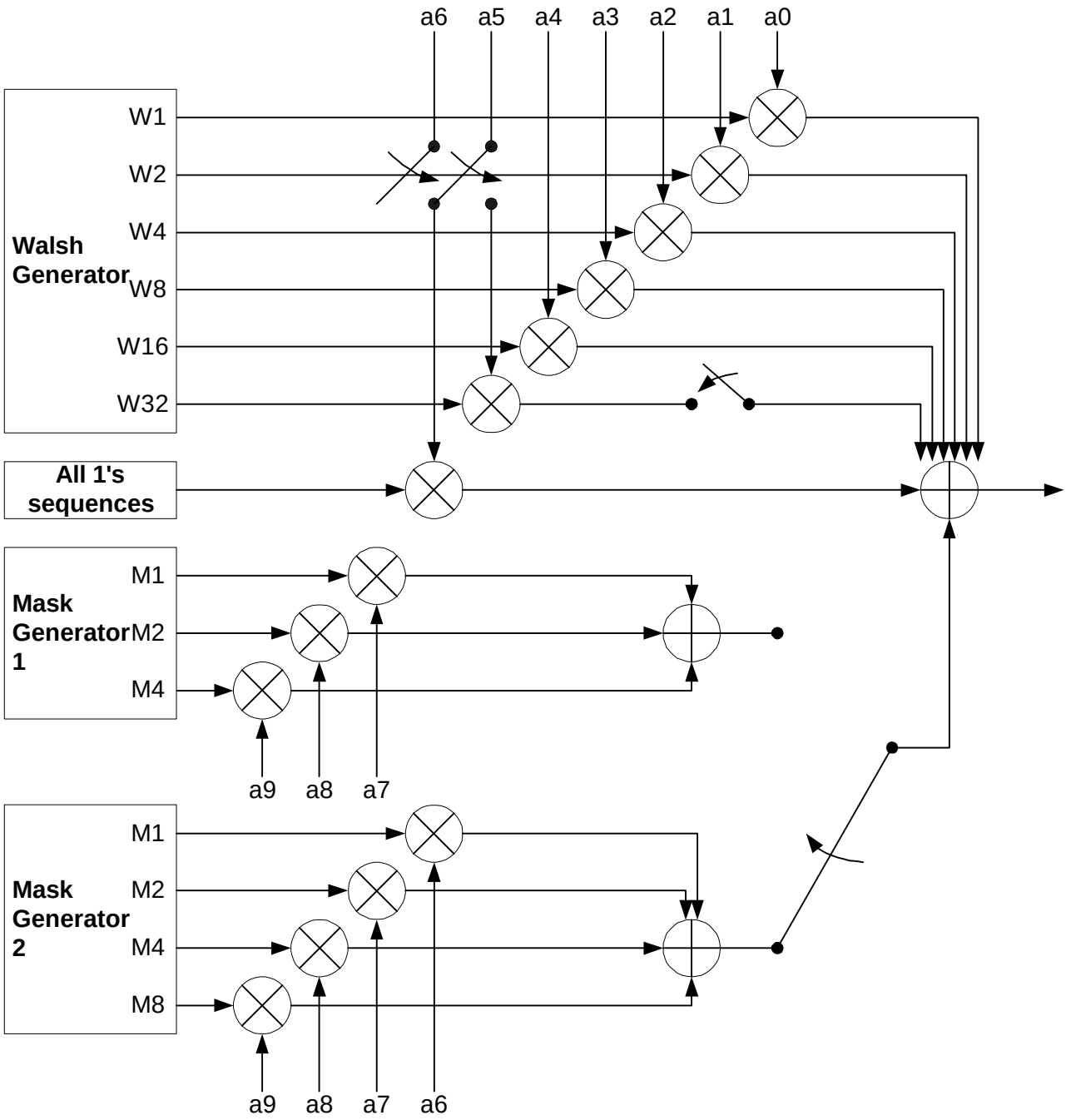

Fig 6. An example of the encoder structure of the proposed TFCI coding scheme for long TFCI.

4.1.2 Decoder Structure of the Proposed TFCI Coding Scheme for Long TFCI

Figure 7 shows the general decoder structure for the sub-code of the second order Reed Muller code. In Figure 7, the decoder consists of a multiplier for the multiplication of the masks, IFHT (Inverse Fast Hadamard Transform) block, and a storage & comparison block.

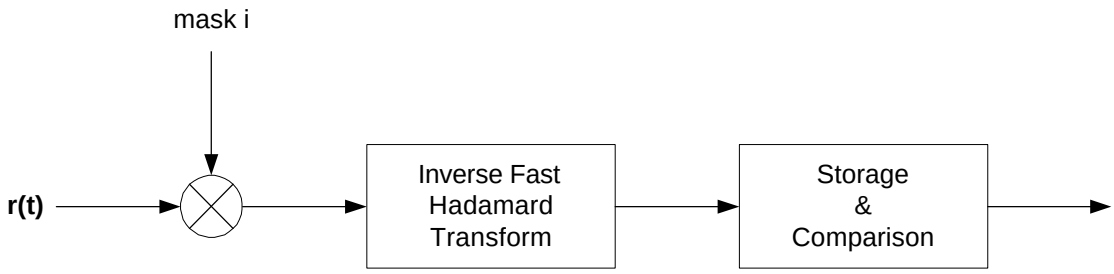

Fig 7. General Decorder structure for the sub code of the second order Reed Muller code.

The additional hardware needed to decode the proposed TFCI coding scheme for 8PSK for long TFCI are some extra memory to store the masks for the (64,10) sub code of the second order Reed Muller code and an extra stage of IFHT of length 64.

Figure 8 illustrates the principal of IFHT for decoding 16 bit code word. As shown in Figure 8, IFHT of length 2^4=16 consists of 4 stages, and the operation of each stage can be conducted iteratively. In general, IFHT of length 2^n consists of n stages.

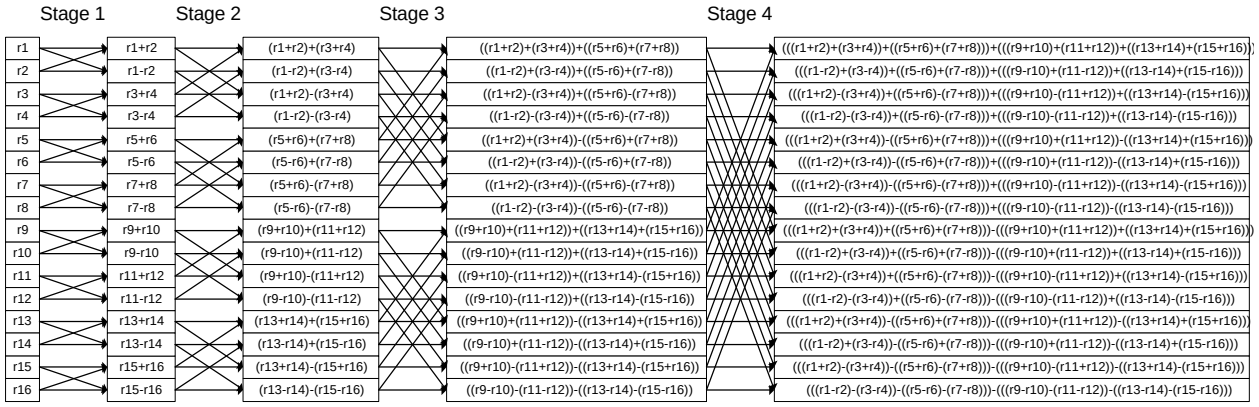

Fig 8. The principal of IFHT of length 16.

For the proposed TFCI coding scheme , the decoder uses a IFHT of length 64 for 8PSK modulation. For QPSK, the 6^{th} stage of the IFHT can be turned off and the output can be obtained from the 5^{th} stage. Note that the IFHT block can be shared with TFCI decoder of short TFCI described below.

4.2 Decoder Structure of the Proposed TFCI Coding Scheme for Short TFCI

Figure 9 shows the general decoder structure for proposed coding scheme i.e. (24,5) punctured first order Reed Muller code. In Figure 5, the decoder consists of a 0 insertion block, IFHT (Inverse Fast Hadamard Transform) block, and comparison block.

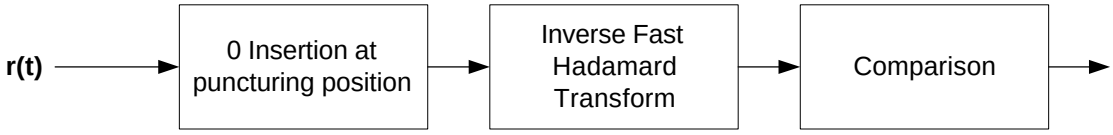

Fig 9. General Decorder structure for (24,5) punctured first order Reed Muller code.

There is no additional hardware needed to decode the proposed TFCI coding scheme for 3-5bits TFCI in 8PSK, because the IFHT for the length 32 is already available for decoding (32,10) the second order Reed Muller code as a sub-block of 64 bit IFHT.

5. Simulation Results

Figure 10 – 12 show the simulation result of the proposed TFCI coding scheme compared to the current scheme for AWGN and fading channels.

The simulation parameters are as follows.

Channel model	1-path
Doppler frequency	30 km/sec
Number of antenna	1
Channel estimation	Ieal
Power control	None

As shown in the figures, the proposed TFCI coding schemes out perform the current schemes. Figure 10 and 11 show the performance of the proposed TFCI scheme for long TFCI for AWGN and fading channels, respectively. At word error rate 0.001, the proposed scheme achieves a coding gain of 0.4 dB for AWGN channel and about 1 dB for fading channel.

Figure 12 shows the performance of the proposed TFCI coding scheme for short TFCI for fading channel. At word error rate 0.001, the proposed scheme has a coding gain of more than 4 dB.

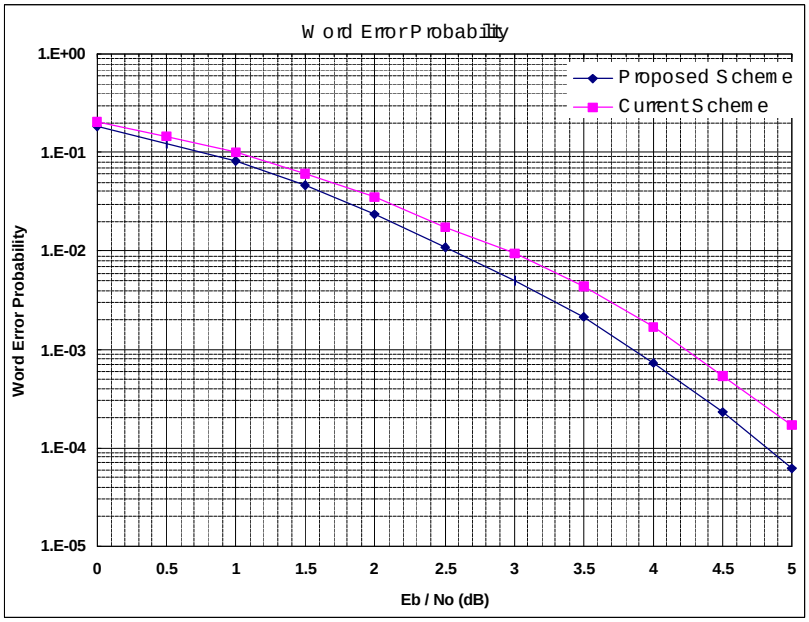

Fig 10. Word error probability of the proposed TFCI coding scheme for long TFCI for AWGN channel.

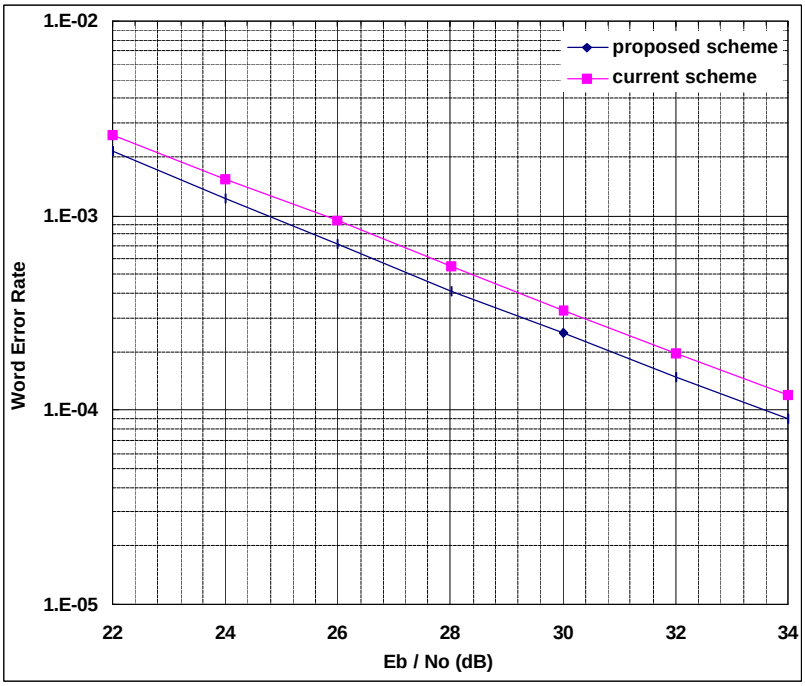

Fig 11. Word error probability of the proposed TFCI coding scheme for long TFCI for fading channel.

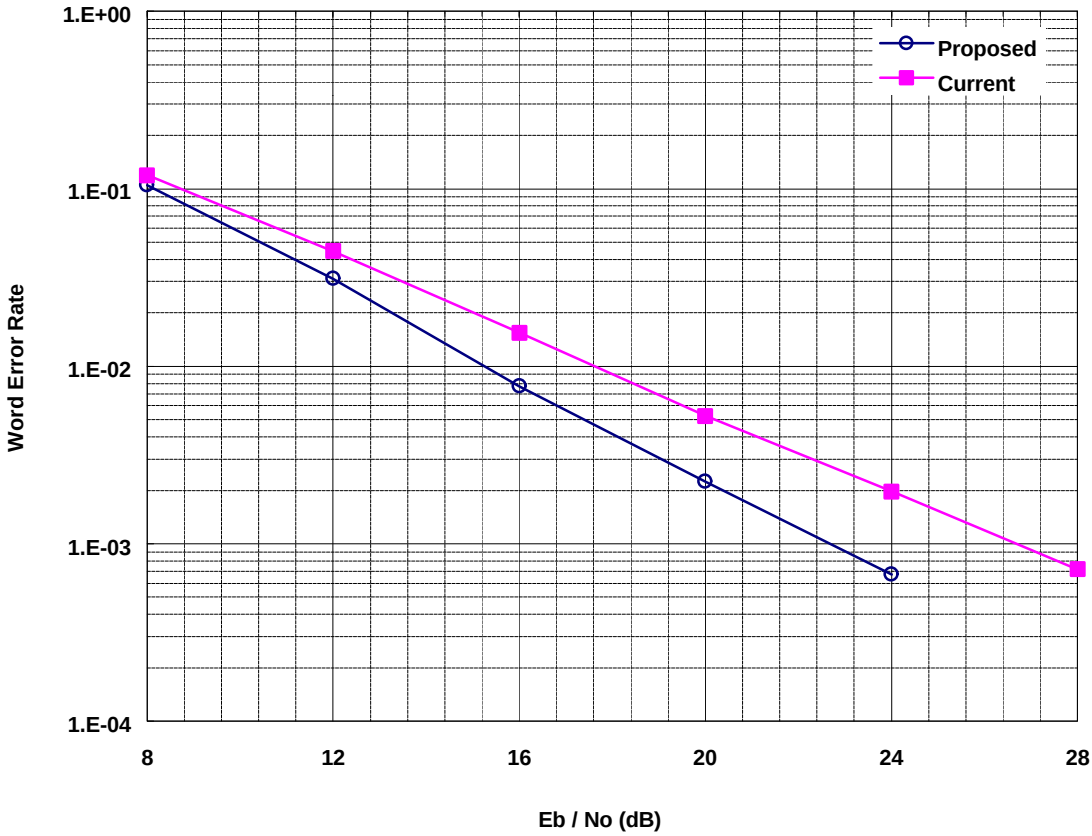

Fig 12. Word error probability of the proposed TFCI coding scheme for short TFCI for fading channel.

6. Conclusion

In this contribution, we propose an efficient TFCI coding scheme for 8PSK modulation.

Since the TFCI symbols carry the information about the Transport Format Combination, TFCI decoding error will cause a serious problem in reconstructing the received data. Therefore, the performance of the TFCI coding scheme is very important.

The coding scheme for TFCI bits varies depending on the number of TFCI bits and the modulation used. When QPSK modulation is used, the proposed TFCI coding scheme is the same as that of the 3.84 Mcps TDD option. For 8PSK modulation, TFCI coding schemes with improved performance are proposed for long and short TFCIs.

The proposed TFCI coding scheme for long TFCI has a minimum distance d_{min} = 18, which is greater than the current scheme by 2. The included simulation result for AWGN and fading channel environment showed that the proposed TFCI coding scheme achieves a coding gain of 0.3 – 0.4 dB and 1 dB for AWGN and fading, respectively, at word error rate 0.001 over the current scheme.

The proposed TFCI coding scheme for short TFCI achieved a minimum distance d_{min} = 12, an optimal bound for (24,5) linear block code. This is an improvement by 4 over the current scheme. The simulation result for fading channel showed that the proposed TFCI coding scheme achieves more than 4 dB of coding gain at word error rate 0.0001 compared to the current scheme.

It is important to note that the coding gain of the proposed TFCI coding scheme comes with minor extra hardware complexity.

We propose to add the following text proposal into the Working CR for TS25.222 as the TFCI coding scheme for 8PSK modulation of the 1.28Mcps TDD.

Reference:

[1] TR 25.928, “Radio Access Network (RAN); 1.28Mcps functionality for UTRA TDD Physical Layer”, TSG RAN, WG1.

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4.4.2 Coding of transport format combination indicator (TFCI) for 8PSK

Encoding of TFCI bits depends on the number of them and the modulation in use. When 2 Mcps service is transmitted, 8PSK modulation is applied in 1.28 Mcps TDD option. The coding scheme for TFCI when the number of bits are 6 – 10, and less than 6 are described in section 4.4.2.1 and 4.4.2.2, respectively.

4.4.2.1 Coding of long TFCI 8PSK

When the number of TFCI bits are 6 – 10, the TFCI bits are encoded by using a (64,10) sub-code of the second order Reed-Muller code, then 16 bits out of 64 bits are punctured (Puncturing positions are 0, 4, 8, 13, 16, 20, 27, 31, 34, 38, 41, 44, 50, 54, 57, 61st bits). The coding procedure is shown in Figure [F1].

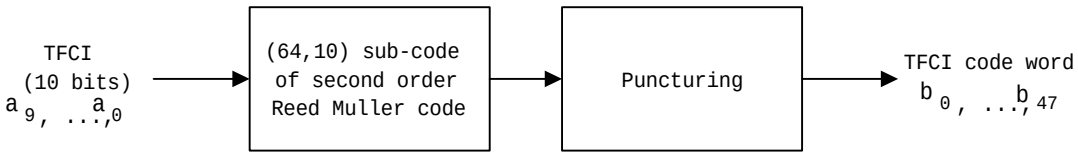

Figure [F1]: Channel coding of long TFCI bits for 8PSK

The code words of the punctured (48,10) sub-code of the second order Reed-Muller codes are linear combination of 10 basis sequences. The basis sequences are shown in Table [T1].

Table [T1]: Basis sequences for (48,10) TFCI code

I	$M_{i,0}$	$M_{i,1}$	$M_{i,2}$	$M_{i,3}$	$M_{I,4}$	$M_{i,5}$	$M_{i,6}$	$M_{I,7}$	$M_{I,8}$	$M_{i,9}$
0	1	0	0	0	0	0	1	0	1	0
1	0	1	0	0	0	0	1	1	0	0
2	1	1	0	0	0	0	1	1	0	1
3	1	0	1	0	0	0	1	1	1	0
4	0	1	1	0	0	0	1	0	1	0
5	1	1	1	0	0	0	1	1	1	0
6	1	0	0	1	0	0	1	1	1	1
7	0	1	0	1	0	0	1	1	0	1
8	1	1	0	1	0	0	1	0	1	0
9	0	0	1	1	0	0	1	1	0	0
10	0	1	1	1	0	0	1	1	0	1
11	1	1	1	1	0	0	1	1	1	1
12	1	0	0	0	1	0	1	0	1	1
13	0	1	0	0	1	0	1	1	1	0
14	1	1	0	0	1	0	1	0	0	1
15	1	0	1	0	1	0	1	0	1	1
16	0	1	1	0	1	0	1	1	0	0
17	1	1	1	0	1	0	1	1	1	0
18	0	0	0	1	1	0	1	0	0	1
19	1	0	0	1	1	0	1	0	1	1
20	0	1	0	1	1	0	1	0	1	0
21	0	0	1	1	1	0	1	0	1	0
22	1	0	1	1	1	0	1	1	0	1
23	0	1	1	1	1	0	1	1	1	0
24	0	0	0	0	0	1	1	1	0	1
25	1	0	0	0	0	1	1	1	1	0
26	1	1	0	0	0	1	1	1	1	1
27	0	0	1	0	0	1	1	0	1	1
28	1	0	1	0	0	1	1	1	0	1
29	1	1	1	0	0	1	1	0	1	1
30	0	0	0	1	0	1	1	0	0	1
31	0	1	0	1	0	1	1	0	0	1
32	1	1	0	1	0	1	1	1	1	1
33	1	0	1	1	0	1	1	0	0	1
34	0	1	1	1	0	1	1	1	1	0
35	1	1	1	1	0	1	1	1	0	1
36	0	0	0	0	1	1	1	1	1	0
37	1	0	0	0	1	1	1	0	1	1
38	1	1	0	0	1	1	1	1	1	1
39	0	0	1	0	1	1	1	1	0	0
40	1	0	1	0	1	1	1	1	0	0
41	1	1	1	0	1	1	1	1	1	1
42	0	0	0	1	1	1	1	1	1	1
43	0	1	0	1	1	1	1	0	1	0
44	1	1	0	1	1	1	1	0	1	0
45	0	0	1	1	1	1	1	0	1	1
46	0	1	1	1	1	1	1	0	0	1
47	1	1	1	1	1	1	1	1	0	0

Let's define the TFCI information bits as a_0 , a_1 , a_2 , a_3 , a_4 , a_5 , a_6 , a_7 , a_8 , a_9, where a_0 is the LSB and a_9 is the MSB. The TFCI information bits shall correspond to the TFC index (expressed in unsigned binary form) defined by the RRC layer to reference the TFC of the CCTrCH in the associated DPCH radio frame.

The output code word bits b_i are given by:

$$b_i = \sum_{n=0}^{9} (a_n \times M_{i,n}) \bmod 2$$

where i=0…47. N_{TFCI}=48.

4.4.2.2 Coding of short TFCI lengths

4.4.2.2.1 Coding very short TFCIs by repetition

When the number of TFCI bits is 1 or 2, then repetition will be used for the coding. In this case, each bit is repeated to a total of 6 times giving 6-bit transmission (N_{TFCI} = 6) for a single TFCI bit and 12-bit transmission (N_{TFCI} = 12) for 2 TFCI bits. For a single TFCI bit b_0, the TFCI code word shall be {b_0, b_0, b_0, b_0, b_0, b_0}. For TFCI bits b_0 and b_0, the TFCI code word shall be {b_0, b_1, b_0, b_1, b_0, b_1, b_0, b_1, b_0, b_1, b_0, b_1}.

4.4.2.2.2 Coding short TFCIs using the first order Reed Muller code

If the number of TFCI bits are in the range of 3 to 5, the TFCI bits are encoded using a (32,5) first order Reed-Muller code, then 8 bits out of 32 bits are punctured (Puncturing positions are 0, 1, 2, 3, 4, 5, 6, 7th bits). The coding procedure is shown in Figure [F2].

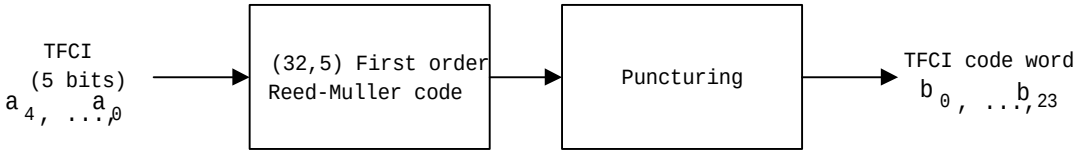

Figure [F2]: Channel coding of short TFCI bits for 8PSK

The code words of the punctured (32,5) first order Reed-Muller codes are linear combination of 5 basis sequences shown in Table [T2].

Table [T2]: Basis sequences for (24,5) TFCI code

I	$M_{i,0}$	$M_{i,1}$	$M_{i,2}$	$M_{i,3}$	$M_{i,4}$
0	0	0	0	1	0
1	1	0	0	1	0
2	0	1	0	1	0
3	1	1	0	1	0
4	0	0	1	1	0
5	1	0	1	1	0
6	0	1	1	1	0
7	1	1	1	1	0
8	0	0	0	0	1
9	1	0	0	0	1
10	0	1	0	0	1
11	1	1	0	0	1
12	0	0	1	0	1
13	1	0	1	0	1
14	0	1	1	0	1
15	1	1	1	0	1
16	0	0	0	1	1
17	1	0	0	1	1
18	0	1	0	1	1
19	1	1	0	1	1
20	0	0	1	1	1
21	1	0	1	1	1
22	0	1	1	1	1
23	1	1	1	1	1

Let's define the TFCI information bits as a_0 , a_1 , a_2 , a_3 , a_4, where a_0 is the LSB and a_5 is the MSB. The TFCI information bits shall correspond to the TFC index (expressed in unsigned binary form) defined by the RRC layer to reference the TFC of the CCTrCH in the associated DPCH radio frame.

The output code word bits b_i are given by:

$$b_i = \sum_{n=0}^{4} (a_n \times M_{i,n}) \bmod 2$$

where i=0…23. N_{TFCI}=24.

4.4.2.3 Mapping of TFCI word

Denote the number of bits in the TFCI word by N_{TFCI}, and denote the code word bits by b_k, where k = 0, …, N_{TFCI}-1. The mapping of the TFCI word to the TFCI bit positions in a time slot shall be as follows.

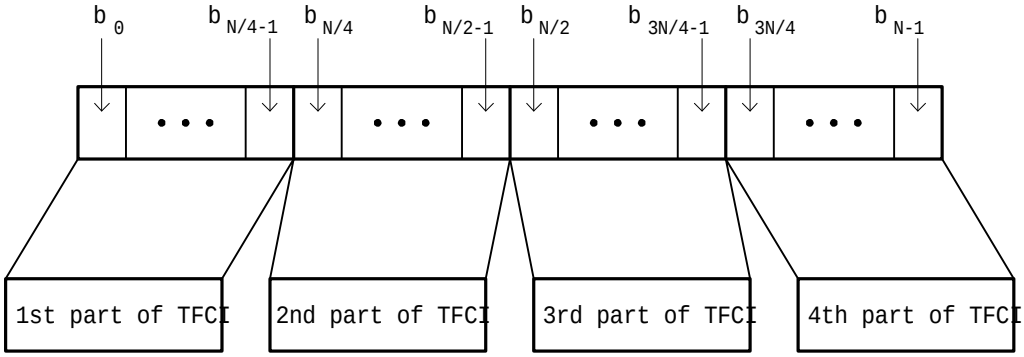

Figure [F3]: Mapping of TFCI word bits to timeslot in 1.28 Mcps TDD option, where N = N_{TFCI}.

The location of the 1st to 4th parts of TFCI in the timeslot is defined in [2].