3GPP TSG RAN WG1#14 R1-00-0938

Oulu, Finland , July 4-7, 2000

Agenda Item:

Source: CWTS/CATT

To: TSG RAN WG1

Title: Transmission of TFCI in low chip rate TDD option

Document for: discussion and approval

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1 Summary

In low chip rate TDD option, the concept of transmission of TFCI is same as that of high chip rate TDD option. The TFCI information can be transmitted both uplink and downlink. For every user, it is transmitted once per 10ms i.e. per radio frame. The transmission of TFCI is done in the data parts of the respective physical channel, TFCI and data bits are subject to the same spreading procedure.

However , in low chip rate TDD option , the radio frame is divided into two subframe , so before physical channel mapping there need one more step – subframe segmentation. This will also affect that the transmission of TFCI for it is transmitted once per radio frame. The 10 ms TFCI information is divided into two equal parts transmitted in two sub frame before mapping onto the physical channel. This is some different from that of high chip rate TDD option.

This CR proposes to change the section 5.2.2.1 of TS25.221so that it can cover both the high chip option and low chip rate option.

3GPP TSG RAN WG1 Meeting #14
Oulu, Finland, July 4 –7, 2000

Document R1-00xxx
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.221	CR		Current Version:	3.2.0

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ *↑ CR number as allocated by MCC support team*

For submission to: *list expected approval meeting # here ↑*		for approval	X	strategic		*(for SMG use only)*
		for information		non-strategic		

Form: CR cover sheet, version 2 for 3GPP and SMG *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: *(at least one should be marked with an X)*	(U)SIM		ME	X	UTRAN / Radio	X	Core Network	

Source:	CWTS	**Date:** 30/06/2000
Subject:	Transmission of TFCI in low chip rate TDD option	
Work item:	Low chiprate TDD option	

Category: *(only one category shall be marked with an X)*

F	Correction		**Release:**	Phase 2	
A	Corresponds to a correction in an earlier release			Release 96	
B	Addition of feature	X		Release 97	
C	Functional modification of feature			Release 98	
D	Editorial modification			Release 99	
				Release 00	X

Reason for change: Due to the different frame structure, the transmission of TFCI in low chip rate TDD option is different from that of high chip rate TDD option. So some changes must be done in the corresponding section of TS25.221.

Clauses affected: 5.2.2.1, new 5.2.2.1.1 and 5.2.2.1.2

Other specs affected:

Other 3G core specifications		→ List of CRs:
Other GSM core specifications		→ List of CRs:
MS test specifications		→ List of CRs:
BSS test specifications		→ List of CRs:
O&M specifications		→ List of CRs:

Other comments:

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<--------- double-click here for help and instructions on how to create a CR.

5.2.2.1 Transmission of TFCI

~~Both burst types 1 and 2 provide the possibility for transmission of TFCI both in up- and downlink~~

The transmission of TFCI is done in the data parts of the respective physical channel, this means TFCI and data bits are subject to the same spreading procedure as depicted in [8]. Hence the midamble structure and length is not changed.

The transmission of TFCI is negotiated at call setup and can be re-negotiated during the call. For each CCTrCH it is indicated by higher layer signalling, which TFCI format is applied. Additionally for each allocated timeslot it is signalled individually whether that timeslot carries the TFCI or not.If a time slot contains the TFCI, then it is always transmitted using the first allocated channelisation code in the timeslot, according to the order in the higher layer allocation message.

5.2.2.1.1 Transmission of TFCI in the high chiprate TDD option

Both burst types 1 and 2 provide the possibility for transmission of TFCI both in up- and downlink.

~~The transmission of TFCI is done in the data parts of the respective physical channel, this means TFCI and data bits are subject to the same spreading procedure as depicted in [8]. Hence the midamble structure and length is not changed.~~
The TFCI information is to be transmitted directly adjacent to the midamble, possibly after the TPC. Figure 6 shows the position of the TFCI in a traffic burst in downlink. Figure 7 shows the position of the TFCI in a traffic burst in uplink.

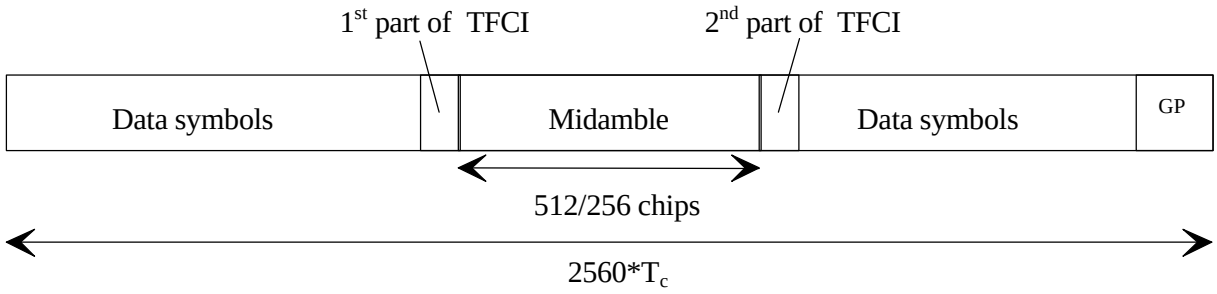

Figure 6: Position of TFCI information in the traffic burst in case of no TPC in the high chiprate TDD option

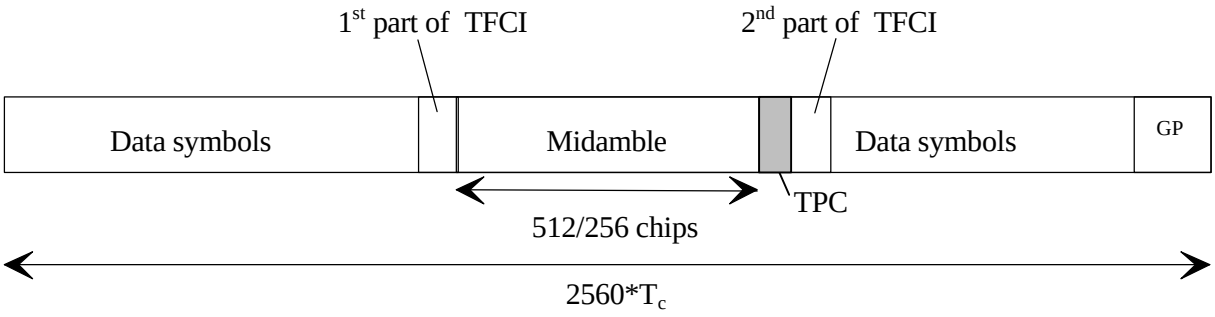

Figure 7: Position of TFCI information in the traffic burst in case of TPC in the high chiprate TDD option

Two examples of TFCI transmission in the case of multiple DPCHs used for a connection are given in the Figure 8 and Figure 9 below. Combinations of the two schemes shown are also applicable. It should be noted that the SF can vary for the DPCHs not carrying TFCI information.

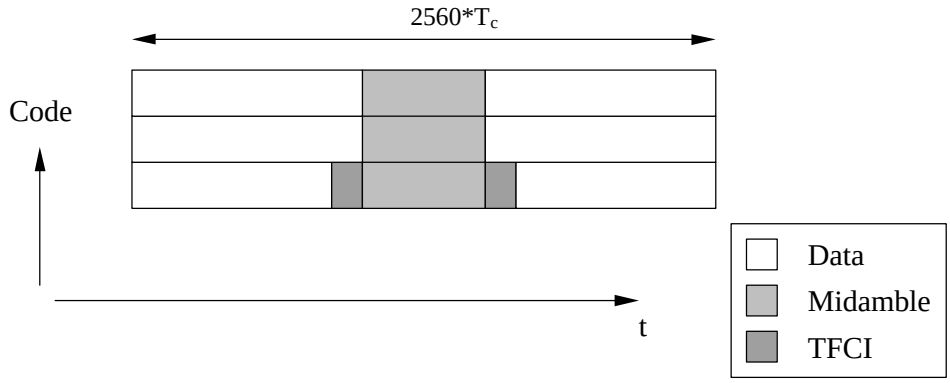

Figure 8: Example of TFCI transmission with physical channels multiplexed in code domain in the high chiprate TDD option

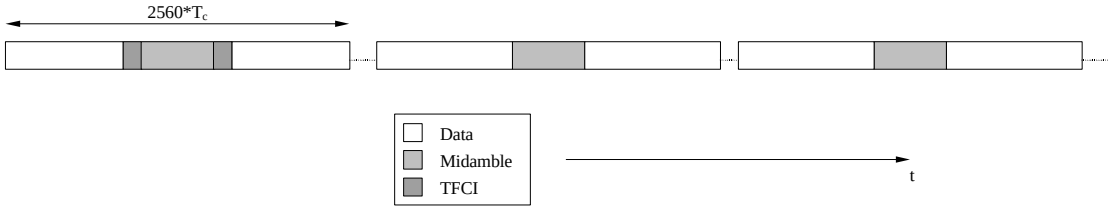

Figure 9: Example of TFCI transmission with physical channels multiplexed in time domain in the high chiprate TDD option

5.2.2.1.2 Transmission of TFCI in the low chiprate TDD option

In the low chiprate TDD option the burst type for normal time slot also provides the possibility for transmission of TFCI in uplink and downlink.

The encoded TFCI symbols are equally distributed between the two subframes and the respective data fields. The TFCI information is to be transmitted directly adjacent to the midamble, possibly after the SS and TPC symbols. Figure [X] shows the position of the TFCI in a traffic burst, if neither SS nor TPC are transmitted. Figure [Y] shows the position of the TFCI in a traffic burst , if SS and TPC are transmitted.

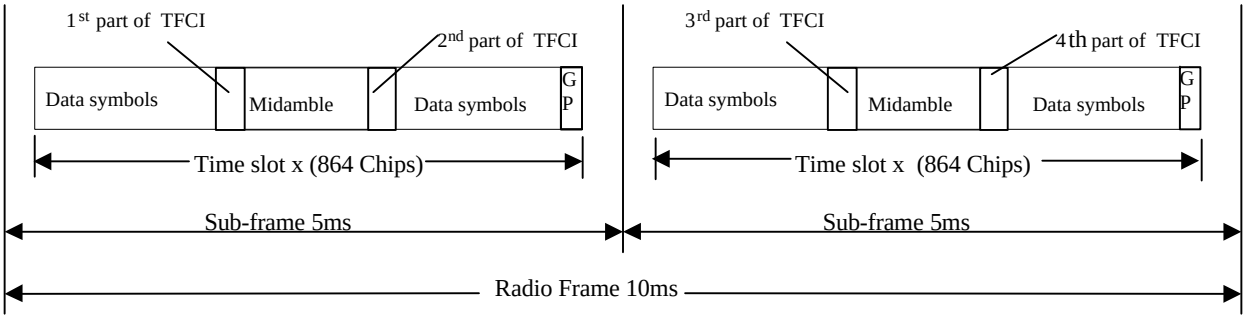

Figure X: Position of TFCI information in the traffic burst in case of no TPC and SS in the low chiprate TDD option

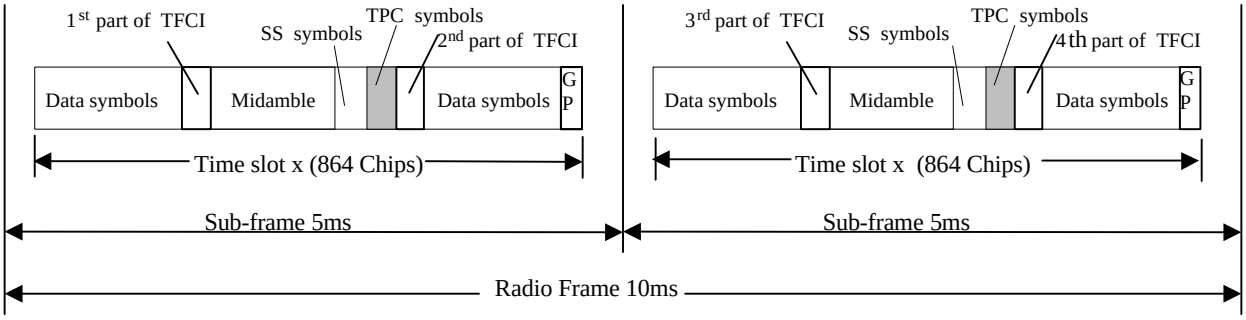

Figure Y:Position of TFCI information in the traffic burst in case of TPC and SS in the low chiprate TDD option