TSG-RAN Working Group1 meeting #14

TSGR1#14(00)0907

Oulu, Finland, 4-7, July 2000

Agenda Item:
Source: **SAMSUNG Electronics Co.**
Title: Uplink Interference Reduction Gain of Gated DPCCH Transmission
Document for: **Discussion**

1. Introduction

In this document, we show the average uplink interference reduction gain in uplink/downlink gated DPCCH transmission mode. In gating mode, the following transmission cases are possible.

- DPCCH only transmission
- DPDCH and DPCCH transmission

That is, as shown in Figure 1, DPCCH is always transmitted but DPDCH can be transmitted when there's data to transmit during gating mode. (Here, for example, DPDCH transfers low rate data such as signaling message which is usually transmitted occasionally. Let "DPDCH frequency" be the probability of transmitting DPDCH during gating mode.)

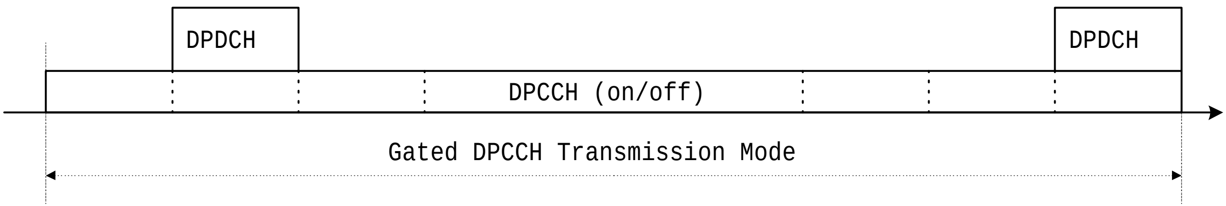

Figure 1. DPDCH Transmission during gated DPCCH transmission mode

The average interference reduction gain is defined as:

Average Uplink interference reduction gain
= (average transmit power when no gating)/(average transmit power when gating)

Note that the average uplink interference reduction gain is defined as the ratio of the average transmission power. Although the transmit power of DPDCH should be increased to compensate the reduced power control rate, the transmit power can be saved during DPCCH only transmission period. Thus the average interference reduction gain highly depends on the DPDCH frequency, and the results are shown with respect to the DPDCH frequency ranges from 1% to 30%.

Simulation and analysis results show that the average interference reduction gain is 4~6dB if the DPDCH frequency is 1%, 2.5~3.5dB if the DPDCH frequency is 10%. Since the average interference reduction gain the ratio of average transmit power, the gated DPCCH transmission provides gain in terms of UE Tx power saving.

2. Link level simulation

2.1 Simulation parameters

The link-level simulation was performed to evaluate the required Eb/No of uplink DPDCH during gated DPCCH transmission mode. Note that the performance of the uplink DPDCH depends on the uplink power control rate (downlink TPC rate). More precisely, the FER of uplink DPDCH is simulated when the downlink TPC is transmitted with rate 1, 1/3, and 1/5. The channel models are CASE1 for 3km/h and CASE3 for 120km/h[11]. The detail simulation parameters are shown in table 1.

Table 1. Simulation parameters (uplink)

Carrier frequency		2.0 GHz
Chip rate		3.84 Mcps
Channel bit rate	DPDCH	60 kbps
	DPCCH	15 kbps

Modulation	Data	BPSK
	Spreading	QPSK
Slot structure	DPCCH	Pilot: 6, TPC: 2, TFCI: 2
	DPDCH	Data: 40
Channel model	Multi-path fading	2-path Rayleigh
	Finger	2 fingers
	Receiver antenna diversity	On
	Doppler frequency [Hz]	5.6(3km/h) , 222(120km/h)
DPCCH/DPDCH [dB]		-2.69dB
Power control	Dynamic range	Unlimited (assume ideal power amplifier)
	Step size	1.0 dB
	Rate	1500Hz(1/1 gating = no gating), 500Hz(1/3 gating), 300Hz(1/5 gating)
	TPC error	4%
Channel estimation		Ideal

2.2 Simulation results

Figure 2 shows the uplink DPDCH FER when the downlink TPC is transmitted with rate 1, 1/3, and 1/5, where GR represents gating rate.

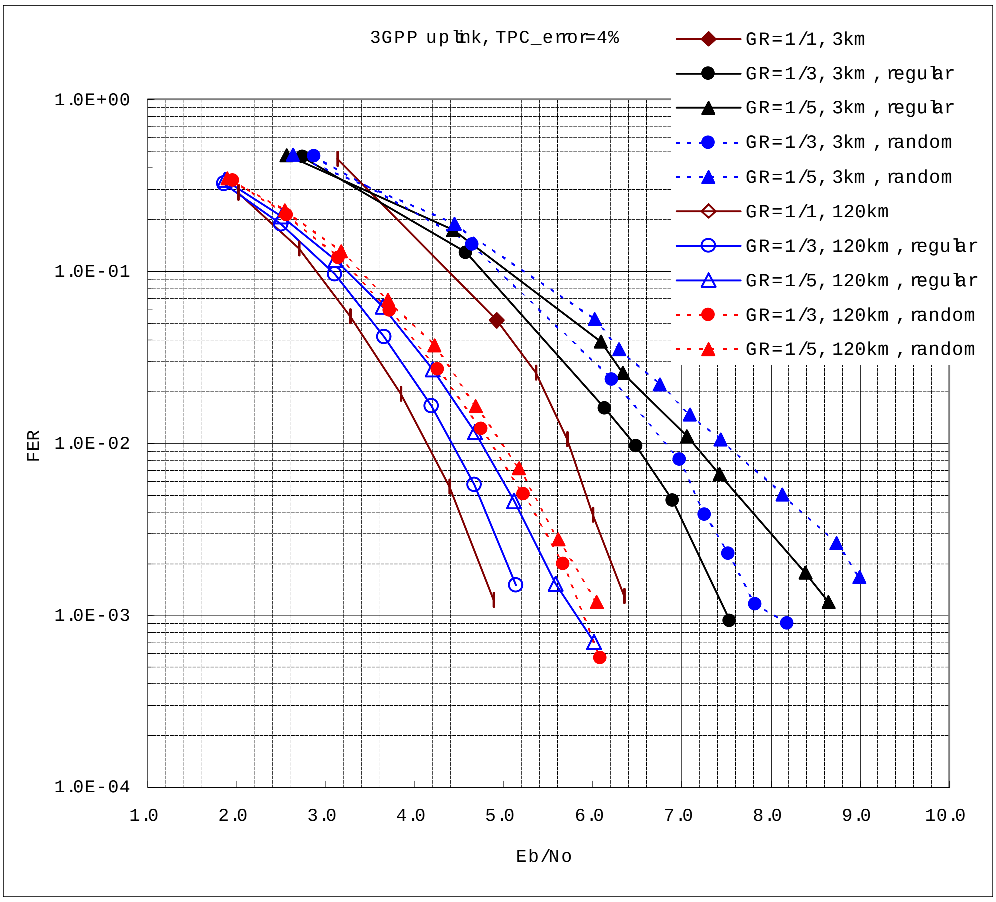

Figure 2. Uplink DPDCH Frame Error Rate with various gating rate and speed

The required received Eb/No for the uplink DPDCH to obtain 1% FER is summarised in table 2 and 3, when the gating pattern is regular and random, respectively. In addition, the Eb/No difference compared with gate rate 1 is also given. From the results, we can see that the Eb/No loss by 1/3 rate gating at 3km/h is about 0.8dB (regular pattern) and 1.1dB (random pattern), for example. The uplink DPCCH performance loss, which is measured by TPC BER, due to gated DPCCH transmission is max. 0.5dB for gating rate=1/5.

Table 2. Required Rx E_b/N_0[dB] to maintain 1% FER (Uplink DPDCH Performance with downlink regular gating pattern[14])

UE speed	Gating Rate		
	1/1	1/3	1/5
3km/h	**5.70**	6.50 (**+0.80**)	7.10 (**+1.40**)
120km/h	**4.20**	4.40 (**+0.20**)	4.80 (**+0.60**)

* ( ) indicates Eb/No difference compared with 1/1(no gating)
Rx. $E_b = E_{DPDCH} + E_{DPCCH}$ per one antenna

Table 3. Required Rx E_b/N_0[dB] to maintain 1% FER (Uplink DPDCH Performance with downlink random gating pattern[14])

UE speed	Gating Rate		
	1/1	1/3	1/5
3km/h	**5.70**	6.80 (**+1.10**)	7.50 (**+1.80**)
120km/h	**4.20**	4.80 (**+0.60**)	5.00 (**+0.80**)

* ( ) indicates Eb/No difference compared with 1/1(no gating)
Rx. $E_b = E_{DPDCH} + E_{DPCCH}$ per one antenna

2.3 Uplink Interference Reduction Gain

In this subsection we analyse the average uplink interference reduction gain in gated DPCCH transmission mode based on the link simulation results in subsection 2.2. The disadvantage of the gated DPCCH transmission is the increase of the required Eb/No to obtain 1% DPDCH FER. In addition, the transmit power of DPCCH also should be increased due to reduced uplink power control rate. The average uplink interference reduction gain is defined in section 1 and restated for convenience.

Average uplink interference reduction gain
= (Average transmit power when no gating)/(Average transmit power when gating)

In order to see the gain, let's assume the following parameters.

F = DPDCH frequency (%),
R = Gating rate (1, 1/3, or 1/5)
P_{DPCCH} = Power of DPCCH,
P_{DPDCH} = Power of DPDCH = $\alpha \times P_{DPCCH}$ (α=2.69dB)
E_{DPCCH} = Additional Eb/No required for DPCCH only transmission (0.5dB)
E_{DPCH} = Additional Eb/No required for DPDCH+DPCCH transmission (Given in table 2, 3)

where α is value usually used in WG4 simulation [x].

From the assumed parameters, only DPCCH is transmitted in F% of time, and both (DPDCH+DPCCH) are transmitted in (100-F)% of time. The average uplink interference reduction gain is defined as the ratio of average transmission power as follows.

Average Uplink Interference Reduction Gain

Average uplink interference reduction gain
= 10 * log10 (P(no gating)/P(gating))

where P(no gating) and P(gating) represents the average transmit power when the gated DPCCH transmission is disabled and enabled, respectively.

P(no gating)

The average transmit power when the gated DPCCH transmission is disabled is given by

P(no gating) = (Average transmit power when no gating)
= (100-F) * P_{DPCCH} + F * (P_{DPCCH} + P_{DPDCH})

$= (100+\alpha\times F)\ P_{DPCCH}$

P(gating)

The average transmit power when the gated DPCCH transmission is enabled is given by

P(gating) = (Average transmit power during only DPCCH transmission when gating)
+ (Average transmit power during (DPDCH+DPCCH) transmission when gating)

During DPCCH only transmission period, the average transmit power is given by

(Average transmit power during only DPCCH transmission when gating)
$= (100-F) * P_{DPCCH} * 10\text{^}(0.1*E_{DPCCH}) * R$

During both (DPDCH+DPCCH) transmission period, there is E_{DPCH} loss, so the required power is

(Average transmit power during (DPDCH+DPCCH) transmission when gating)
$= F * (P_{DPCCH} + P_{DPDCH}) * 10\text{^}(0.1*E_{DPCH})$.

Based on the above method, we calculate the average uplink interference reduction gain for 1% DPDCH frequency as table 4 (F=1).

Table 4. Uplink interference reduction [dB] (1% DPDCH frequency)

UE speed	Overall interference reduction gain [dB]			
	Regular gating pattern		Random gating pattern	
	1/3	1/5	1/3	1/5
3km/h	**4.01**	**5.90**	**3.98**	**5.84**
120km/h	**4.06**	**6.01**	**4.03**	**5.99**

Consequently, in case of 1% DPDCH frequency, the uplink interference reduction gain (4dB~6dB) can be achieved by gated DPCCH transmission in spite of increasing transmission power of DPDCH during gating. The DPDCH frequency has an important role in the uplink interference reduction gain. Figure 3 and 4 show the average uplink interference reduction gain against the DPDCH frequency for regular and random gating pattern, respectively. From these figures, we can see that more than 2.2dB gain can be achieved when the DPDCH duty cycle is 10%, and the gain increases as the DPDCH frequency decreases.

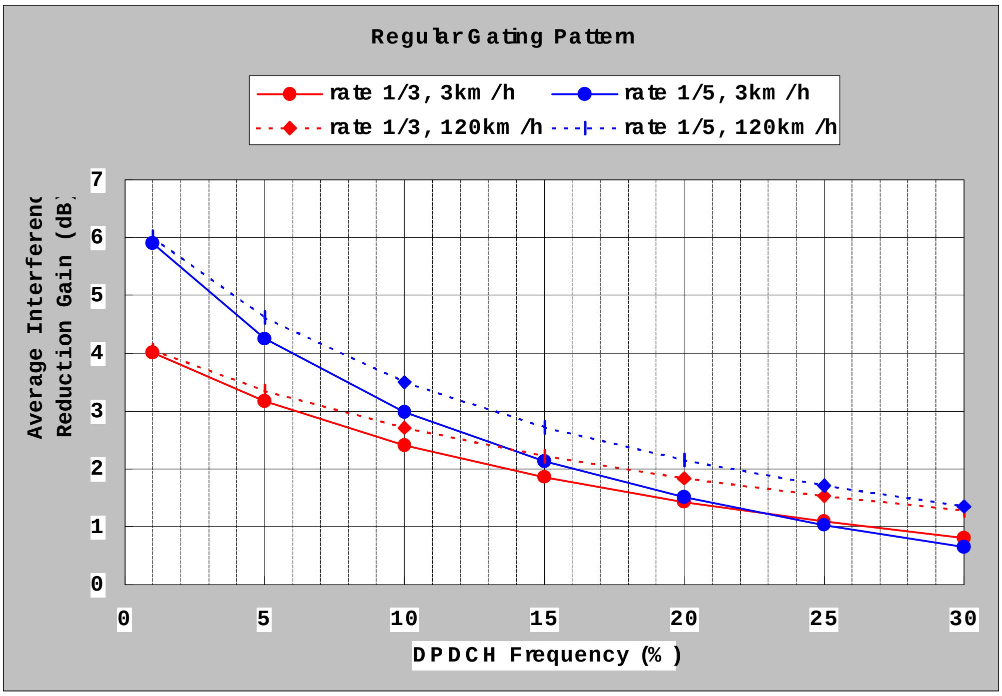

Figure 3. Average uplink interference reduction gain (Regular Gating Pattern)

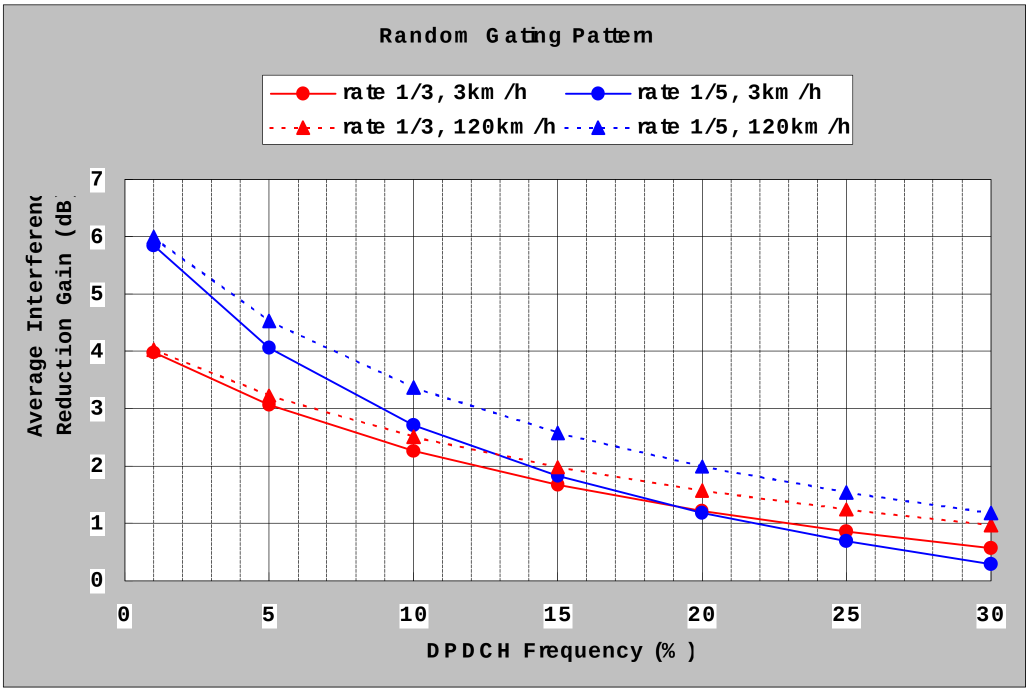

Figure 4. Average uplink interference reduction gain (Random Gating Pattern)

3. Conclusion

One of the advantages obtainable with gated DPCCH transmission is the interference reduction which can be translated to the Tx power reduction. We performed the link level simulation to obtain the required Eb/No when the power control rate is reduced due to gating. And we analysed the interference reduction gain based on the link level simulation results. Since the interference reduction gain is highly dependent on the DPDCH duty cycle, various DPDCH duty cycle (from 1% to 30%) were considered. From the results, we can see that if the DPDCH duty cycle is 10%, the interference reduction gain is more than 2.2dB, and the gain increases as the DPDCH frequency decreases. Consequently, we can conclude that the gated DPCCH transmission is beneficial to the interference reduction, that is, the transmit power reduction.

Reference

[1] TSGR1#4(99)478, “Gated transmission of DPCCH in DCH/DCH control only substates”, SAMSUNG.
[2] TSGR2#4(99)439, “RRC procedures and parameters for gated transmission of uplink/downlink DPCCH in control only substate”, SAMSUNG.
[3] 3GPP RAN S1.14 V2.0.0(1999-04) “FDD Physical layer procedures”.
[4] TSGR1#3(99)191 “Detail description of transmission stop and resumption control”
[5] 3GPP RAN S1.11 V2.0.0(1999-04) “FDD physical channels and mapping of transport channels onto physical channels”
[6] 3GPP RAN S2.03 V0.1.0(1999-04) “UE Functions and Interlayer Procedures in Connected Mode”
[7] Kevin Thompson, Gregory J Miller, and Rick Wilder in MCI Telecommunications Corporation, "Wide-Area Internet Traffic Patterns and Characteristics", IEEE Network Magazine, pp.10~23, November/December 1997.
[8] D.N.Knisely, "Performance Analysis of Control Hold, Suspended, and Dormant State for Packet Data Services", Lucent Technologies,TR45.5.1.5/98.12.
[9] Joseph Shapira, “Microcell Engineering in CDMA Cellular Networks”, IEEE Transactions on Vehicular technology, Vol. 43, No.4, November, 1994.
[10] UMTS 30.03 v3.2.0, “Selection procedure for the choice of radio transmission technologies of the UMTS.
[11] TS 25.104 v.3.2.0 (2000-03)
[12] TSGR1#5(99)669, “Performance evaluation of uplink/downlink DPCCH gating”, SAMSUNG.
[13] TSGR1#6(99)869, “Further clarifications to the gain for the DPCCH gating in COS”, SAMSUNG.

[14] TSGR1#10(00)0108, “Clarification of issues on gated DPCCH transmission”, SAMSUNG.
[15] TSGR1#10(00)0109, “Proposed text for Gated DPCCH transmission in 25.214”, SAMSUNG.

[Contact]

Hokyu CHOI	choihk@telecom.samsung.co.kr
Kiho JUNG	jkiho@samsung.co.kr
Sungho CHOI	shchoi1@samsung.co.kr
Hyeonwoo LEE	woojaa@samsung.co.kr
Changsoo PARK	chang@telecom.samsung.co.kr