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**Title: Proposed Clock Model for Node B Synchronization  
over the Air:**

**Document for: Discussion**

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## 1 Introduction

This paper proposes a clock model for analysis on Node B Synchronization studies. Reference [3], Node B synchronisation for TDD, TSGR1#10(00)0074, Beijing, China, January 18-21 2000 provided performance results for Node B synchronization over the air. The clock model of reference [3] is included in the table below, copied from the reference for convenience.

Parameter	Value
Initial Timing Error	Uniform Random Distribution over $\pm 50$ ms
Initial Clock Rate Error	Uniform Random Distribution over $\pm 0.050$ ppm
Measurement Resolution	$\frac{1}{4}$ chip
Clock Variance	$10^{-17}$ sec <sup>2</sup> /sec

It is a concern that the clock variance of  $10^{-17}$  sec<sup>2</sup>/sec may be too well behaved to serve as a realistic assumption. This model suggests that time drift will grow as a random walk and would take 100,000 seconds, or over one day to grow by 1 microsecond 1 sigma. This paper proposes a clock model that creates a more dynamically changing random component.

## 2 Proposed Model

### 2.1 Input Parameters

The model uses the following input parameters

Time interval for simulation = tint:

Typical value = 1 second (could be 20 seconds)

RMS frequency uncertainty, long term= serror

Typical Value = .05 ppm =  $5 \times 10^{-8}$

Short Term Frequency uncertainty ; e.g. over 1 second:= shterror

This is the Allen Variance; the expected value of the RMS change in frequency with each sample, normalized by the oscillator frequency. where the sample interval is specified; e.g. 1 second or 20 seconds. Note that the term, variance is often used, although the value is usually quoted as the RMS value.

Typical value = 10-10

Random Walk Component = sigmarw

Typical Value = 10-17 sec<sup>2</sup>/sec

## 2.2 *Derived Parameters*

Calculate the parameters alpha and gain from the following:

$$\alpha = (\text{shterror}) * (\text{shterror}) / (2 * \text{sserror} * \text{sserror})$$

$$\text{gain} = \text{SQR}((2 - \alpha) / \alpha) * \text{sserror}$$

$$\text{sigmatau} = \text{sigmrq} / \text{sqr}(\text{tint})$$

## 2.3 *Generating expressions*

For each time interval:

Generate x, a random variable from gaussian distribution:

Mean=0

Sigma=1

$$x1 = x * \text{gain}$$

$$\text{freq} = \text{freq} + \alpha * (x1 - \text{freq})$$

$$\text{tau1} = \text{tau1} + \text{freq} * \text{tint}$$

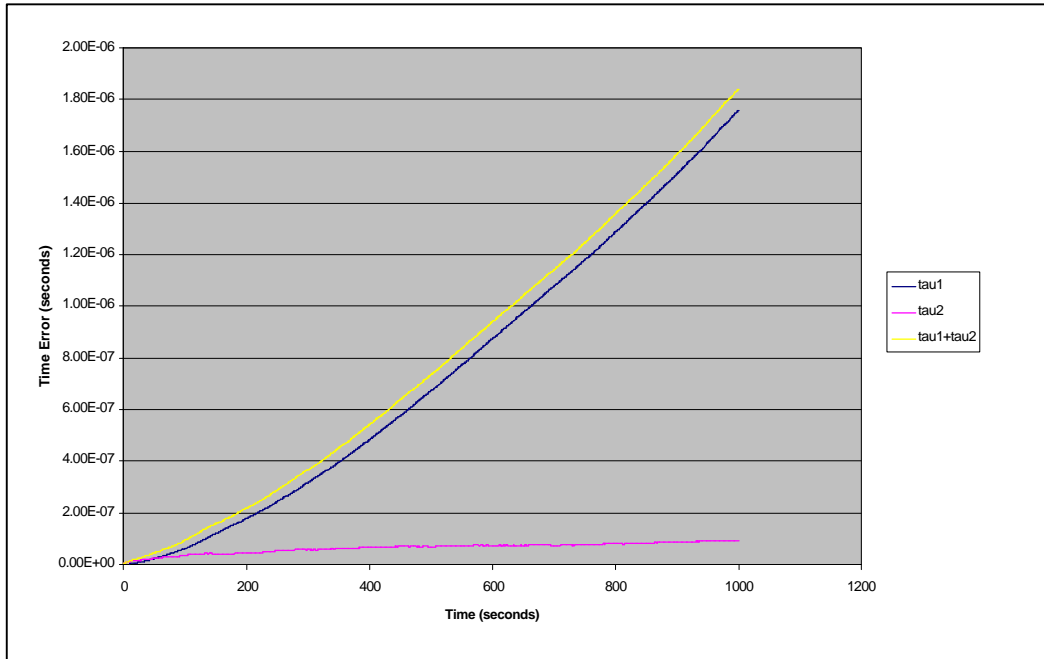
$$\text{tau2} = \text{tau2} + x * \text{sigmatau} * \text{tint}$$

$$\text{tau3} = \text{tau1} + \text{tau2}$$

## 3 **Typical Results**

The following figure shows simulated results for the rms value for tau1, tau2, and tau1+tau2 as function of time for the typical values. The assumption for these curves is that

- Both Frequency and time offset have been estimated correctly up to the time, t=0.
- Time drift shown in the figure represents the deviation from the values which would be predicted based on the estimates which were correct at t=0; i.e. this is the contribution due to the unpredicted random drift.



Observe that this example simulates almost 2 microseconds of clock drift after 1000 seconds, while the random walk model of reference [3] caused only about 0.1 microseconds of random drift.

Note also that these curves represent the drift of one clock from ideal. The relative drift between two non-ideal clocks would be the appropriately larger.

## 4 Conclusions

We have suggested a clock model to serve as the basis for continuing simulation work for the Node B synchronization studies. It may not be totally realistic but it does provide for a greater level of stress to the synchronization process than the original model in reference [3].

However, we encourage other companies to propose a realistic clock model, if available.

## 5 References

- [1] Synchronization of TDD Cells, TSGR3#6(99)905, Sophia Antipolis, France, August 23-27, 1999, InterDigital Comm. Corp.
- [2] NBAP & RNSAP Procedure for TDD Synchronization (some additions/modifications to R3-99905) TSGR3#6(99) 882, Italtel / Siemens, August 23rd 1999, Sophia Antipolis, France
- [3] Node B synchronisation for TDD, Siemens, TSGR1#10(00)0074, Beijing, China, January 18-21 2000
- [4] Synchronisation of Node B's in TDD via Selected PRACH Time Slots, Siemens, TSG RAN WG1 (99)G42, New York, USA, October 12 - 15, 1999

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