**3GPP TSG-RAN WG1 Meeting #114 R1-23xxxxx**

**Toulouse, France, 21-25 August, 2023**

**Agenda Item: 9.17**

**Source: Moderator (Huawei)**

**Title: Summary of email discussion [Post114-38.212-NR\_MIMO\_evo\_DL\_UL]**

**Document for: Discussion and Decision**

# Introduction

This document summarizes the discussions on the 38.212 draft CR on NR MIMO Evolution for Downlink and Uplink, and aims to stabilize the 38.212 draft CR.

[Post114-38.212-NR\_MIMO\_evo\_DL\_UL] Email discussion on Rel-18 draft CRs by September 7 – Editors

# First round discussions

This section summarize the first round email discussions on draft CR v00. Companies are encouraged to provide the first round views by 09/05 (Tuesday), 6:00am UTC, then we can update the draft CR accordingly for the next step discussions.

## Multi-TRP enhancements

Please provide your comments/suggestions on Multi-TRP enhancements here, including unified TCI framework and two TAs for multi-DCI.

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| *Company* | *View* |
| Editor | The changes are marked with author “Yan Cheng\_post RAN1#114” on top of the version R1-2306315 endorsed in RAN1#113, which are to reflect the agreements RAN1#114. |
| QC | For two TAs for multi-DCI, our understanding is that the following agreements should be implemented in 38.212, Section 7.3.1.2.1 (DCI format 1\_0, the part that describes PDCCH order):  **Agreement (RAN1 #114)**  For inter-cell multi-DCI based Multi-TRP operation with two TA enhancement, support indication of additionalPCI in the PDCCH order   * as baseline capability: support PRACH triggering towards servingCell PCI or active additionalPCI.   **Agreement (RAN1 #112-b)**  For intercell multi-DCI based Multi-TRP operation with two TA enhancement, support indication of which PRACH configuration to be used in the RACH procedure in the PDCCH order.   * FFS: Whether *additionalPCI* or a generic identifier is indicated in PDCCH order * FFS: The detail of the indication in PDCCH order in terms of whether to support PRACHtriggered for inactive *additionalPCI*. |
| Samsung | We would like to suggest the following change to unify the field(s) name in 1\_1 and 1\_2.   |  | | --- | | 7.3.1.2.2 Format 1\_1  - TCI ~~states~~ selection – 0 bit if higher layer parameter *tciSelection-PresentInDCI* is not enabled; otherwise 2 bits according to Table 7.3.1.2.2-11. | |
| ZTE | Thanks for editor’s effort on this CR.  **Comment#1**  We share same view to QC that the new field in DCI format 1\_0 of the indication of PRACH triggering towards either serving cell or active additional PCI should be added in TS 38.212. Given that 1 bit is enough to fulfill this indication that CFRA configuration of PRACH triggering associated with CORESETPoolIndex of either serving cell PCI or the active additional PCI, one example is proposed as follows:  --------------------------------------------------------  - PRACH triggering indicator – 0 or 1 bit:  - 1 bit if the higher layer parameter *[additionalCFRA-ToAddModList-r18]* is configured, where value 0 indicates that CFRA configuration of PRACH triggering associated with CORESETPoolIndex of serving cell PCI, and value 1 indicates that CFRA configuration of PRACH triggering associated with CORESETPoolIndex of the active additional PCI.  - 0 bit otherwise.  -------------------------------------------------------- |

## CSI enhancements

Please provide your comments/suggestions on CSI enhancements here, including CSI enhancement for high/medium UE velocities and coherent JT (CJT).

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| *Company* | *View* |
| Editor | The changes are marked with author “Yan Cheng\_post RAN1#114” on top of the version R1-2306315 endorsed in RAN1#113, which are to reflect the agreements RAN1#114. |
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## Reference signal enhancement

Please provide your comments/suggestions on Reference signal enhancements here, including increased number of orthogonal DMRS ports and SRS enhancements.

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| *Company* | *View* |
| Editor | The changes are marked with author “Yan Cheng\_post RAN1#114” on top of the version R1-2306315 endorsed in RAN1#113, which are to reflect the agreements RAN1#114. |
| ZTE (DMRS) | Thanks for editor’s effort on this CR.  **Comment#1**  Similar to the title of Table 73112-25B, the condition “*maxRank>4*” should be added to keep alignment with the following agreement endorsed in RAN1#114 meeting.  **Agreement (RAN1#114)**  For partial/non-coherent PUSCH, if 2 port PTRS is configured in *maxNrofPorts* in *PTRS-UplinkConfig*, and if more than 4 layers is configured in *maxMIMO-Layers* [or *MaxMIMO-LayersDCI-0-2* in *PUSCH-ServingCellConfig],*   * + Alt.1: The size of PTRS-DMRS association field is 4-bit in DCI format 0\_1 [or DCI format 0\_2].   Table 1: PTRS-DMRS association for UL PTRS ports 0 and 1   |  |  |  |  | | --- | --- | --- | --- | | **Value of MSB** | **DMRS port** | **Value of LSB** | **DMRS port** | | 0 | 1st DMRS port which shares PTRS port 0 | 0 | 1st DMRS port which shares PTRS port 1 | | 1 | 2nd DMRS port which shares PTRS port 0 | 1 | 2nd DMRS port which shares PTRS port 1 | | 2 | 3rd DMRS port which shares PTRS port 0 | 2 | 3rd DMRS port which shares PTRS port 1 | | 3 | 4th DMRS port which shares PTRS port 0 | 3 | 4th DMRS port which shares PTRS port 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **Proposed changed (Section 7.3.1.1.2)**  **Table 7.3.1.1.2-26A: PTRS-DMRS association for UL PTRS ports 0 and 1, *maxRank>4***   |  |  |  |  | | --- | --- | --- | --- | | **Value of 2 MSBs** | **DMRS port** | **Value of 2 LSBs** | **DMRS port** | | 0 | 1st DMRS port which shares PTRS port 0 | 0 | 1st DMRS port which shares PTRS port 1 | | 1 | 2nd DMRS port which shares PTRS port 0 | 1 | 2nd DMRS port which shares PTRS port 1 | | 2 | 3rd DMRS port which shares PTRS port 0 | 2 | 3rd DMRS port which shares PTRS port 1 | | 3 | 4th DMRS port which shares PTRS port 0 | 3 | 4th DMRS port which shares PTRS port 1 | |   **Comment#2**  The indexes of several DMRS indication rows should be reordered as listed as following:   * In Table 7.3.1.2.2-9, rows 35-55 should be reordered as rows 33-53. * In Table 7.3.1.2.2-9A, rows 35-56 should be reordered as rows 33-54. * In Table 7.3.1.2.2-10, rows 129-136 should be reordered as rows 128-137. * In Table 7.3.1.2.2-10A, rows 129-137 should be reordered as rows 128-136, respectively. | |

## Enhanced uplink transmission

Please provide your comments/suggestions on enhanced uplink transmission here, including UL precoding indication for multi-panel transmission and SRI/TPMI enhancement for enabling 8TX UL transmission.

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| *Company* | *View* |
| Editor | The changes are marked with author “Yan Cheng\_post RAN1#114” on top of the version R1-2306315 endorsed in RAN1#113, which are to reflect the agreements RAN1#114. |
| QC (STxMP) | **Comment 1**: Based on the following agreement in RAN1 #114, the multi-DCI based STxMP PUSCH+PUSCH is enabled by a new RRC configuration (“enableSTx2PofmDCI”) in addition to configurations of two coresetPoolIndex values and two SRS resource sets. We suggest to also add this condition in various places where multi-DCI based STxMP PUSCH+PUSCH is discussed.  **Agreement**   * Regarding how to configure multi-DCI based STxMP PUSCH+PUSCH in RRC, * Introduce a new RRC parameter to indicate the multi-DCI based STxMP PUSCH+PUSCH. The multi-DCI based STxMP PUSCH+PUSCH is configured when the new RRC parameter is configured, two different *coresetPoolIndex* values are configured and two SRS resource sets for CB/NCB are configured.   When multi-DCI based STxMP PUSCH+PUSCH is configured, the DCI field SRS resource set indicator is not present.  **Comment 2**: The last codepoint of SRS resource set indicator in Table 7.3.1.1.2-36 should be reserved / not used for SDM/SFN schemes based on the following agreement. A note can be added to the Table to capture this.  **Agreement**  When the single-DCI based PUSCH SDM/SFN is configured, the codepoint ‘11’ of the DCI field SRS resource set indicator is reserved.  **Comment 3**: In Section 7.3.1.1.3 (DCI format 0\_2), there are a couple of instances (copied below), where instead of DCI format 0\_2, DCI format 0\_1 is mentioned (typo):  - is the number of configured SRS resources in the SRS resource set associated with the *coresetPoolIndex* value for the CORESET used for the PDCCH carrying the DCI format 0\_1, if the UE is not provided *coresetPoolIndex* or is provided *coresetPoolIndex* with value 0 for the first CORESETs, and is provided *coresetPoolIndex* with value 1 for the second CORESETs,  **…**  When the UE is not provided *coresetPoolIndex* or is provided *coresetPoolIndex* with value 0 for the first CORESETs, and is provided *coresetPoolIndex* with value 1 for the second CORESETs, and there are two SRS resource sets configured by *srs-ResourceSetToAddModListDCI-0-2* and associated with *usage* of value '*codebook*' or '*nonCodeBook*', the Precoding information and number of layers field is associated with the SRS resource set that is associated with the *coresetPoolIndex* value for the CORESET used for the PDCCH carrying the DCI format 0\_1.  **Comment 4**: Some of the editor’s notes may not be needed anymore given the outcome of RAN1 #114, like the followings notes:  “Editor’s note: No agreement on “11” yet, will further update later if needed depending on further agreement”  “Editor’s note: There is no agreement on what to do when *multipanelScheme* is configured to *sfnScheme. Further update will be done once there is further agreement.*” |
| MediaTek (STxMP) | Thanks for your great effort on the draft CR. Please find our comments bellow. 7.3.1.1.2 Format 0\_1& 7.3.1.1.3 Format 0\_2 **Comment:**  Based on RAN1 agreement, multi-DCI based STxMP PUSCH+PUSCH is configured/enabled by the new RRC parameter. Therefore, the presence of SRS resource set indicator should depend on not only the configuration of *coresetPoolIndex* but also the new RRC parameter.Thus, we suggest the following changes to DCI format 0\_1 and 0\_2:   |  | | --- | | - SRS resource set indicator – 0 or 2 bits  - 2 bits according to Table 7.3.1.1.2-36 if  - *txConfig = nonCodeBook*, and there are two SRS resource sets configured by *srs-ResourceSetToAddModList* and associated with the *usage* of value '*nonCodeBook*', and is not configured with *coresetPoolIndex* or the value of *coresetPoolIndex* is the same for all CORESETs if *coresetPoolIndex* is provided, and the higher layer parameter *enableSTx2PofmDCI* is not configured or  - *txConfig*=*codebook*, and there are two SRS resource sets configured by *srs-ResourceSetToAddModList* and associated with *usage* of value '*codebook*', and is not configured with *coresetPoolIndex* or the value of *coresetPoolIndex* is the same for all CORESETs if *coresetPoolIndex* is provided, and the higher layer parameter *enableSTx2PofmDCI* is not configured;  - 0 bit otherwise. | |
| ZTE (STxMP) | Thanks for editor’s effort on this CR.  **Comment#1**  In section 7.3.1.1.3, “DCI format 0\_1” should be changed to “DCI format 0\_2”. Hence we have the following suggestion.   |  | | --- | | **Proposed change (section 7.3.1.1.3) :**  ...  - bits according to Tables 7.3.1.1.2-32 if the higher layer parameter *txConfig = codebook*, where  - is the number of configured SRS resources in the SRS resource set indicated by SRS resource set indicator field if present,  - is the number of configured SRS resources in the SRS resource set associated with the *coresetPoolIndex* value for the CORESET used for the PDCCH carrying the DCI format 0\_2~~1~~, if the UE is not provided *coresetPoolIndex* or is provided *coresetPoolIndex* with value 0 for the first CORESETs, and is provided *coresetPoolIndex* with value 1 for the second CORESETs,  - otherwise is the number of configured SRS resources in the SRS resource set configured by higher layer parameter *srs-ResourceSetToAddModListDCI-0-2* and associated with the higher layer parameter *usage* of value '*codeBook*', where the SRS resource set is composed of the first SRS resources together with other configurations in the SRS resource set configured by higher layer parameter *srs-ResourceSetToAddModList*, if any, and associated with the higher layer parameter *usage* of value '*codeBook*', except for the higher layer parameters *'srs-ResourceSetId' and 'srs-ResourceIdList'*.  ...  When the UE is not provided *coresetPoolIndex* or is provided *coresetPoolIndex* with value 0 for the first CORESETs, and is provided *coresetPoolIndex* with value 1 for the second CORESETs, and there are two SRS resource sets configured by *srs-ResourceSetToAddModListDCI-0-2* and associated with *usage* of value '*codebook*' or '*nonCodeBook*', the Precoding information and number of layers field is associated with the SRS resource set that is associated with the *coresetPoolIndex* value for the CORESET used for the PDCCH carrying the DCI format 0\_2~~1~~.  ... | |
| ZTE (8Tx) | Thanks for editor’s effort on this CR.  **Comment #1**  In section 7.3.1.1.2 for DCI Format 0\_1 of the draft CR, there are several descriptions on transform precoder is enabled for 8Tx as shown below.   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | - Precoding information and number of layers – number of bits determined by the following:  - 0 bits if the higher layer parameter *txConfig = nonCodeBook*;  - 0 bits for 1 antenna port and if the higher layer parameter *txConfig = codebook*;  ...  - 7 bits according to Table 7.3.1.1.2-5B for 8 antenna ports, if *CodebookType*=*Codebook1,* transform precoder is disabled, *maxRank* = *8*, and according to *ULcodebookFC-N1N2*;  - 7 bits according to Table 7.3.1.1.2-5C for 8 antenna ports, if *CodebookType*=*Codebook1*, transform precoder is disabled, *maxRank* =7, and according to *ULcodebookFC-N1N2;*  - 7 bits according to Table 7.3.1.1.2-5D for 8 antenna ports, if *CodebookType*=*Codebook1*, transform precoder is disabled, *maxRank* =4, 5 or 6, and according to *maxRank;*  - 4, 6 or 7 bits according to Table 7.3.1.1.2-5E for 8 antenna ports, if *CodebookType*=*Codebook1*, transform precoder is enabled or *maxRank* =2 or 3 if transform precoder is disabled, and according to transform precoder and *maxRank*;  - 8 bits according to Table 7.3.1.1.2-5F for 8 antenna ports, if *CodebookType*=*Codebook4,* transform precoder is disabled, *maxRank*=5, 6, 7 or 8, and according to *maxRank;*  - 6 or 7 or 8 bits according to Table 7.3.1.1.2-5G for 8 antenna ports, if *CodebookType*=*Codebook4,* transform precoder is disabled, *maxRank*=2, 3 or 4, and according to *maxRank;*  - 3 bits according to Table 7.3.1.1.2-5H for 8 antenna ports, if *CodebookType*=*Codebook4,* transform precoder is enabled.  ...  **Table 7.3.1.1.2-5E: Precoding information and number of layers, for 8 antenna ports, if transform precoder is enabled or *maxRank*=2 or 3 if transform precoder is disabled, *CodebookType=Codebook1, ULcodebookFC-N1N2 = (4,1) or (2,2)***   |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | Bit field mapped to index | transform precoder is disabled or enabled, *maxRank*=1 | Bit field mapped to index | transform precoder is ~~enabled~~disabled, and *maxRank*=2 | Bit field mapped to index | transform precoder is ~~enabled~~disabled, and *maxRank=3* | | 0 | 1 layer: TPMI=0 | 0 | 1 layer: TPMI=0 | 0 | 1 layer: TPMI=0 | | 1 | 1 layer: TPMI=1 | 1 | 1 layer: TPMI=1 | 1 | 1 layer: TPMI=1 | | … | … | … | … | … | … | | 15 | 1 layer: TPMI=15 | 15 | 1 layer: TPMI=15 | 15 | 1 layer: TPMI=15 | |  |  | 16 | 2 layer2: TPMI=0 | 16 | 2 layer2: TPMI=0 | |  |  | 17 | 2 layer2: TPMI=1 | 17 | 2 layer2: TPMI=1 | |  |  | … | … | … | … | |  |  | 47 | 2 layers: TPMI=31 | 47 | 2 layers: TPMI=31 | |  |  | 48-63 | reserved | 48 | 3 layers: TPMI=0 | |  |  |  |  | 49 | 3 layers: TPMI=1 | |  |  |  |  | … | … | |  |  |  |  | 71 | 3 layers: TPMI=23 | |  |  |  |  | 72-127 | reserved |   **...**  **Table 7.3.1.1.2-5H: Precoding information and number of layers, for 8 antenna ports, if transform precoder is enabled or disabled, and *CodebookType=Codebook4***   |  |  | | --- | --- | | Bit field mapped to index | Precoding information and number of layers | | 0 | 1 layer: TPMI=0 | | … | … | | 7 | 1 layer: TPMI=7 | |   To our understanding, it has not been discussed 8Tx precoder when transform precoding is enabled. According to the current draft CR for 38.211 as shown below, it was assumed that:   * single layer precoder of Ng=1 and Ng=8 can be supported when transform precoding is enabled or disabled with same set of precoders, * for more than one layer, only disabled transform precoding is supported, as in legacy.  |  | | --- | | Table 6.3.1.5-9: Precoding matrix type (4,1) with one antenna group for single-layer transmission using eight antenna ports.  ...  Table 6.3.1.5-10: Precoding matrix type (4,1) with one antenna group for two-layer transmission using eight antenna ports with transform precoding disabled.  ...  Table 6.3.1.5-16: Precoding matrix type (4,1) with one antenna group for eight-layer transmission using eight antenna ports with transform precoding disabled.  ...  Table 6.3.1.5-47: Precoding matrix with 8 antenna groups for transmission using eight antenna ports. Up to 8 layers are supported with transform precoding disabled and up to one layer with transform precoding enabled.  ... |   So we suggest to modify the above mentioned parts to reflect same principles (red text above) as in 38.211 for the case when transform precoding enabled.  **Comment #2**  In section 7.3.1.1.2 for DCI Format 0\_1 of the draft CR, it seems that the scheme highlighted below as defined in Table 7.3.1.1.2-29B cannot match the legacy scheme, so it is not directly extended based on legacy scheme.   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Table 7.3.1.1.2-29B: SRI indication, for non-codebook based PUSCH transmission, ,   |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | | Bit field mapped to index | SRI(s), | Bit field mapped to index | SRI(s), | Bit field mapped to index | SRI(s), | Bit field mapped to index | SRI(s), | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | | 5 |  | 5 | 5 | 5 | 5 | 5 | 5 | | … | … | 6 |  | 6 | 6 | 6 | 6 | | 14 |  | … | … | 7 |  | 7 | 7 | | 15 | reserved | 20 |  | … | … | 8 |  | |  |  | 21-31 | reserved | 27 |  | … | … | |  |  |  |  | 28-31 | reserved | 35 |  | |  |  |  |  |  |  | 36-63 | reserved | | where a bit field value (B) is mapped to SRIs by the following, where is the number of layers:    For  Find the largest in Table 5.2.2.2.5-4 of [6, TS 38.214] such that | | | | | | | | |   For Nsrs = 4, Lmax = 4, the orders are different between the legacy scheme and the one in draft CR.    For other Nsrs > 4, e.g, Nsrs =5,    So we suggest to adopt an enumerated scheme for mapping SRI to the SRS resource combinations in TS 38.212 on the top of the endorsed CR, instead of an explicit formula which has not been agreed. E.g., as follows.  Likewise, other cases can take the same formula to the indicated SRS combinations for NCB PUSCH in Table 7.3.1.1.2-29B/29C/30B/30C/31B/31C/31D/31E/31F/31G/31H/31I/31J/31K.  **Table 1** Enumerated SRS resource combinations for each SRI value   |  |  | | --- | --- | | Bit field mapped to index | SRS resource index(es), | | 0 | 0 | | 1 | 1 | | ... | ... | | 7 | 7 | | 8 | 0, 1 | | 9 | 0, 2 | | ... | ... | | 14 | 0, 7 | | ... | ... | | 35 | 6,7 | | 36 | 0, 1, 2 | | 37 | 0, 1, 3 | | ... | ... | | 41 | 0, 1, 7 | | 42 | 0, 2, 3 | | 43 | 0, 2, 4 | | ... | ... | | 46 | 0, 2, 7 | | ... | ... | | 91 | 5, 6, 7 | | 92 | 0, 1, 2, 3 | | 93 | 0, 1, 2, 4 | | ... | ... | | 161 | 4, 5, 6, 7 | | 162 | 0, 1, 2, 3, 4 | | 163 | 0, 1, 2, 3, 5 | | ... | ... | | 217 | 3, 4, 5, 6, 7 | | 218 | 0, 1, 2, 3, 4, 5 | | 219 | 0, 1, 2, 3, 4, 6 | | ... | ... | | 245 | 2, 3, 4, 5, 6, 7 | | 246 | 0, 1, 2, 3, 4, 5, 6 | | 247 | 0, 1, 2, 3, 4, 5, 7 | | ... | ... | | 253 | 1, 2, 3, 4, 5, 6, 7 | | 254 | 0-7 | | 255 | reserved | |
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# Second round discussions

TBD