**3GPP TSG-RAN WG1 Meeting #114 R1-23xxxxx**

**Toulouse, France, 21-25 August, 2023**

**Agenda Item: 9.17**

**Source: Moderator (Huawei)**

**Title: Summary of email discussion [Post114-38.212-NR\_MIMO\_evo\_DL\_UL]**

**Document for: Discussion and Decision**

# Introduction

This document summarizes the discussions on the 38.212 draft CR on NR MIMO Evolution for Downlink and Uplink, and aims to stabilize the 38.212 draft CR.

[Post114-38.212-NR\_MIMO\_evo\_DL\_UL] Email discussion on Rel-18 draft CRs by September 7 – Editors

# First round discussions

This section summarize the first round email discussions on draft CR v00. Companies are encouraged to provide the first round views by 09/05 (Tuesday), 6:00am UTC, then we can update the draft CR accordingly for the next step discussions.

## Multi-TRP enhancements

Please provide your comments/suggestions on Multi-TRP enhancements here, including unified TCI framework and two TAs for multi-DCI.

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| *Company* | *View* |
| Editor | The changes are marked with author “Yan Cheng\_post RAN1#114” on top of the version R1-2306315 endorsed in RAN1#113, which are to reflect the agreements RAN1#114. |
| QC | For two TAs for multi-DCI, our understanding is that the following agreements should be implemented in 38.212, Section 7.3.1.2.1 (DCI format 1\_0, the part that describes PDCCH order):**Agreement (RAN1 #114)**For inter-cell multi-DCI based Multi-TRP operation with two TA enhancement, support indication of additionalPCI in the PDCCH order* as baseline capability: support PRACH triggering towards servingCell PCI or active additionalPCI.

**Agreement (RAN1 #112-b)**For intercell multi-DCI based Multi-TRP operation with two TA enhancement, support indication of which PRACH configuration to be used in the RACH procedure in the PDCCH order.* FFS: Whether *additionalPCI* or a generic identifier is indicated in PDCCH order
* FFS: The detail of the indication in PDCCH order in terms of whether to support PRACHtriggered for inactive *additionalPCI*.
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| Samsung | We would like to suggest the following change to unify the field(s) name in 1\_1 and 1\_2.

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| 7.3.1.2.2 Format 1\_1- TCI ~~states~~ selection – 0 bit if higher layer parameter *tciSelection-PresentInDCI* is not enabled; otherwise 2 bits according to Table 7.3.1.2.2-11.  |

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## CSI enhancements

Please provide your comments/suggestions on CSI enhancements here, including CSI enhancement for high/medium UE velocities and coherent JT (CJT).

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| *Company* | *View* |
| Editor | The changes are marked with author “Yan Cheng\_post RAN1#114” on top of the version R1-2306315 endorsed in RAN1#113, which are to reflect the agreements RAN1#114. |
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## Reference signal enhancement

Please provide your comments/suggestions on Reference signal enhancements here, including increased number of orthogonal DMRS ports and SRS enhancements.

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| *Company* | *View* |
| Editor | The changes are marked with author “Yan Cheng\_post RAN1#114” on top of the version R1-2306315 endorsed in RAN1#113, which are to reflect the agreements RAN1#114. |
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## Enhanced uplink transmission

Please provide your comments/suggestions on enhanced uplink transmission here, including UL precoding indication for multi-panel transmission and SRI/TPMI enhancement for enabling 8TX UL transmission.

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| *Company* | *View* |
| Editor | The changes are marked with author “Yan Cheng\_post RAN1#114” on top of the version R1-2306315 endorsed in RAN1#113, which are to reflect the agreements RAN1#114. |
| QC (STxMP) | **Comment 1**: Based on the following agreement in RAN1 #114, the multi-DCI based STxMP PUSCH+PUSCH is enabled by a new RRC configuration (“enableSTx2PofmDCI”) in addition to configurations of two coresetPoolIndex values and two SRS resource sets. We suggest to also add this condition in various places where multi-DCI based STxMP PUSCH+PUSCH is discussed.**Agreement*** Regarding how to configure multi-DCI based STxMP PUSCH+PUSCH in RRC,
* Introduce a new RRC parameter to indicate the multi-DCI based STxMP PUSCH+PUSCH. The multi-DCI based STxMP PUSCH+PUSCH is configured when the new RRC parameter is configured, two different *coresetPoolIndex* values are configured and two SRS resource sets for CB/NCB are configured.

When multi-DCI based STxMP PUSCH+PUSCH is configured, the DCI field SRS resource set indicator is not present.**Comment 2**: The last codepoint of SRS resource set indicator in Table 7.3.1.1.2-36 should be reserved / not used for SDM/SFN schemes based on the following agreement. A note can be added to the Table to capture this.**Agreement**When the single-DCI based PUSCH SDM/SFN is configured, the codepoint ‘11’ of the DCI field SRS resource set indicator is reserved.**Comment 3**: In Section 7.3.1.1.3 (DCI format 0\_2), there are a couple of instances (copied below), where instead of DCI format 0\_2, DCI format 0\_1 is mentioned (typo):- $N\_{SRS}$ is the number of configured SRS resources in the SRS resource set associated with the *coresetPoolIndex* value for the CORESET used for the PDCCH carrying the DCI format 0\_1, if the UE is not provided *coresetPoolIndex* or is provided *coresetPoolIndex* with value 0 for the first CORESETs, and is provided *coresetPoolIndex* with value 1 for the second CORESETs,**…**When the UE is not provided *coresetPoolIndex* or is provided *coresetPoolIndex* with value 0 for the first CORESETs, and is provided *coresetPoolIndex* with value 1 for the second CORESETs, and there are two SRS resource sets configured by *srs-ResourceSetToAddModListDCI-0-2* and associated with *usage* of value '*codebook*' or '*nonCodeBook*', the Precoding information and number of layers field is associated with the SRS resource set that is associated with the *coresetPoolIndex* value for the CORESET used for the PDCCH carrying the DCI format 0\_1.**Comment 4**: Some of the editor’s notes may not be needed anymore given the outcome of RAN1 #114, like the followings notes:“Editor’s note: No agreement on “11” yet, will further update later if needed depending on further agreement”“Editor’s note: There is no agreement on what to do when *multipanelScheme* is configured to *sfnScheme. Further update will be done once there is further agreement.*” |
| MediaTek (STxMP) | Thanks for your great effort on the draft CR. Please find our comments bellow.7.3.1.1.2 Format 0\_1& 7.3.1.1.3 Format 0\_2**Comment:** Based on RAN1 agreement, multi-DCI based STxMP PUSCH+PUSCH is configured/enabled by the new RRC parameter. Therefore, the presence of SRS resource set indicator should depend on not only the configuration of *coresetPoolIndex* but also the new RRC parameter.Thus, we suggest the following changes to DCI format 0\_1 and 0\_2:

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| - SRS resource set indicator – 0 or 2 bits- 2 bits according to Table 7.3.1.1.2-36 if - *txConfig = nonCodeBook*, and there are two SRS resource sets configured by *srs-ResourceSetToAddModList* and associated with the *usage* of value '*nonCodeBook*', and is not configured with *coresetPoolIndex* or the value of *coresetPoolIndex* is the same for all CORESETs if *coresetPoolIndex* is provided, and the higher layer parameter *enableSTx2PofmDCI* is not configured or- *txConfig*=*codebook*, and there are two SRS resource sets configured by *srs-ResourceSetToAddModList* and associated with *usage* of value '*codebook*', and is not configured with *coresetPoolIndex* or the value of *coresetPoolIndex* is the same for all CORESETs if *coresetPoolIndex* is provided, and the higher layer parameter *enableSTx2PofmDCI* is not configured;- 0 bit otherwise. |

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# Second round discussions

TBD