**3GPP TSG RAN WG1 Meeting #110-bis-e R1-220xxxx**

**e-Meeting, October 10 – 19, 2022**

**Source: Moderator (Intel Corporation)**

**Title: Summary of issues on initial access aspect of NR extension up to 71 GHz**

**Agenda item: 8.2**

**Document for: Discussion**

# Introduction

In this contribution, moderator summarizes discussions on remaining issues related to initial access for extending NR up to 71 GHz based submitted contributions from RAN1 #110-bis-e.

# Summary of issues

## 2.1 (Issue 1) No CD-SSB frequency indication using NCD-SSB

### Summary of Discussions

LGE asserts that range that indicates that there is no CD-SSB within a GSCN range is small.

If a UE detects NCD-SSB in FR2 and determines that a CORESET for Type0-PDCCH CSS set is not present by , the UE determines that there is no CD-SSB within a GSCN range where and are up to 16, which is suggested to be too narrow for FR2-2.

Proposes TP#1-1.

### List of TPs

#### TP #1-1 (TS38.213) [R1-2209436]

|  |
| --- |
| **Reason for change**: If a UE detects NCD-SSB in FR2 and determines that a CORESET for Type0-PDCCH CSS set is not present by , the UE determines that there is no CD-SSB within a GSCN range where and are up to 16, which is too narrow for FR2-2 case.  **Summary of change:** Introduce a factor of step size to indicate GSCN ranges where CD-SSB does not exist by using NCD-SSB.  **Consequences if not approved:** The network can indicate only limited scope of GSCN ranges where CD-SSB does not exist by using NCD-SSB. |
| 13 UE procedure for monitoring Type0-PDCCH CSS sets  **<Unchanged parts are omitted>**  If a UE detects a SS/PBCH block and determines that a CORESET for Type0-PDCCH CSS set is not present, and for for FR1 or for for FR2, the UE determines that there is no SS/PBCH block having an associated Type0-PDCCH CSS set within a GSCN range where in FR1 and FR2-1, 3 in FR2-2. and are respectively determined by *controlResourceSetZero* and *searchSpaceZero* in *pdcch-ConfigSIB1*. If the GSCN range is , the UE determines that there is no information for a second SS/PBCH block with a CORESET for an associated Type0-PDCCH CSS set on the detected SS/PBCH block. |

### Comments from Companies

Please comment on TP#1-1

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | We don’t think this TP is needed. No CD-SSB frequency indication using NCD-SSB doesn’t require a full frequency range indication even in Rel-15, which is the essential difference from the CD-SSB indication using NCD-SSB discussed in the last meeting. The indication range is only [-15, 15], and fixed for all SCSs, and it also applies to the bands with sync interval larger than 1 in FR1 and FR2-1. In this sense, we didn’t see an essential need for enhancement, and would like to maintain the same UE behavior as FR1 and FR2-2. |
| ZTE, Sanechips | In our opinion, it is also feasible if no optimization is made. But if making above change, it is consistent with the approved CR in last meeting and the complexity of UE detection may be improved. |
| LG Electronics | From Rel-15, frequency indication by using NCD-SSB provides two tools. One is to indicate the location of CD-SSB around NCD-SSB while the other is to indicate a GSCN range where there is no CD-SSB.  In the last meeting, we agreed to introduce step size 3 for the former case (i.e., CD-SSB indication). TP#1-1 is proposing to introduce step size 3 as well for the latter case (i.e., no CD-SSB indication).  As Samsung pointed out, the design principle of the latter case is not to cover whole frequency band (differently from the former case). However, considering the interval between adjacent GSCNs is multiple integer of 3 in FR2-2, it would make sense to apply the same step size 3 for both cases, which can make specification more consistent for FR2-2. |
| vivo | We are fine with this change that is consistent with the approved CR. |
| Intel | While we don’t think the CR is critical. We would be ok to accept the changes to make the raster granularity consistent with indicated SSB case. |
| Ericsson | We support the TP and share the same view as LGE. This achieves consistency from the CR from last meeting. |
| Huawei, HiSilicon | It is an optimization change. We are fine with the change if majority support. |

### Summary of Offline Discussions

TDB

# Summary of Proposed Agreements/Conclusions by Moderator

To be filled after discussions in RAN1 #110-bis-e.

# Summary of Agreements/Conclusions from RAN1 #110

To be filled once agreements and conclusion are made available at the end of the meeting.

# Reference

1. R1-2209436, Draft CR for indicating GSCN ranges where CD-SSB does not exist using NCD-SSB in FR2-2, LG Electronics
2. R1-2209437, Discussion on how to indicate GSCN ranges where CD-SSB does not exist using NCD-SSB in FR2-2, LG Electronics

# List of RAN1 Agreements on initial access

## RAN1 #104-e

**R1-2102073** [Draft] LS on beam switching gap for 60 GHz band Intel Corporation

Final LS endorsed in R1-2102202

Agreement:

Send an LS to RAN4 to get input on gap required for gNBs and UEs for beam switching and for UL/DL and DL/UL switching.

Agreement:

Whether or not to support 240 kHz, 480kHz and 960kHz SCS for SSB and the conditions under which SSB for 240 kHz, 480 kHz and 960 kHz may be supported will be decided no later than RAN1#104bis-e.

Agreement:

For an unlicensed band that requires LBT, further study whether/how to support discovery burst (DB) and discovery burst transmission window (DBTW) at least for 120 kHz SSB SCS

* If DB supported
  + FFS: What signals/channels are included in DB other than SS/PBCH block
* If DBTW is supported
  + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs
    - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.
  + PBCH payload size is no greater than that for FR2
  + Duration of DBTW is no greater than 5 ms
  + Number of PBCH DMRS sequences is the same as for FR2
* The following points are additionally FFS:
  + How to indicate candidate SSB indices and QCL relation without exceeding limit on PBCH payload size
  + Details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands
  + Whether or not to support DBTW for SSB SCS(s) other than 120 kHz if other SSB SCS(s) are supported

Agreement:

For CORESET#0 and Type0-PDCCH search space configured in MIB:

* Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {120, 120} kHz
  + Support at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 for {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz.
    - FFS: Supporting additional values
  + FFS: Supported values for SSB to CORESET#0 offset RBs
* If 480kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {480, 480} kHz
* If 960 kHz SSB SCS that configures CORESET#0 and Type0-PDCCH CSS in MIB is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {960, 960} kHz
* If 240 kHz SSB SCS is agreed to be supported,
  + Support {SS/PBCH Block, CORESET#0 for Type0-PDCCH} SCS equal to {240, 120} kHz
* FFS: any other combinations between one of SSB SCS (120, 240, 480, 960) and one of CORESET#0 SCS (120, 480, 960)
  + FFS: initial timing resolution based on low SCS (120 kHz) and its impact on the performance of higher SCS (480/960 kHz)

Agreement:

For 480 kHz and 960 kHz SSB SCS (if agreed)

* Study further on reserving symbol gap between SSB positions with different SSB index (and possibly between SSB position and other signal/channels)
  + FFS: whether symbol gap is needed for only 960 kHz or both 480 and 960 kHz.
* Study further on reserving gap for UL/DL switching within the pattern accounting possibility for reserving UL transmission occasions in the SSB pattern
* Study should account for inputs from RAN4

Agreement:

* For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2.
* For non-initial access use cases,
  + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.
    - FFS: support of sequence length L = 571, 1151
* FFS: Support of 480 and/or 960 kHz PRACH SCS for initial access use cases, if 480 and/or 960 kHz SSB SCS is agreed to be supported for initial access

Agreement:

If 480 and/or 960 kHz PRACH SCS is supported, RAN1 should study whether or not the current RA-RNTI calculation and PRACH identification in RAR correctly provides unique identification of PRACH.

## RAN1 #104-bis-e

Agreement:

For the case where SSB location and SCS are explicitly provided to the UE (non-initial access) and SSB does not configure Type-0 PDCCH, support 480 kHz and 960 kHz numerologies for the SSB

* Note: Strive to minimize specification impact due to the new SCS for SSB

Agreement:

* For operation with shared spectrum channel access of NR 52.6 – 71 GHz, support discovery burst (DB) and define the DB same as in Rel-16 37.213 Section 4.0
* FFS: Support discovery burst transmission window (DBTW) at least for SSB with 120 kHz SCS with the following requirements
  + PBCH payload size is no greater than that for FR2
  + Duration of DBTW is no greater than 5 ms
  + Number of PBCH DMRS sequences is the same as for FR2
  + FFS: applicability of DBTW design for 120kHz to SSB with 480kHz and 960kHz SCS
  + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs
    - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.
    - FFS: details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands
    - FFS: details of how to inform UEs of the configuration of DBTW

Agreement:

For SSB with 120kHz SCS for NR 52.6 GHz to 71 GHz,

* 120 kHz SCS: the first symbols of the candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
* For carrier frequencies within 52.6 GHz to 71GHz, support at least 𝑛 = 0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18.
  + Other values of *n* (if any) are FFS, and support of additional n values are subject to support of DBTW for 120kHz SSB

Agreement:

* PRACH configuration for 480/960 kHz SCS (if agreed)
  + The minimum PRACH configuration period is 10 ms (as in FR2)
  + For RO configuration for PRACH with 480/960kHz SCS,
    - FFS: details of how to configure the 480/960 kHz PRACH ROs using [60 or 120 kHz] reference slot considering at least:
      * location of 480/960 kHz PRACH slot per reference slot
      * location of duration containing 480/960khz PRACH slot pattern within 10ms
      * potential impact to RA-RNTI calculation

## RAN1 #105-e

Agreement:

For 480kHz/960kHz SSB, select one of the following alternatives:

* ALT 1) First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
  + value of X and Y are identical for 480kHz and 960kHz
    - FFS: exact value of X and Y
* ALT 2) First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
* Values of n for 480kHz and 960kHz for ALT 1 and 2
  + FFS: whether number of values for ‘n’ depend on LBT operation (i.e. LBT vs no-LBT)
  + FFS: exact values of ‘n’ for each SCS
  + Values of ‘n’ for one mode of operation shall be strictly a subset of values for another mode of operation, if two mode of operation exist for number of candidate SSBs
  + FFS: whether values of ‘n’ shall not be all consecutive integer values (i.e. non-candidate SSB slots are positioned every few candidate SSB slots)

Proposal:

In addition to 120kHz, support **480** kHz SSB for initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with following constraints.

* Limited sync raster entry numbers
  + It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than 665 (Note: the total number of synchronization raster entries in FR2 for band n259 + n261 is 602). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.
* only 480kHz CORESTE#0/Type0-PDCCH SCS supported for 480 kHz SSB SCS.
* SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible

Formal objection sustained by: Huawei, MediaTek (would like to discuss at next meeting)

Proposal:

In addition to 120kHz, support **both** **480 and 960** kHz SSB for initial access with support of CORESET0/Type0-PDCCH configuration in the MIB with following constraints.

* Limited sync raster entry numbers
  + It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than 665 (Note: the total number of synchronization raster entries in FR2 for band n259 + n261 is 602). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.
* only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS i.e., (480,480) and (960,960).
* SSB time domain candidate resource pattern (within a slot or pair of slots) for 480 and 960kHz SSB are identical
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible

Formal objection sustained by: Huawei, MediaTek (object to 960 kHz)

Proposal:

To support ANR and PCI confusion detection for 480/960kHz SCS based SSB, support CORESET#0/Type0-PDCCH configuration in MIB of 480 and 960kHz SSB

* FFS: additional method(s) to enable support to obtain neighbor cell PCI and SIB1 contents related to CGI reporting
* Only 1 CORESTE#0/Type0-PDCCH SCS supported for each SSB SCS, i.e., (480,480) and (960,960).
* Prioritize support SSB-CORESET0 multiplexing pattern 1. Other patterns discussed on a best effort basis.
* Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible
* Note: From UE perspective, ANR detection for 480/960kHz SCS based SSB is not supported if the UE does not support 480/960 SCS for SSB.
* Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.

Formal objection sustained by: Huawei

Agreement:

For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access)

* Support configuring CORESET#0/Type0-PDCCH for the purpose of ANR/PCI confusion detection by down selecting from the following two alternatives
  + Alt 1) Using dedicated signaling
  + Alt 2) Using configuration in MIB
    - Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.

Agreement:

For 480kHz and 960kHz PRACH,

* Down-select among option 1 and 2
  + Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
    - FFS: supported values of the starting PRACH slot index within reference slot and whether or not the ROs for a given PRACH configuration can span more than one PRACH slot if gaps between consecutive ROs are supported for LBT and/or beam switching purposes
  + Option 2) Each 120kHz RO corresponds to 4 and 8 candidate RO positions for 480kHz and 960kHz PRACH, respectively. Information about the number and locations of 480/960kHz candidate RO(s) are configured or pre-selected within each 120kHz RO. The reference 120kHz RO is determined by the current PRACH configuration method in Rel-15/16 specification.
* Following alternatives are considered on PRACH density
  + ALT 1) At least the same density (i.e. number of PRACH slots per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: support for higher PRACH slot density (number of PRACH slots per reference slot)
  + ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - FFS: support for higher RO density
  + An “example” illustration of PRACH slots for 480/960kHz is shown below:



* FFS: whether and how to account for LBT in RO configuration (if needed)
* FFS: whether and how to account for beam switching gap in RO configuration (if needed)

Agreement:

FFS: Support DBTW at least for 120kHz

* FFS whether DBTW will be applicable for 480/960 kHz SSB SCS
  + If DBTW is supported for 480/960kHz SSB:
    - For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access), indication of DBTW configuration (e.g. enable/disable of DBTW,  , and DBTW length) are supported by dedicated signaling.
* For 120kHz SSB, support mechanism to distinguish at least the following scenarios:
  + Case 1) (Unlicensed with LBT off) + DBTW disabled
  + Case 2) (Unlicensed with LBT on) + DBTW enabled
  + Case 3) (Unlicensed with LBT on) + DBTW disabled
  + Case 4) (Licensed) + DBTW disabled
  + FFS: Whether/how LBT on/off is indicated in MIB
    - If not indicated in MIB, then FFS whether/how the UE determines different sizes of DCI 1\_0 with CRC scrambled by SI-RNTI
  + FFS: whether any case(s) can be combined for DBTW signaling design and how to handle implications to DCI 1\_0 size ambiguity if is not distinguished in signaling
  + FFS: whether all above cases need an explicit indication
  + FFS: Whether a single indication can be used for combination of more than one cases
* For 120 kHz SSB, enable/disable of DBTW is indicated by one or more of the following methods:
  + Option 1) signaling in MIB
    - Option 1-1) disabling DBTW is jointly coded with
    - Option 1-2) indicated by other bit fields in MIB
    - FFS: among options 1-1 and 1-2
  + Option 2) distinct GSCN used by the SSB
  + Option 3) By comparing the value of  in MIB and DBTW length after UE reads SIB1 or by comparing the value of  in MIB and default DBTW length of 5 ms before UE reads SIB1.
  + FFS: whether to support option 1, 2, 3, or any combination of the options.
  + Note: enable/disable signaling of DBTW by MIB or GSCN does not preclude other signaling methods

Agreement:

If DBTW is supported,

* Working assumption: MIB signaling to support
  + Alt A) indication of at least for 120kHz SSB
    - In this case, the total number of values of to not exceed 4
  + Alt B) Explicit indication of SSB index and/or SSB candidate location
    - FFS on the details of signaling
  + FFS betweenAlt A, or B, or supporting both
* Supported DBTW lengths
  + Alt 1) 0.5, 1, 2, 3, 4, 5 msec
    - Note: same as Rel-16 FR1 NR-U
  + Alt 2) maximum 5 msec
    - FFS other values
  + FFS between Alt 1 and 2
* Number of candidate positions when DBTW is enabled
  + For 120kHz SSB
    - FFS between 64 or 80
  + If DBTW is additionally supported for 480/960kHz SSB
    - FFS between 64 or 128

## RAN1 #106-e

Conclusion:

RAN1 will continue discussions to develop solutions for supporting DBTW

Agreement:

* For 480 and 960kHz PRACH:
  + The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.



Agreement:

* For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, X} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.



* Alt 1: X = 8
* Alt 2: X = 9

Agreement:

For 480kHz and 960kHz sub-carrier spacing, first symbols of the candidate SSB have index {2, 9} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame.

Working assumption:

For 120kHz SSB, the number of candidates SSBs in a half frame is 64.

Agreement:

For DBTW with 120kHz SCS (if supported), support DBTW lengths {0.5, 1, 2, 3, 4, 5} msec

* Note: this should be the same as Rel-16 NR-U DBTW lengths.

Agreement:

For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,

* Support the following set of parameters.

|  |  |  |
| --- | --- | --- |
| SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols |
| 1 | 24 | 2 |
| 1 | 48 | 1 |
| 1 | 48 | 2 |

* + Note: the number of entries corresponding the same {mux pattern, number of RB, number of symbol} tuple (listed above) will depend on required RB offsets that needs to be supported based on channel and sync raster design.
* FFS: addition other set of parameters

Agreement:

Do not support PRACH length L=571, 1151 for 960kHz PRACH and at least L =1151 for 480kHz PRACH.

Agreement:

For 480 and 960kHz PRACH:

* At least the same RO density in time domain (i.e. number of specified RO per reference slot according the PRACH configuration index) as for 120kHz PRACH in FR2 is supported
  + FFS: Support gap between consecutive ROs in time domain and the details to derive the gap

Agreement:

For 480 and 960kHz PRACH,

* When a PRACH slot can contain all time domain PRACH occasions corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching,
  + and when number of PRACH slots in a reference slot is 1,
    - for 480kHz and for 960kHz PRACH
  + and when the number of PRACH slots in a reference slot is 2,
    - for 480kHz and for 960kHz PRACH
* FFS: values, when a PRACH slot cannot contain all time domain PRACH occasions~~,~~ corresponding to a PRACH Config. Index in Table 6.3.3.2-4 of 38.211 including gap(s) between consecutive PRACH occasions (if supported) to account for LBT and/or beam switching.
* FFS: whether to allow for additional values if the maximum that can be configured for the number of FD RO’s is less than 8 (due to BW limitation)

## RAN1 #106-bis-e

Working assumption:

Support DBTW for 120 kHz.

* FFS: Support for 480 kHz and 960 kHz

Conclusion:

Do not support gap between consecutive ROs for 480kHz and 960kHz

Agreement:

Same DCI size for DCI 1\_0 in CSS regardless of channel access mode (i.e., LBT on/off).

* Existing DCI size alignment in TS38.212 applies to DCI 1\_0 and 0\_0 in CSS.

Agreement:

* Indication of licensed and unlicensed operation is not explicitly indicated in MIB or PBCH payload.
  + FFS: Whether or not to indicate licensed regime by different synchronization raster entries.
* Indication of use of LBT or no-LBT is not explicitly indicated in MIB or PBCH payload.

Agreement:

No other values of n other than agreed previously is supported for 120kHz SCS, where parameter ‘n’ is the set of values to determine the first symbols of the candidate SSB blocks for 120kHz SCS in agreement from RAN1 #104-bis-e.

Working assumption:

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz, support multiplexing pattern 1 with 96 PRB CORESET#0, and {1, 2} symbol durations
* Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design

Agreement:

Additionally, support PRACH length L=571 for 480kHz

Agreement:

Support 120 kHz and 480 kHz subcarrier spacing for initial UL BWP for PCell.

Working assumption:

For SCS that DBTW is supported, the following fields are used to indicate parameters related to operation of DBTW

* If only 1 bit is needed: subCarrierSpacingCommon
* If 2 bits is needed: subCarrierSpacingCommon, and 1 bit from pdcch-ConfigSIB1 (pending CORESET0 or search space design would allows for this bit), else, use the spare-bit (not the Msg Extension bit)
  + The design of CORESET0 and search space shall be done without any consideration to this proposal
  + If 2 bits are needed for both 120kHz and 480/960kHz cases, then use the same bit field combination (i.e. use pdcch-ConfigSIB1 bit for 120/480/960 kHz or spare-bit for 120/480.960 kHz)
  + Note: If pdcch-ConfigSIB1 bit is used, the use of controlResourceSetZero (searchSpaceZero) for 120 kHz and   searchSpaceZero (controlResourceSetZero) for 480/960 kHz is not precluded
* FFS: if 3 bits are required
* Note: the working assumption can be confirmed after RAN1 agrees on the number of needed SSB-CORESET0 offsets based on RAN4 channelization design

Agreement:

For 120kHz SCS, for  values:

* If 2 bits are available in MIB for , at least support {16, 32, 64}
* If 1 bit is available in MIB for , support {32, 64}
  + FFS: methods to indicate more  values without increasing used number of bits, e.g., {16, 32, 64}
* Note: value  < 64 indicates DBTW enabled/supported and operation with shared spectrum.
* Note: For operation without shared spectrum channel access, a UE expects to be configured with  = 64. Use of =64 in shared spectrum is not precluded.
* FFS: 1 bit or 2 bits used for 

Agreement:

Supported value of n for 480/960kHz SSB slot pattern:

* ALT A) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
  + same pattern will apply to 480kHz and 960kHz (i.e same N and M for 480 and 960 kHz)
  + N = 2, M = 8
  + FFS: starting position of n
* ALT B) non-contiguous, N slot gap (slots that do not contain SSB) every M slots that contain SSB
  + scaled version pattern will apply between 480 and 960 kHz (i.e. N and M for 480kHz, 2N and 2M for 960 kHz)
  + N = 2, M = 8
  + FFS: starting position of n
* ALT C) slots that do not contain SSB correspond to the slots that do not contain SSB in 120 kHz Case D.
  + Note: ALT 4 means that only slots 32-39 for 480 kHz SSB pattern are reserved for UL and 960 kHz SSB pattern is contiguous.

Agreement:

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, use the following table for multiplexing pattern 1:

* FFS: The value of X (> 0)
* FFS: whether or not to use different X value depending on whether DBTW is ON/OFF
* FFS: whether or not to use same or different X value for 480 and 960 kHz
* FFS: whether Y = , or Y=, or whether to remove entries with Y

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Index** |  | **Number of search space sets per slot** |  | **First symbol index** |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 2 | X | 1 | 1 | 0 |
| 3 | X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 4 | 5 | 1 | 1 | 0 |
| 5 | 5 | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 6 | 0 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 7 | X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 8 | 5 | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 9 | 5 + X | 1 | 1 | 0 |
| 10 | 5 + X | 2 | 1/2 | {0, if  is even}, {7, if  is odd} |
| 11 | 5 + X | 2 | 1/2 | {0, if  is even}, {Y, if  is odd} |
| 12 | 0 | 1 | 2 | 0 |
| 13 | 5 | 1 | 2 | 0 |
| 14 | Reserved | | | |
| 15 | Reserved | | | |

## RAN1 #107-e

**Agreement**

* Support DBTW with 480 and 960 kHz SCS.
* For licensed and unlicensed operation, support 64 candidate SSB positions in a half frame
* Working assumption: Use 2 bits for Q:
  + SubcarrierSpacingCommon
  + spare bit in MIB
* Send LS to RAN2 for confirming the use of the spare bit in MIB
  + The use of 2 bits for Q can be revisited if RAN2 tells RAN1 that the spare bit cannot be used

R1-2112614 [Draft] LS on initial access for 60 GHz Intel Corporation

Final LS endorsed in R1-2112805.

**Agreement**

Confirm the following working assumptions:

* (From #106-bis-e) Support DBTW for 120 kHz.
* (From #106-e) For 120kHz SSB, the number of candidates SSBs in a half frame is 64.

**Agreement**

For SCS that support DBTW, UE derives the QCL relation between candidate SSBs by the value of , where is the candidate SSB index.

**Conclusion**

* The bit-width of ssb-PositionsInBurst in SIB1 and ServingCellConfigCommon is kept the same as in Rel-15 (i.e., 16-bits in SIB1 and 64-bits in ServingCellConfigCommon).

**Agreement**

If multiplexing pattern 3 for 480 and 960 kHz is supported, the TDRA allocation table C is updated as follows:

* Row index 6 (previously reserved) is set to
  + Dmrs-TypeA-Position: 2,3
  + PDSCH mapping type: Type B
  + K0 : 0
  + S = 11
  + L = 2

**Agreement**

Finalizing PRACH slot index for 480 and 960 kHz (removal of bracket of previous agreement)

* when number of PRACH slots in a reference slot is 1,
  + for 480kHz and for 960kHz PRACH
* when the number of PRACH slots in a reference slot is 2,
  + for 480kHz and for 960kHz PRACH

**Agreement**

Update the Table 8.1-2 in TS38.213 to indicate the Ngap (gap between valid RO and SS/PBCH) for 480 kHz and 960 kHz SCS as follows:

* for 480 kHz
* for 960 kHz;

**Agreement**

For single cell operation or for operation with carrier aggregation in a same frequency band, a UE does not transmit PRACH and PUSCH/PUCCH/SRS in a same slot or when a gap between the first or last symbol of a PRACH transmission in a first slot is separated by less than 𝑁 symbols from the last or first symbol, respectively, of a PUSCH/PUCCH/SRS transmission in a second slot where 𝑁=16 for 𝜇=5, 𝑁=32 for 𝜇=6, and 𝜇 is the SCS configuration for the active UL BWP. For a PUSCH transmission with repetition Type B, this applies to each actual repetition for PUSCH transmission [6, TS 38.214].

**Conclusion:**

as part of gap between last symbol of PDCCH order reception and first symbol of the PRACH transmission for FR2-2 uses the same value as FR2-1 (i.e. single value for FR2).

**Agreement**

* For 480 kHz, slot index, n, that contain SSB are:
  + n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, 16,17,18,19,20,21,22,23, 24,25,26,27,28,29,30,31}
* For 960 kHz, slot index, n, that contain SSB are:
  + n = {0,1,2,3,4,5,6,7, 8,9,10,11,12,13,14,15, 16,17,18,19,20,21,22,23, 24,25,26,27,28,29,30,31}

**Agreement**

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz,

* use Table 13-12 in TS38.213 for multiplexing pattern 1,
* use Table 13-15 in TS38.213 for multiplexing pattern 3.

**Agreement**

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, parameter X from previous RAN1 agreement is set to:

* X = 1.25 for 480 kHz
* X = 0.625 for 960 kHz

**Conclusion:**

For FR2-2, support the same mechanism as in Rel-16 for extended RAR window for both 4-step and 2-step RACH.

**Agreement**

For a Type-2 random access procedure, a UE transmits a PUSCH, when applicable, after transmitting a PRACH. The UE encodes a transport block provided for the PUSCH transmission using redundancy version number 0. The PUSCH transmission is after the PRACH transmission by at least symbols where for and for , and is the SCS configuration for the active UL BWP.

**Agreement**

For 480 and 960 kHz, supported DBTW lengths are:

* {1.25, 1, 0.75, 0.5, 0.25, 0.125, X} ms, where X = 0.0625 if Q=8 is supported and X is removed if Q=8 is not supported.

**Agreement**

SSB-PositionQCL-Relation IE to indicate QCL relationship between SSB positions for FR2-2 are same set of values supported for in MIB.

**Agreement**

For operation with shared spectrum access, for SS/PBCH block and CORESET#0 multiplexing pattern 3, a UE monitors PDCCH in the Type0-PDCCH CSS set over slots that include Type0-PDCCH monitoring occasions associated with SS/PBCH blocks that are quasi co-located with the SS/PBCH block that provides a CORESET for Type0-PDCCH CSS set.

**Agreement**

For ‘searchSpaceZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz, parameter Y from previous RAN1 agreement is Y = .

**Agreement**

* For 480kHz and 960kHz PRACH, reuse the RA-RNTI and MSGB-RNTI formula as FR2 and express the slot indexes t\_id based on 120kHz SCS:
  + RA-RNTI =1+s\_id+14×t\_id+14×80×f\_id +14×80×8×ul\_carrier\_id
  + MSGB-RNTI = 1 + s\_id + 14 × t\_id + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id + 14 × 80 × 8 × 2
    - where the subcarrier spacing to determine t\_id is based on the value of µ specified in clause 5.3.2 in TS 38.211 [8] for µ = {0, 1, 2, 3}
    - for µ = {5, 6}, t\_id is the index of the 120 kHz slot in a system frame that contains the PRACH occasion (0 ≤ t\_id < 80).
  + Note: As per previous RAN1 agreement, there is only one 480 or 960 kHz PRACH slot in a 120kHz slot, such that RA-RNTI and MSGB-RNTI does not result in ID collision.
* Send LS to RAN2 on the updates on RA-RNTI and MSGB-RNTI.

R1-2112734 [Draft] LS on RA-RNTI and MSGB-RNTI for 480 and 960 kHz Intel Corporation

Final LS endorsed in R1-2112832 (with removal of “first” in text referring to the captured agreement)

**Agreement**

* Same values using the same set of signaling bits are supported for 120, 480, and 960 kHz.
* Supported values of : {16, 32, 64}
  + Note:
    - For operation with shared spectrum channel access, any supported value of can be indicated and value < 64 indicates DBTW enabled
    - UE is expected to be configured with =64 in licensed operations
    - For operation with and without shared spectrum channel access, =64 indicates that the SS/PBCH block index and the candidate SS/PBCH block index have a one-to-one mapping relationship.

**Working assumption**

For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,

* After supporting entries for multiplexing pattern 1 for the agreed pairs of (, ) ={(24, 2), (48, 1), (48,2)} (with required RB offsets), if additional entries are left, support multiplex pattern 3 with 24 PRB and 2 symbol duration, and multiplexing pattern 3 with 48 PRB and 2 symbol duration.

**Working assumption**

For ‘controlResourceSetZero’ configuration for {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz and {960, 960} kHz,

* After supporting entries for multiplexing pattern 1 for the agreed pairs of (, ) ={(24, 2), (48, 1), (48,2)} (with required RB offsets) and multiplex pattern 3 with 24 and 48 PRB and 2 symbol duration (with required RB offsets), if additional entries are left, support multiplexing pattern 1 with 96 PRB and 2 symbol duration
  + Note: the working assumption can be confirmed once RAN1 agrees on the number of needed SSB-CORESET0 offsets for 24 and 48 RB CORESET0 based on RAN4 channelization design.

**Agreement**

* If is indicated, the same interpretation of ssb-PositionsInBurst in SIB1 or ServingCellConfigCommon as in Rel-16 is supported, i.e.:
  + A bit set to 1 at position indicates SS/PBCH block index k-1
  + The UE assumes that a bit at position k > is set to 0
    - For ssb-PositionsInBurst in SIB1, the UE assumes that a bit at *groupPresence* corresponding to a SS/PBCH block index ≥ is set to 0
  + Note: for ssb-PositionsInBurst in SIB1, position k corresponds to the SS/PBCH block index indicated by a bit in inOneGroup and a bit in groupPresence
* In operation with shared spectrum in 60 GHz, for ssb-PositionsInBurst in ServingCellConfigCommonSIB,
  + for MSB k, k≥1, of inOneGroup and MSB m, m≥1, of groupPresense of ssb-PositionsInBurst:
    - if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to ‘SSB index’ equal to k-1+(m-1)×8 may be transmitted;
    - if MSB k of inOneGroup or MSB m of groupPresense is set to 0, the UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to ‘SSB index’ equal to k-1+(m-1)×8 is not transmitted;
* In operation with shared spectrum in 60 GHz, for ssb-PositionsInBurst in ServingCellConfigCommon,
  + ssb-PositionsInBurst bits correspond to supported ‘SSB indices’,
    - and UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to indicated bit(s) may be transmitted;
    - and UE assumes that SSB(s) within DBTW with ‘candidate SSB index(es)’ corresponding to not indicated bit(s) are not transmitted
* Note to spec editor: The above three bullets maintain the same behavior as Rel-16 NR-U

**Agreement**

Update the Table 6.3.3.2-1 in TS 38.211 as follows:

* Table 6.3.3.2-1: Supported combinations of and , and the corresponding value of .

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | for PRACH | for PUSCH | , allocation expressed in number of RBs for PUSCH |  |
| ... | ... | ... | ... | ... |
| 139 | 120 | 120 | 12 | 2 |
| 139 | 120 | 480 | 3 | 1 |
| 139 | 120 | 960 | 2 | 23 |
| 139 | 480 | 120 | 48 | 2 |
| 139 | 480 | 480 | 12 | 2 |
| 139 | 480 | 960 | 6 | 2 |
| 139 | 960 | 120 | 96 | 2 |
| 139 | 960 | 480 | 24 | 2 |
| 139 | 960 | 960 | 12 | 2 |
| 571 | 120 | 120 | 48 | 2 |
| 571 | 120 | 480 | 12 | 1 |
| 571 | 120 | 960 | 7 | 47 |
| 571 | 480 | 120 | 192 | 2 |
| 571 | 480 | 480 | 48 | 2 |
| 571 | 480 | 960 | 24 | 2 |
| 1151 | 120 | 120 | 97 | 6 |
| 1151 | 120 | 480 | 25 | 23 |
| 1151 | 120 | 960 | 13 | 45 |

## RAN1 #107-bis-e

**Conclusion:**

RRC parameters list to capture changes identified below:

* Add the following note to the comment section of discoveryBurstWindowLength-r17 row in RRC parameter list
  + “Note: This parameter is to be included in both SIB1 and the common serving cell configuration parameters”.
* Support adding “SSB-PositionQCL-Relation-r17” to RRC parameter list as both UE-specific and cell-specific parameter.
* Inform RAN2 (by adding notes to RRC parameter list) that the either the value range of the information element SSB-PositionQCL-Relation-r16 needs to be extended, or a new Rel-17 IE need to be defined to allow configuration of Q = 16, 32, or 64 in SIB2, SIB3, SIB4, MeasObjectNR, and ServingCellConfigCommon for RRM measurements when operating with shared spectrum channel access in FR2-2.

The TP below for TS38.213v17.0.0 is endorsed as a working assumption

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| =========== Unchanged Text Omitted ===========  Table 13-15A: PDCCH monitoring occasions for Type0-PDCCH CSS set - SS/PBCH block and CORESET multiplexing pattern 3 and {SS/PBCH block, PDCCH} SCS {480, 480} kHz or {960, 960} kHz   |  |  |  | | --- | --- | --- | | Index | PDCCH monitoring occasions (SFN and slot number) | First symbol index  ( = 0, 1, …, 31) | | 0 |  | 2, 9 in  , |   ============ Unchanged Text Omitted ============ |

The TP below for TS38.211v17.0.0 is endorsed

|  |
| --- |
| \*\*\* Unchanged text omitted \*\*\*  5.3.2 OFDM baseband signal generation for PRACH  The time-continuous signal  on antenna port for PRACH is defined by  \*\*\* Unchanged text omitted \*\*\* |

The TP below for TS38.214v17.0.0 is endorsed

|  |
| --- |
| \*\*\* Unchanged text omitted \*\*\*  7       UE procedures for transmitting and receiving on a carrier with intra-cell guard bands  For operation with shared spectrum channel access in FR1, when the UE is configured with any of *IntraCellGuardBandsPerSCS* for UL carrier and for DL carrier with SCS configuration , the UE is provided with intra-cell guard bands on a carrier with , each defined by start CRB and size in number of CRBs, and, provided by higher layer parameters *startCRB* and *nrofCRBs*, respectively, where. The subscript *x* is set to DL and UL for the downlink and uplink, respectively. Where there is no risk of confusion, the subscript *x* can be dropped. The intra-cell guard bands separateRB sets, each defined by start and end CRB,and, respectively. The UE does not expect that *nrofCRBs* is configured with non-zero value smaller than the applicable intra-cell guard bands as specified in [8, TS 38.101-1] corresponding to and carrier size. The UE determines the start and end CRB indices for as  \*\*\* Unchanged text omitted \*\*\* |

**R1-2200689** Summary #1 of email discussion on initial access aspect of NR extension up to 71 GHz Moderator (Intel Corporation)

TP# 8-1a for TS38.213 in section 3 of R1-2200689 is endorsed.

**Conclusion**

RRC parameters list to capture changes identified below

* New parameter, ra-ResponseWindow-r17, under sub-feature group SSB and RACH
  + Value range {sl240, sl320, sl640, sl960, sl1280, sl1920, sl2560}
  + Based on previous conclusion:
    - For FR2-2, support the same mechanism as in Rel-16 for extended RAR window for both 4-step and 2-step RACH.
* New parameter, msgB-ResponseWindow-r17, under sub-feature group SSB and RACH
  + Value range { sl240, sl640, sl960, sl1280, sl1920, sl2560}
  + Based on previous conclusion:
    - For FR2-2, support the same mechanism as in Rel-16 for extended RAR window for both 4-step and 2-step RACH.
* Existing parameter, msgA-PRACH-RootSequenceIndex-r16, under sub-feature group SSB and RACH
  + Description:
    - May not need to change the IE, but need to add in the note on the limitation to be used with SCS. Field description requires updating to capture that L = 1151 is not supported for SCS 480 and 960 kHz and L = 571 is not supported for 960 kHz.
  + Value range:
    - CHOICE { l571 INTEGER {0..569}, l1151 INTEGER {0..1149}}
  + Cell-specific

## RAN1 #108-e

Working assumption

* Use 1 bit for Q in MIB
  + SubcarrierSpacingCommon field will be used to convey value of {32, 64} for operation with shared spectrum channel access



* + Note that this is revising the working assumption made in RAN1#107-e on “use 2 bits for Q, {SubcarrierSpacingCommon, spare bit in MIB}”

**Conclusion**

Update the ssb-PositionQCL in RRC to {32, 64} values.

* For reference, the following are list of RRC IEs that references ssb-PositionQCL in release 16.
  + SIB2:: ssb-PositionQCL-Common-r16
  + SIB3:: ssb-PositionQCL-r16
  + SIB4:: ssb-PositionQCL-Common-r16
  + SIB4:: ssb-PositionQCL-r16
  + MeasObjectNR:: ssb-PositionQCL-Common-r16
  + MeasObjectNR:: ssb-PositionQCL-r16
  + ServingCellConfigCommon:: ssb-PositionQCL-r16

Text Proposal #1-3 (for 38.213, Section 4.1) in section 3 of R1-2202503 is endorsed.

TP# 1-3 for TS38.213

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4 Synchronization procedures  4.1 Cell search  < Unchanged parts are omitted >  For operation without shared spectrum channel access, an SS/PBCH block index is same as a candidate SS/PBCH block index.  < Unchanged parts are omitted >  For operation with shared spectrum channel access in FR2-2, a UE assumes that SS/PBCH blocks in a serving cell that are within a same discovery burst transmission window or across discovery burst transmission windows are quasi co-located with respect to average gain, quasi co-location 'typeA' and 'typeD' properties, when applicable, if a value of is same among the SS/PBCH blocks, where is the candidate SS/PBCH block index. is either provided by *ssb-PositionQCL* or, if *ssb-PositionQCL* is not provided,obtained from a *MIB* provided by a SS/PBCH block according to Table 4.1-2. The UE can determine an SS/PBCH block index according to . The UE assumes that within a discovery burst transmission window, a number of transmitted SS/PBCH blocks on a serving cell is not larger than and a number of transmitted SS/PBCH blocks with a same SS/PBCH block index is not larger than one.  For operation without shared spectrum channel access in FR2-2, a UE expects *subCarrierSpacingCommon* = ‘*scs30or120’* from a MIB provided by a SS/PBCH block.  Table 4.1-2: Mapping between ~~the combination of~~ *subCarrierSpacingCommon* ~~and~~ *~~spare~~* to for operation with shared spectrum channel access in FR2-2   |  |  |  | | --- | --- | --- | | *subCarrierSpacingCommon* | *~~spare~~* |  | | ~~scs15or60~~ | ~~0~~ | ~~16~~ | | scs15or60 | ~~1~~ | 32 | | scs30or120 | ~~0~~ | 64 | | ~~scs30or120~~ | ~~1~~ | ~~reserved~~ |   < Unchanged parts are omitted > |

**Conclusion**

* For operation with shared spectrum channel access, support default DBTW length of 5ms if discoveryBurstWindowLength is not provided in FR2-2.
* No change to specification is needed

**Working Assumption**

* The following table is used for set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120}, {480, 480}, and {960, 960} kHz for FR2-2.
  + FFS: whether/how to define X, if defined, candidate values {56, 76}
* Text Proposal #4-2D (for 38.213, Section 13) in section 3 of R1-2202503 is endorsed
* Note: this working assumption can be revisited once RAN4 finalizes the further details of the channelization.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Index** | **SS/PBCH block and CORESET multiplexing pattern** | **Number of RBs** | **Number of Symbols** | **Offset (RBs)** |
| 0 | 1 | 24 | 2 | 0 |
| 1 | 1 | 24 | 2 | 4 |
| 2 | 1 | 48 | 1 | 0 |
| 3 | 1 | 48 | 1 | 14 |
| 4 | 1 | 48 | 1 | 28 |
| 5 | 1 | 48 | 2 | 0 |
| 6 | 1 | 48 | 2 | 14 |
| 7 | 1 | 48 | 2 | 28 |
| 8 | 1 | 96 | 1 | 0 |
| 9 | 1 | 96 | 1 | X |
| 10 | 1 | 96 | 2 | 0 |
| 11 | 1 | 96 | 2 | X |
| 12 | 3 | 24 | 2 | -20 if  -21 if > 0 |
| 13 | 3 | 24 | 2 | 24 |
| 14 | 3 | 48 | 2 | -20 if  -21 if > 0 |
| 15 | 3 | 48 | 2 | 48 |

Text Proposal #5-1A (for 38.215, Section 5.1.3) in section 3 of R1-2202503 is endorsed.

TP# 5-1A for TS38.215

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 5.1.3 SS reference signal received quality (SS-RSRQ)  ======================== Unchanged Text Omitted ===========================  Table 5.1.3-1: NR Carrier RSSI measurement symbols   |  |  | | --- | --- | | **OFDM signal indication *endSymbol*** | **Symbol indexes** | | | 0 | {0,1} | | 1 | For 480 kHz and 960 kHz {0,1,2,..,10,12}; otherwise {0,1,2,..,10,11} | | 2 | {0,1,2,…, 5} | | 3 | {0,1,2,…, 7} |   ========================= Unchanged Text Omitted ============================== |

Text Proposal #7-2B (for 38.211, Section 5.3.2) in section 3 of R1-2202503 is endorsed.

TP# 7-2B for TS38.211

|  |
| --- |
| **5.3.2 OFDM baseband signal generation for PRACH**  < Unchanged parts are omitted >  where  -  is given by the parameter "starting symbol" in Tables 6.3.3.2-2 to 6.3.3.2-4;  -  is the PRACH transmission occasion within the PRACH slot, numbered in increasing order from 0 to  within a RACH slot where  is given Tables 6.3.3.2-2 to 6.3.3.2-4 for and fixed to 1 for ;  -  is given by Tables 6.3.3.2-2 to 6.3.3.2-4;  -  is given by  - if kHz, then  - if kHz and either of "Number of PRACH slots within a subframe" in Tables 6.3.3.2-2 to 6.3.3.2-3 or "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then , otherwise  *{indent backwards here}*- if kHz and ~~- the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then for kHz and for kHz~~  - the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 1, then for kHz and for kHz, or  - the "Number of PRACH slots within a 60 kHz slot" in Table 6.3.3.2-4 is equal to 2, then for kHz and for kHz.  < Unchanged parts are omitted > |

Text Proposal #7-3B (for 38.211, Section 7.4.3.1) in section 3 of R1-2202503 is endorsed.

TP# 7-3B for TS38.211

|  |
| --- |
| 7.4.3.1 Time-frequency structure of an SS/PBCH block ============= Unchanged Text Omitted =============  - For operation with shared spectrum channel access in FR2-2 and f~~F~~or operation without shared spectrum channel access ~~and for operation with shared spectrum channel access in FR2-2~~, the 4 least significant bits of  are given by the higher-layer parameter *ssb-SubcarrierOffset* and for FR1 the most significant bit of  is given by in the PBCH payload as defined in clause 7.1.1 of [4, TS 38.212].  - For operation with shared spectrum channel access in FR1, the 4 least significant bits of are given by the higher-layer parameter *ssb-SubcarrierOffset* and the most significant bit of is given by in the PBCH payload as defined in clause 7.1.1 of [4, TS 38.212]. If , ; otherwise, , and if *ssb-SubcarrierOffset* is not provided, is derived from the frequency difference between the SS/PBCH block and Point A.  ============= Unchanged Text Omitted ===================== |

Text Proposal #7-4B (for 38.213, Section 13) in section 3 of R1-2202503 is endorsed.

TP# 7-4B for TS38.213

|  |
| --- |
| 13 UE procedure for monitoring Type0-PDCCH CSS sets  ============= Unchanged Text Omitted =============  For operation with shared spectrum channel access in FR2-2 and f~~F~~or operation without shared spectrum channel access ~~and for operation with shared spectrum channel access in FR2-2~~, a UE assumes that the offset in Tables 13-1 through 13-10C is defined with respect to the SCS of the CORESET for Type0-PDCCH CSS set from the smallest RB index of the CORESET for Type0-PDCCH CSS set to the smallest RB index of the common RB overlapping with the first RB of the corresponding SS/PBCH block. The SCS of the CORESET for Type0-PDCCH CSS set is provided by *subCarrierSpacingCommon* for FR1 and FR2-1 and same as the SCS of the corresponding SS/PBCH block for FR2-2. In Tables 13-7, 13-8, and 13-10 is defined in [4, TS 38.211].  ============= Unchanged Text Omitted ===================== |

## RAN1 #109-e

R1-2205380 LS to RAN2 on RRC parameter update for NR up to 71GHz RAN1, Qualcomm

Final LS is endorsed in R1-2205380.

**Agreement:**

* Text Proposal #1-1 (for TS38.213 v17.1.0, clause 13) in section 3 of R1-2205138 is endorsed, without the empty row.

**TP #1-1 (TS38.213)**

|  |
| --- |
| **Reasons for change:**  The specification is missing additional SSB and CORESET RB offset for FR2-2 when using 96 RB CORESET. |
| **Summary of change:**  Add 76 RB offset for 96 RB CORESET with SSB/CORESET multiplexing pattern 1. |
| **Consequence if not approved:**  Unable to support 96 RB CORESET for some channel location deployments in FR2-2 |
| 13 UE procedure for monitoring Type0-PDCCH CSS sets  ============== Unchanged Text Omitted ==============  Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz, {480, 480} kHz, or {960, 960} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 1 | 14 | | 4 | 1 | 48 | 1 | 28 | | 5 | 1 | 48 | 2 | 0 | | 6 | 1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 | 1 | 96 | 1 | 76 | | 10 | 1 | 96 | 2 | 0 | | 11 | 1 | 96 | 2 | 76 | | 12 | 3 | 24 | 2 | -20 if  -21 if | | 13 | 3 | 24 | 2 | -24 | | 14 | 3 | 48 | 2 | -20 if  -21 if | | 15 | 3 | 48 | 2 | -48 |   ============== Unchanged Text Omitted ============== |

**Agreement:**

* Text Proposal #3-1 (for TS38.213 v17.1.0, clause 13) in section 3 of R1-2205138 is endorsed.

**TP#3-1 (TS38.213)**

|  |
| --- |
| **Reasons for change:**  The sign offset RB value of index 13 and 15 of Table 13-10A is incorrect. |
| **Summary of change:**  Remove the ‘-‘ negative sign for offset RB value of index 13 and 15 of Table 13-10A. |
| **Consequence if not approved:**  Incorrect RB offset configuration for multiplexing pattern 3 and both network and UE are not able to utilize the configuration. |
| 13 UE procedure for monitoring Type0-PDCCH CSS sets \*\*\* Unchanged text is omitted \*\*\*  Table 13-10A: Set of resource blocks and slot symbols of CORESET for Type0-PDCCH search space set when {SS/PBCH block, PDCCH} SCS is {120, 120} kHz, {480, 480} kHz, or {960, 960} kHz for FR2-2   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Index | SS/PBCH block and CORESET multiplexing pattern | Number of RBs | Number of Symbols | Offset (RBs) | | 0 | 1 | 24 | 2 | 0 | | 1 | 1 | 24 | 2 | 4 | | 2 | 1 | 48 | 1 | 0 | | 3 | 1 | 48 | 1 | 14 | | 4 | 1 | 48 | 1 | 28 | | 5 | 1 | 48 | 2 | 0 | | 6 | 1 | 48 | 2 | 14 | | 7 | 1 | 48 | 2 | 28 | | 8 | 1 | 96 | 1 | 0 | | 9 |  |  |  |  | | 10 | 1 | 96 | 2 | 0 | | 11 |  |  |  |  | | 12 | 3 | 24 | 2 | -20 if  -21 if | | 13 | 3 | 24 | 2 | 24 | | 14 | 3 | 48 | 2 | -20 if  -21 if | | 15 | 3 | 48 | 2 | 48 |   \*\*\* Unchanged text is omitted \*\*\* |

**Agreement:**

* Text Proposal #3-2A for TS38.331 in section 3 of R1-2205138 is endorsed and recommended to RAN2.
* Send LS to RAN2 asking to update the description.

**TP#3-2A (TS38.331)**

|  |
| --- |
| *SSB-ToMeasure* field descriptions |
| ***longBitmap***  Bitmap when maximum number of SS/PBCH blocks per half frame equals to 64 as defined in TS 38.213 [13], clause 4.1. For operation with shared spectrum channel access, if the k-th bit is set to 1, the UE assumes that one or more SS/PBCH blocks within the SMTC measurement duration with candidate SS/PBCH block indexes corresponding to SS/PBCH block index equal to k – 1 may be transmitted; if the k-th bit is set to 0, the UE assumes that the corresponding SS/PBCH block(s) are not transmitted. |

## RAN1 #110

**Agreement**

Endorse the TP below for TS38.213

13 UE procedure for monitoring Type0-PDCCH CSS sets

**<Unchanged parts are omitted>**

If a UE detects a first SS/PBCH block and determines that a CORESET for Type0-PDCCH CSS set is not present, and for for FR1 or for for FR2, the UE may determine the nearest (in the corresponding frequency direction) global synchronization channel number (GSCN) of a second SS/PBCH block having a CORESET for an associated Type0-PDCCH CSS set as . is the GSCN of the first SS/PBCH block, in FR1 and FR2-1, 3 in FR2-2, and is a GSCN offset provided by Table 13-16 for FR1 and Table 13-17 for FR2. If the UE detects the second SS/PBCH block and the second SS/PBCH block does not provide a CORESET for Type0-PDCCH CSS set, as described in clause 4.1, the UE may ignore the information related to GSCN of SS/PBCH block locations for performing cell search.



**<Unchanged parts are omitted>**

Final CR is agreed in [R1-2208241](file:///C:\Users\daewonle\OneDrive%20-%20Intel%20Corporation\Documents\ngs\Docs\R1-2208241.zip)

**Agreement**

TP for TS38.211 in [R1-2206083](file:///C:\Users\daewonle\OneDrive%20-%20Intel%20Corporation\Documents\ngs\Docs\R1-2206083.zip) and TP for TS38.213 in [R1-2206084](file:///C:\Users\daewonle\OneDrive%20-%20Intel%20Corporation\Documents\ngs\Docs\R1-2206084.zip) are endorsed.

**Agreement**

Final CRs are agreed in [R1-2208033](file:///C:\Users\daewonle\OneDrive%20-%20Intel%20Corporation\Documents\ngs\Docs\R1-2208033.zip) TS38.213 CR0337 and [R1-2208034](file:///C:\Users\daewonle\OneDrive%20-%20Intel%20Corporation\Documents\ngs\Docs\R1-2208034.zip) TS38.211 CR0100.