Table for set 1 FR1 TDD

|  |  |  |
| --- | --- | --- |
| **Power state** | Relative Power | **Total transition time5** |
| Deep sleep1 | P1=1 | Cat 1:  20ms [CATT],  50ms [Intel, E//],  80ms[Fujitsu]  Cat 2:  5s [ZTE],  10s [Huawei],  few seconds [Nokia?],  1s[vivo]  1s[CMCC] |
| Light sleep2 | Cat 1:  3 [CATT]  5 [ZTE]  1.5[Huawei]  1.5[vivo]  1.875[CMCC]  2.04[Samsung]  Cat 2:  25 [E//],  25[QC]  20[Intel]  25[fujitsu] | Cat 1:  2ms [CATT]  5ms[Intel, E//]  6ms[QC]  4ms[Fujitsu]  1ms[vivo]  100ms[CMCC]  Cat 2:  400ms[ZTE]  Few seconds [Huawei], |
| Micro | Cat1:  5[CATT]  10[ZTE]  3 [Huawei]  5.5[vivo]  7.65[Samsung]  2.54[CMCC]  Cat 2:  60[E//, QC]  40[Intel] | 0 |
| DL | Cat 1:  10[CATT]  100[ZTE]  8.79[CMCC]  19.05[Samsung]  Cat 2:  260[E//]  300[QC]  320[Intel]  172[vivo] |  |
| UL | Cat 1:  100[E//, QC]  120[Intel]  Cat 2:  1 [CATT]  10[ZTE]  11.5[vivo]  4.17[CMCC] |  |

Table for set 2 FR1 FDD

|  |  |  |
| --- | --- | --- |
| **Power state** | Relative Power | **Total transition time5** |
| Deep sleep1 | P1=1 | T1  20ms [QC],  50ms [Intel, E//],  Cat 2:  5s [ZTE],  10s [Huawei],  few seconds [Nokia?], |
| Light sleep2 | P2  Cat 1:  5 [ZTE]  1.5[Huawei]  Cat 2:  20 [QC]  20[Intel] | T2  Cat 1:  5ms[Intel, E//]  6ms[QC]  Cat 2:  400ms[ZTE]  Few seconds [Huawei], |
| Micro | Cat 1:  10[ZTE]  3 [Huawei]  Cat 2:  50[QC]  40[Intel]  42[E//] |  |
| DL | Cat 1:  270[QC]  320[Intel]  Cat 2:  100[ZTE] |  |
| UL | Cat 1:  1 [CATT]  10[ZTE]  Cat 2:  80[QC]  84[E//]  120[Intel] |  |

Table for set 3

|  |  |  |
| --- | --- | --- |
| **Power state** | Relative Power | **Total transition time5** |
| Deep sleep1 | P1=1 | T1  Cat 1:  20ms [QC],  50ms [Intel, E//],  Cat 2:  5s [ZTE],  10s [Huawei],  few seconds [Nokia?], |
| Light sleep2 | P2  Cat 1:  5 [ZTE]  1.5[Huawei]  Cat 2:  20[Intel] | T2  Cat1:  5ms[Intel, E//]  6ms[QC]  Cat 2:  400ms[ZTE]  Few seconds [Huawei], |
| Micro | Cat 1:  10[ZTE]  3 [Huawei]  Cat 2::  40[Intel] |  |
| DL | 70[E// for FR2] |  |
| UL |  |  |