Agenda Item:

Source : SK Telecom

Title : CRs to 25.211, 25.213, and 25.214 for clean up of USTS related specifications

Document for : Approval

In the last TSG RAN #6 meeting, USTS is decided to be postponed to the next version of specifications, Release-00, due to the missing support in other working groups. Therefore the USTS related contents in the current specifications, Release-99, shall be removed.

CHANGE REQUEST

Please see embedded help file at the bottom of this page for instructions on how to fill in this form correctly.

25.211	CR	**046**	Current Version:	**3.1.1**

GSM (AA.BB) or 3G (AA.BBB) specification number ↑   *↑ CR number as allocated by MCC support team*

For submission to: **TSG-RAN #7**
list expected approval meeting # here
↑

for approval	**X**
for information	

strategic	
non-strategic	

(for SMG use only)

Form: CR cover sheet, version 2 for 3GPP and SMG   *The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects: (U)SIM ☐   ME **X**   UTRAN / Radio **X**   Core Network ☐
(at least one should be marked with an X)

Source: SK Telecom   **Date:**   2000-03-03

Subject: Clean up of USTS related specifications

Work item:

Category:
F Correction   **X**
A Corresponds to a correction in an earlier release
B Addition of feature
C Functional modification of feature
D Editorial modification

(only one category shall be marked with an X)

Release:
Phase 2	
Release 96	
Release 97	
Release 98	
Release 99	**X**
Release 00	

Reason for change: USTS is Release-00 item. Therefore USTS related specifications shall be removed in Release-99.

Clauses affected: 5.3.2
7.6.3

Other specs affected:
Other 3G core specifications		→ List of CRs:	
Other GSM core specifications		→ List of CRs:	
MS test specifications		→ List of CRs:	
BSS test specifications		→ List of CRs:	
O&M specifications		→ List of CRs:	

**Other comments:**

help.doc

<--------- double-click here for help and instructions on how to create a CR.

5.3.2 Dedicated downlink physical channels

There is only one type of downlink dedicated physical channel, the Downlink Dedicated Physical Channel (downlink DPCH).

Within one downlink DPCH, dedicated data generated at Layer 2 and above, i.e. the dedicated transport channel (DCH), is transmitted in time-multiplex with control information generated at Layer 1 (known pilot bits, TPC commands, and an optional TFCI). The downlink DPCH can thus be seen as a time multiplex of a downlink DPDCH and a downlink DPCCH, compare section 5.2.1. It is the UTRAN that determines if a TFCI should be transmitted, hence making it is mandatory for all UEs to support the use of TFCI in the downlink. ~~In case of USTS, the TPC bits in slot #14 in frames with CFN mod 2 = 0 are replaced by Time Alignment Bits (TABs) as described in section 9.3 of [5]~~

Figure 8 shows the frame structure of the downlink DPCH. Each frame of length 10 ms is split into 15 slots, each of length $T_{slot} = 2560$ chips, corresponding to one power-control period.

DPDCH	DPCCH		DPDCH	DPCCH
Data1 N_{data1} bits	TPC N_{TPC} bits	TFCI N_{TFCI} bits	Data2 N_{data2} bits	Pilot N_{pilot} bits

$$T_{slot} = 2560 \text{ chips}, 10*2^k \text{ bits (k=0..7)}$$

Slot #0	Slot #1		Slot #i		Slot #14

One radio frame, $T_f = 10$ ms
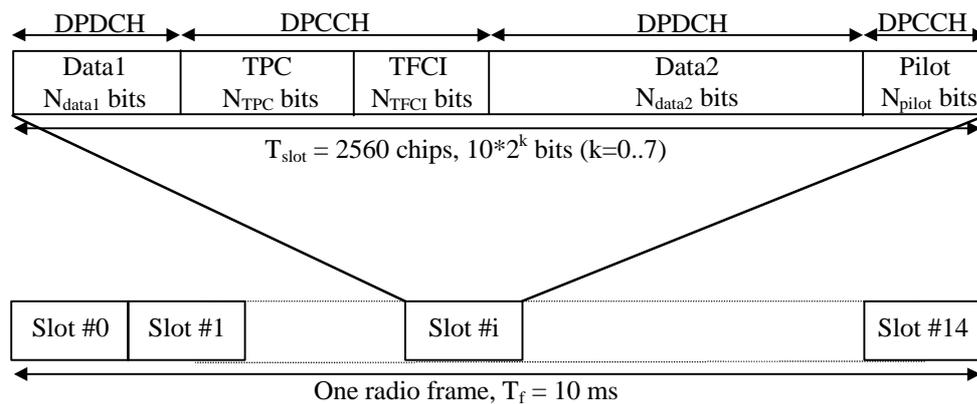
Figure 8: Frame structure for downlink DPCH

The parameter k in figure 8 determines the total number of bits per downlink DPCH slot. It is related to the spreading factor SF of the physical channel as $SF = 512/2^k$. The spreading factor may thus range from 512 down to 4.

The exact number of bits of the different downlink DPCH fields (N_{pilot}, N_{TPC}, N_{TFCI}, N_{data1} and N_{data2}) is determined in table 11.The overhead due to the DPCCH transmission has to be negotiated at the connection set-up and can be re-negotiated during the communication, in order to match particular propagation conditions.

There are basically two types of downlink Dedicated Physical Channels; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI(e.g. for fixed-rate services). These types are reflected by the duplicated rows of table 11. In compressed mode, a different slot format is used compared to normal mode. There are two possible compressed slot formats that are labelled A and B. Format B is used for compressed mode by spreading factor reduction and format A is used for all other transmission time reduction methods. The channel bit and symbol rates given in table 11 are the rates immediately before spreading.

Table 11: DPDCH and DPCCH fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot			Transmitted slots per radio frame N_{Tr}
					N_{Data1}	N_{Data2}	N_{TPC}	N_{TFCI}	N_{Pilot}	
0	15	7.5	512	10	0	4	2	0	4	15
0A	15	7.5	512	10	0	4	2	0	4	8-14
0B	30	15	256	20	0	8	4	0	8	8-14
1	15	7.5	512	10	0	2	2	2	4	15
1B	30	15	256	20	0	4	4	4	8	8-14
2	30	15	256	20	2	14	2	0	2	15
2A	30	15	256	20	2	14	2	0	2	8-14
2B	60	30	128	40	4	28	4	0	4	8-14
3	30	15	256	20	2	12	2	2	2	15
3A	30	15	256	20	2	10	2	4	2	8-14
3B	60	30	128	40	4	24	4	4	4	8-14
4	30	15	256	20	2	12	2	0	4	15
4A	30	15	256	20	2	12	2	0	4	8-14
4B	60	30	128	40	4	24	4	0	8	8-14
5	30	15	256	20	2	10	2	2	4	15
5A	30	15	256	20	2	8	2	4	4	8-14
5B	60	30	128	40	4	20	4	4	8	8-14
6	30	15	256	20	2	8	2	0	8	15
6A	30	15	256	20	2	8	2	0	8	8-14
6B	60	30	128	40	4	16	4	0	16	8-14
7	30	15	256	20	2	6	2	2	8	15
7A	30	15	256	20	2	4	2	4	8	8-14
7B	60	30	128	40	4	12	4	4	16	8-14
8	60	30	128	40	6	28	2	0	4	15
8A	60	30	128	40	6	28	2	0	4	8-14
8B	120	60	64	80	12	56	4	0	8	8-14
9	60	30	128	40	6	26	2	2	4	15
9A	60	30	128	40	6	24	2	4	4	8-14
9B	120	60	64	40	12	52	4	4	8	8-14
10	60	30	128	40	6	24	2	0	8	15
10A	60	30	128	40	6	24	2	0	8	8-14
10B	120	60	64	80	12	48	4	0	16	8-14
11	60	30	128	40	6	22	2	2	8	15
11A	60	30	128	40	6	20	2	4	8	8-14
11B	120	60	64	80	12	44	4	4	16	8-14
12	120	60	64	80	12	48	4	8*	8	15
12A	120	60	64	80	12	40	4	16*	8	8-14
12B	240	120	32	160	24	96	8	16*	16	8-14
13	240	120	32	160	28	112	4	8*	8	15
13A	240	120	32	160	28	104	4	16*	8	8-14
13B	480	240	16	320	56	224	8	16*	16	8-14
14	480	240	16	320	56	232	8	8*	16	15
14A	480	240	16	320	56	224	8	16*	16	8-14
14B	960	480	8	640	112	464	16	16*	32	8-14
15	960	480	8	640	120	488	8	8*	16	15
15A	960	480	8	640	120	480	8	16*	16	8-14
15B	1920	960	4	1280	240	976	16	16*	32	8-14
16	1920	960	4	1280	248	1000	8	8*	16	15
16A	1920	960	4	1280	248	992	8	16*	16	8-14

* If TFCI bits are not used, then DTX shall be used in TFCI field.

NOTE1: Compressed mode is only supported through spreading factor reduction for SF=512 with TFCI.

NOTE2: Compressed mode by spreading factor reduction is not supported for SF=4.

The pilot symbol pattern is described in table 12. The shadowed part can be used as frame synchronization words. (The symbol pattern of the pilot symbols other than the frame synchronization word shall be "11".) In table 12, the transmission order is from left to right. (Each two-bit pair represents an I/Q pair of QPSK modulation.)

In downlink compressed mode through spreading factor reduction, the number of bits in the TPC and Pilot fields are doubled. Symbol repetition is used to fill up the fields. Denote the bits in one of these fields in normal mode by $x_1, x_2, x_3, \ldots, x_X$. In compressed mode the following bit sequence is sent in corresponding field: $x_1, x_2, x_1, x_2, x_3, x_4, x_3, x_4, \ldots, x_{X.}$.

Table 12: Pilot Symbol Pattern

	$N_{pilot} = 2$	$N_{pilot} = 4$		$N_{pilot} = 8$				$N_{pilot} = 16$							
Symbol #	0	0	1	0	1	2	3	0	1	2	3	4	5	6	7
Slot #0	11	11	11	11	11	11	10	11	11	11	10	11	11	11	10
1	00	11	00	11	00	11	10	11	00	11	10	11	11	11	00
2	01	11	01	11	01	11	01	11	01	11	01	11	10	11	00
3	00	11	00	11	00	11	00	11	00	11	00	11	01	11	10
4	10	11	10	11	10	11	01	11	10	11	01	11	11	11	11
5	11	11	11	11	11	11	10	11	11	11	10	11	01	11	01
6	11	11	11	11	11	11	00	11	11	11	00	11	10	11	11
7	10	11	10	11	10	11	00	11	10	11	00	11	10	11	00
8	01	11	01	11	01	11	10	11	01	11	10	11	00	11	11
9	11	11	11	11	11	11	11	11	11	11	11	11	00	11	11
10	01	11	01	11	01	11	01	11	01	11	01	11	11	11	10
11	10	11	10	11	10	11	11	11	10	11	11	11	00	11	10
12	10	11	10	11	10	11	00	11	10	11	00	11	01	11	01
13	00	11	00	11	00	11	11	11	00	11	11	11	00	11	00
14	00	11	00	11	00	11	11	11	00	11	11	11	10	11	01

The relationship between the TPC symbol and the transmitter power control command is presented in table 13.

Table 13: TPC Bit Pattern

TPC Bit Pattern			Transmitter power control command
$N_{TPC} = 2$	$N_{TPC} = 4$	$N_{TPC} = 8$	
11	1111	11111111	1
00	0000	00000000	0

For slot formats using TFCI, the TFCI value in each radio frame corresponds to a certain combination of bit rates of the DCHs currently in use. This correspondence is (re-)negotiated at each DCH addition/removal. The mapping of the TFCI bits onto slots is described in [3].

When the total bit rate to be transmitted on one downlink CCTrCH exceeds the maximum bit rate for a downlink physical channel, multicode transmission is employed, i.e. several parallel downlink DPCHs are transmitted for one CCTrCH using the same spreading factor. In this case, the Layer 1 control information is put on only the first downlink DPCH. The additional downlink DPCHs belonging to the CCTrCH do not transmit any data during the corresponding time period, see figure 9.

In the case of several CCTrCHs of dedicated type for one UE different spreading factors can be used for each CCTrCH and only one DPCCH would be transmitted for them in the downlink.
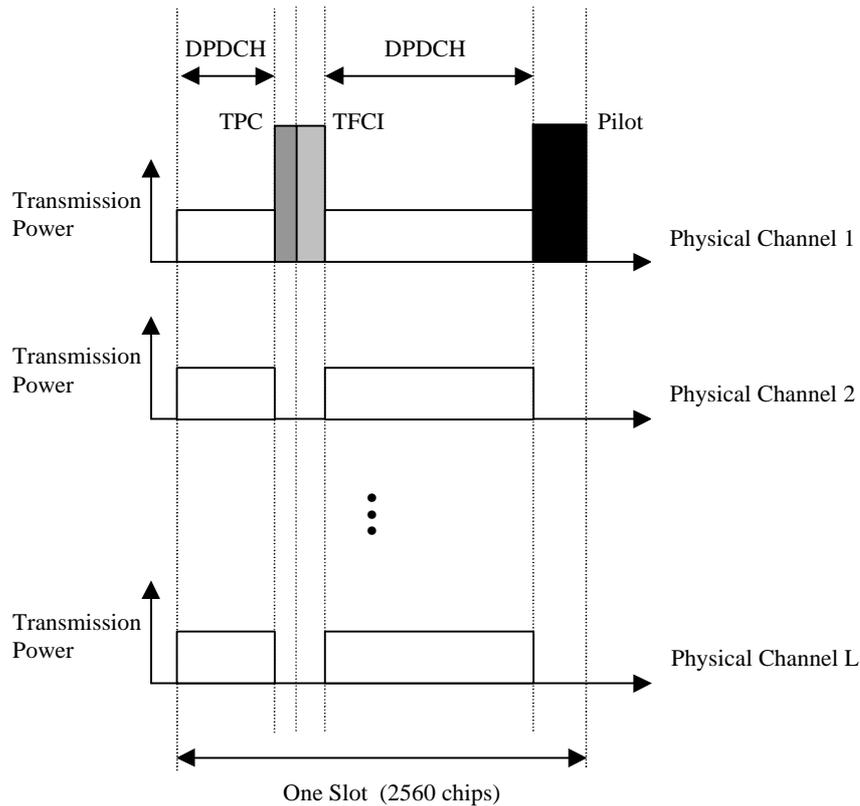
Figure 9: Downlink slot format in case of multi-code transmission

5.3.2.1 STTD for DPCH

The pilot bit pattern for the DPCH channel transmitted on the diversity antenna is given in table 14. The shadowed part indicates pilot bits that are STTD encoded from the corresponding (shadowed) bits in Table 12. For the SF=256 DPCH, if there are only two dedicated pilot bits ($N_{pilot} = 2$ in Tables 12 and 14), they are STTD encoded together with the last two bits (data or DTX) of the second data field (data2) of the slot. STTD encoding for the DPDCH, TPC, and TFCI fields is done as described in section 5.3.1.1.1. For the SF=512 DPCH , the first two bits in each slot, i.e. TPC bits, are not STTD encoded and the same bits are transmitted with equal power from the two antennas. The following four bits are STTD encoded.

Table 14: Pilot pattern of the DPCH channel for the diversity antenna using STTD

	N_{pilot} = 2	N_{pilot} = 4		N_{pilot} = 8				N_{pilot} = 16							
Symbol #	0	0	1	0	1	2	3	0	1	2	3	4	5	6	7
Slot #0	01	01	10	11	00	00	10	11	00	00	10	11	00	00	10
1	10	10	10	11	00	00	01	11	00	00	01	11	10	00	10
2	11	11	10	11	11	00	00	11	11	00	00	11	10	00	11
3	10	10	10	11	10	00	01	11	10	00	01	11	00	00	00
4	00	00	10	11	11	00	11	11	11	00	11	11	01	00	10
5	01	01	10	11	00	00	10	11	00	00	10	11	11	00	00
6	01	01	10	11	10	00	10	11	10	00	10	11	01	00	11
7	00	00	10	11	10	00	11	11	10	00	11	11	10	00	11
8	11	11	10	11	00	00	00	11	00	00	00	11	01	00	01
9	01	01	10	11	01	00	10	11	01	00	10	11	01	00	01
10	11	11	10	11	11	00	00	11	11	00	00	11	00	00	10
11	00	00	10	11	01	00	11	11	01	00	11	11	00	00	01
12	00	00	10	11	10	00	11	11	10	00	11	11	11	00	00
13	10	10	10	11	01	00	01	11	01	00	01	11	10	00	01
14	10	10	10	11	01	00	01	11	01	00	01	11	11	00	11

5.3.2.2 Dedicated channel pilots with closed loop mode transmit diversity

In closed loop mode 1 orthogonal pilot patterns are used between the transmit antennas. Pilot patterns defined in the table 12 will be used on the non-diversity antenna and pilot patterns defined in the table 14 on the diversity antenna. This is illustrated in the figure 10 a which indicates the difference in the pilot patterns with different shading.

In closed loop mode 2 same pilot pattern is used on both of the antennas (see figure 10 b). The pattern to be used is according to the table 12.

(a)

(b)
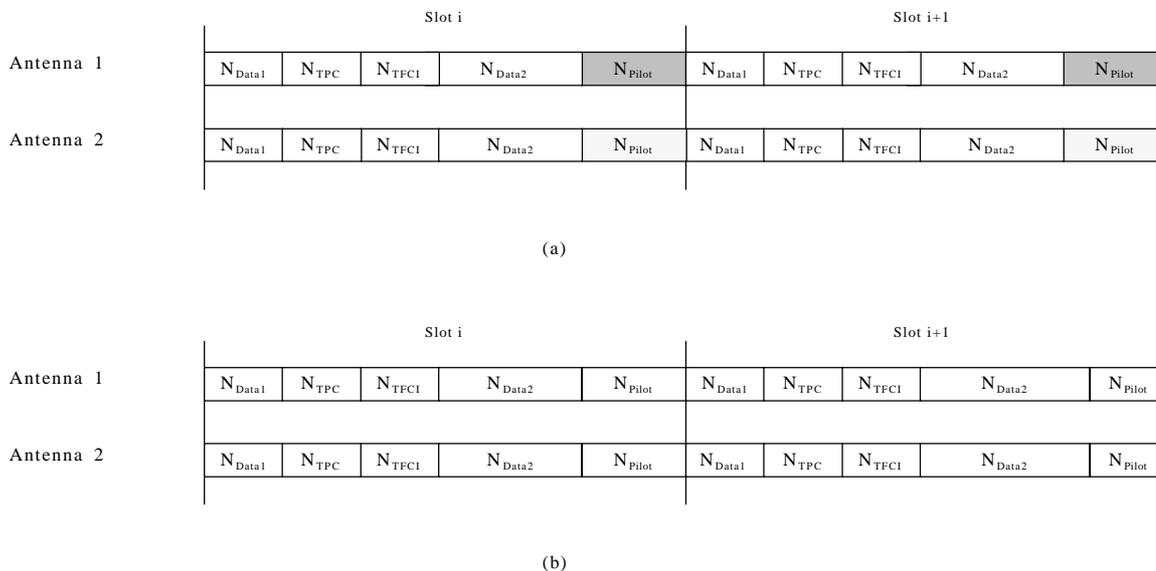
Figure 10: Slot structures for downlink dedicated physical channel diversity transmission.
Structure (a) is used in closed loop mode 1.
Structure (b) is used in closed loop mode 2.
Different shading of the pilots indicate orthogonality of the patterns

5.3.2.3 DL-DPCCH for CPCH

The spreading factor for the UL-DPCCH (message control part) is 256. The spreading factor for the DL-DPCCH (message control part) is 512. The following table 15 shows the DL-DPCCH fields (message control part) which are identical to the first row of table 11 in section 5.3.2.

Table 15: DPDCH and DPCCH fields for CPCH message transmission

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/Frame			Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot		
				DPDCH	DPCCH	TOT		N_{Data1}	N_{Data2}	N_{TFCI}	N_{TPC}	N_{Pilot}
0	15	7.5	512	60	90	150	10	2	2	0	2	4

5.3.3 Common downlink physical channels

5.3.3.1 Common Pilot Channel (CPICH)

The CPICH is a fixed rate (30 kbps, SF=256) downlink physical channel that carries a pre-defined bit/symbol sequence. Figure 11 shows the frame structure of the CPICH.
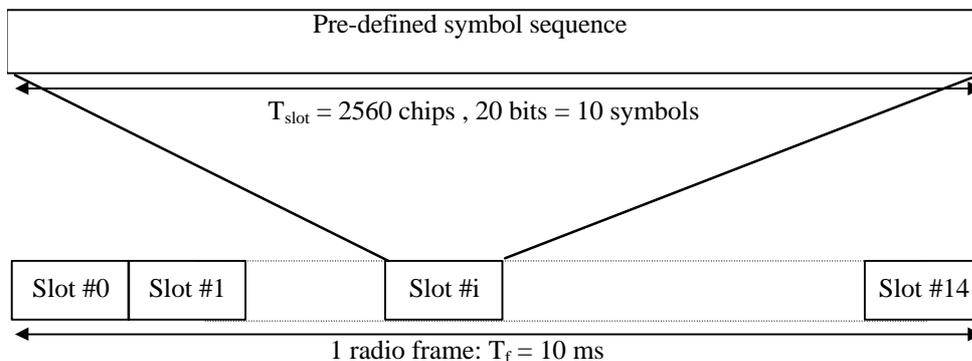
Figure 11: Frame structure for Common Pilot Channel

In case of Transmit Diversity (open or closed loop), the CPICH shall be transmitted from both antennas using the same channelization and scrambling code. In this case, the pre-defined symbol sequence of the CPICH is different for Antenna 1 and Antenna 2, see figure 12. In case of no Transmit Diversity, the symbol sequence of Antenna 1 in figure 12 is used.
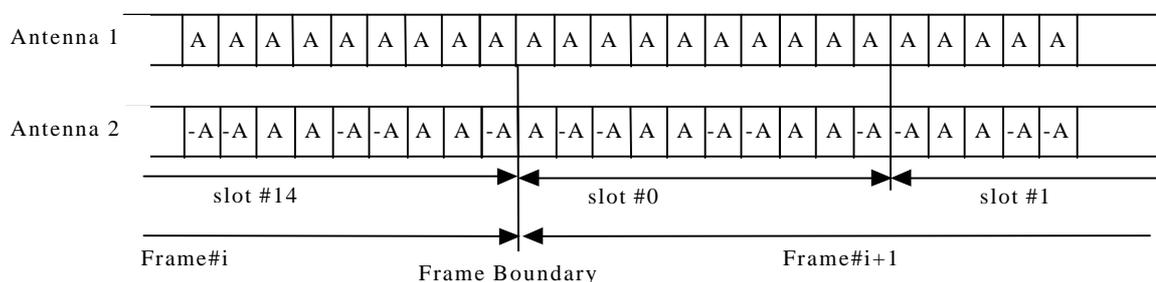
Figure 12: Modulation pattern for Common Pilot Channel (with A = 1+j)

There are two types of Common pilot channels, the Primary and Secondary CPICH. They differ in their use and the limitations placed on their physical features.

5.3.3.1.1   Primary Common Pilot Channel

The Primary Common Pilot Channel has the following characteristics:

- The same channelization code is always used for this channel, see [4]

- Scrambled by the primary scrambling code, see [4]

- One per cell

- Broadcast over the entire cell

The Primary CPICH is the phase reference for the following downlink channels: SCH, Primary CCPCH, AICH, PICH. The Primary CPICH is also the *default* phase reference for all other downlink physical channels.

5.3.3.1.2   Secondary Common Pilot Channel

A Secondary Common Pilot Channel the following characteristics:

- Can use an arbitrary channelization code of SF=256, see [4]

- Scrambled by either the primary or a secondary scrambling code, see [4]

- Zero, one, or several per cell

- May be transmitted over only a part of the cell

- A Secondary CPICH may be the reference for the Secondary CCPCH and the downlink DPCH. If this is the case, the UE is informed about this by higher-layer signalling.

5.3.3.2 Primary Common Control Physical Channel (P-CCPCH)

The Primary CCPCH is a fixed rate (30 kbps, SF=256) downlink physical channels used to carry the BCH.

Figure 13 shows the frame structure of the Primary CCPCH. The frame structure differs from the downlink DPCH in that no TPC commands, no TFCI and no pilot bits are transmitted. The Primary CCPCH is not transmitted during the first 256 chips of each slot. Instead, Primary SCH and Secondary SCH are transmitted during this period (see section 5.3.3.4).
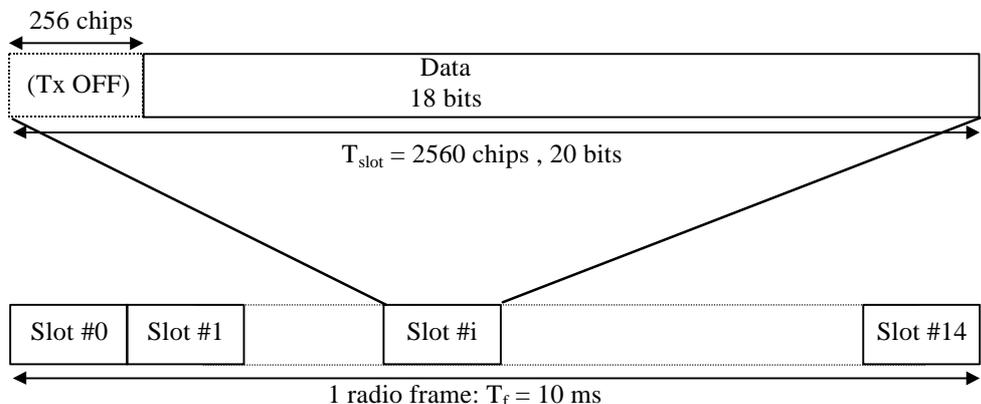
Figure 13: Frame structure for Primary Common Control Physical Channel

5.3.3.2.1 Primary CCPCH structure with STTD encoding

In case the diversity antenna is present in UTRAN and the P-CCPCH is to be transmitted using open loop transmit diversity, the data bits of the P-CCPCH are STTD encoded as given in section 5.3.1.1.1. The last two data bits in even numbered slots are STTD encoded together with the first two data bits in the following slot, except for slot #14 where the two last data bits are not STTD encoded and instead transmitted with equal power from both the antennas, see figure 14. Higher layers signal whether STTD encoding is used for the P-CCPCH or not. In addition, higher layer signalling indicates the presence/absence of STTD encoding on P-CCPCH, by modulating the SCH. During power on and hand over between cells the UE determines the presence of STTD encoding on the P-CCPCH, by either receiving the higher layer message, by demodulating the SCH channel or by a combination of the above two schemes.
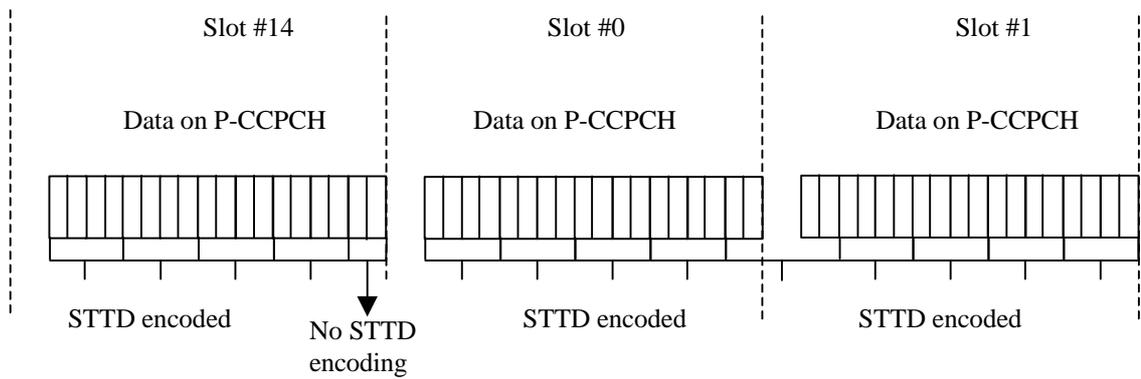
Figure 14: STTD encoding for the data bits of the P-CCPCH

5.3.3.3 Secondary Common Control Physical Channel (S-CCPCH)

The Secondary CCPCH is used to carry the FACH and PCH. There are two types of Secondary CCPCH: those that include TFCI and those that do not include TFCI. It is the UTRAN that determines if a TFCI should be transmitted,

hence making it mandatory for all UEs to support the use of TFCI. The set of possible rates is the same as for the downlink DPCH, see section 5.3.2. The frame structure of the Secondary CCPCH is shown in figure 15.

TFCI N_{TFCI} bits	Data N_{data} bits	Pilot N_{pilot} bits

$$T_{slot} = 2560 \text{ chips}, 20*2^k \text{ bits } (k=0..6)$$

Slot #0	Slot #1		Slot #i		Slot #14

1 radio frame: $T_f = 10$ ms
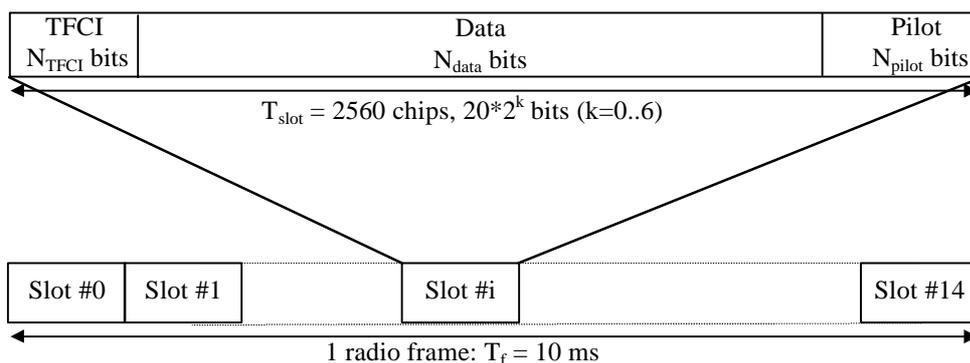
Figure 15: Frame structure for Secondary Common Control Physical Channel

The parameter k in figure 15 determines the total number of bits per downlink Secondary CCPCH slot. It is related to the spreading factor SF of the physical channel as $SF = 256/2^k$. The spreading factor range is from 256 down to 4.

The values for the number of bits per field are given in table 16. The channel bit and symbol rates given in table 16 are the rates immediately before spreading. The pilot patterns are given in table 17.

The FACH and PCH can be mapped to the same or to separate Secondary CCPCHs. If FACH and PCH are mapped to the same Secondary CCPCH, they can be mapped to the same frame. The main difference between a CCPCH and a downlink dedicated physical channel is that a CCPCH is not inner-loop power controlled. The main difference between the Primary and Secondary CCPCH is that the Primary CCPCH has a fixed predefined rate while the Secondary CCPCH can support variable rate with the help of the TFCI field included. Furthermore, a Primary CCPCH is continuously transmitted over the entire cell while a Secondary CCPCH is only transmitted when there is data available and may be transmitted in a narrow lobe in the same way as a dedicated physical channel (only valid for a Secondary CCPCH carrying the FACH).

Table 16: Secondary CCPCH fields

Slot Format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}	N_{pilot}	N_{TFCI}
0	30	15	256	300	20	20	0	0
1	30	15	256	300	20	12	8	0
2	30	15	256	300	20	18	0	2
3	30	15	256	300	20	10	8	2
4	60	30	128	600	40	40	0	0
5	60	30	128	600	40	32	8	0
6	60	30	128	600	40	38	0	2
7	60	30	128	600	40	30	8	2
8	120	60	64	1200	80	72	0	8*
9	120	60	64	1200	80	64	8	8*
10	240	120	32	2400	160	152	0	8*
11	240	120	32	2400	160	144	8	8*
12	480	240	16	4800	320	312	0	8*
13	480	240	16	4800	320	296	16	8*
14	960	480	8	9600	640	632	0	8*
15	960	480	8	9600	640	616	16	8*
16	1920	960	4	19200	1280	1272	0	8*
17	1920	960	4	19200	1280	1256	16	8*

* If TFCI bits are not used, then DTX shall be used in TFCI field.

The pilot symbol pattern is described in table 17. The shadowed part can be used as frame synchronization words. (The symbol pattern of pilot symbols other than the frame synchronization word shall be "11"). In table 17, the transmission order is from left to right. (Each two-bit pair represents an I/Q pair of QPSK modulation.)

Table 17: Pilot Symbol Pattern

	Npilot = 8				Npilot = 16							
Symbol #	0	1	2	3	0	1	2	3	4	5	6	7
Slot #0	11	11	11	10	11	11	11	10	11	11	11	10
1	11	00	11	10	11	00	11	10	11	11	11	00
2	11	01	11	01	11	01	11	01	11	10	11	00
3	11	00	11	00	11	00	11	00	11	01	11	10
4	11	10	11	01	11	10	11	01	11	11	11	11
5	11	11	11	10	11	11	11	10	11	01	11	01
6	11	11	11	00	11	11	11	00	11	10	11	11
7	11	10	11	00	11	10	11	00	11	10	11	00
8	11	01	11	10	11	01	11	10	11	00	11	11
9	11	11	11	11	11	11	11	11	11	00	11	11
10	11	01	11	01	11	01	11	01	11	11	11	10
11	11	10	11	11	11	10	11	11	11	00	11	10
12	11	10	11	00	11	10	11	00	11	01	11	01
13	11	00	11	11	11	00	11	11	11	00	11	00
14	11	00	11	11	11	00	11	11	11	10	11	01

For slot formats using TFCI, the TFCI value in each radio frame corresponds to a certain transport format combination of the FACHs and/or PCHs currently in use. This correspondence is (re-)negotiated at each FACH/PCH addition/removal. The mapping of the TFCI bits onto slots is described in [3].

5.3.3.3.1 Secondary CCPCH structure with STTD encoding

In case the diversity antenna is present in UTRAN and the S-CCPCH is to be transmitted using open loop transmit diversity, the data symbols of the S-CCPCH are STTD encoded as given in Section 5.3.1.1.1. The diversity antenna pilot symbol pattern for the S-CCPCH is given in table 18 below.

Table 18: Pilot symbol pattern for the diversity antenna when STTD encoding is used on the S-CCPCH

	Npilot = 8				Npilot = 16							
Symbol #	0	1	2	3	0	1	2	3	4	5	6	7
Slot #0	11	00	00	10	11	00	00	10	11	00	00	10
1	11	00	00	01	11	00	00	01	11	10	00	10
2	11	11	00	00	11	11	00	00	11	10	00	11
3	11	10	00	01	11	10	00	01	11	00	00	00
4	11	11	00	11	11	11	00	11	11	01	00	10
5	11	00	00	10	11	00	00	10	11	11	00	00
6	11	10	00	10	11	10	00	10	11	01	00	11
7	11	10	00	11	11	10	00	11	11	10	00	11
8	11	00	00	00	11	00	00	00	11	01	00	01
9	11	01	00	10	11	01	00	10	11	01	00	01
10	11	11	00	00	11	11	00	00	11	00	00	10
11	11	01	00	11	11	01	00	11	11	00	00	01
12	11	10	00	11	11	10	00	11	11	11	00	00
13	11	01	00	01	11	01	00	01	11	10	00	01
14	11	01	00	01	11	01	00	01	11	11	00	11

5.3.3.4 Synchronisation Channel (SCH)

The Synchronisation Channel (SCH) is a downlink signal used for cell search. The SCH consists of two sub channels, the Primary and Secondary SCH. The 10 ms radio frames of the Primary and Secondary SCH are divided into 15 slots, each of length 2560 chips. Figure 16 illustrates the structure of the SCH radio frame.
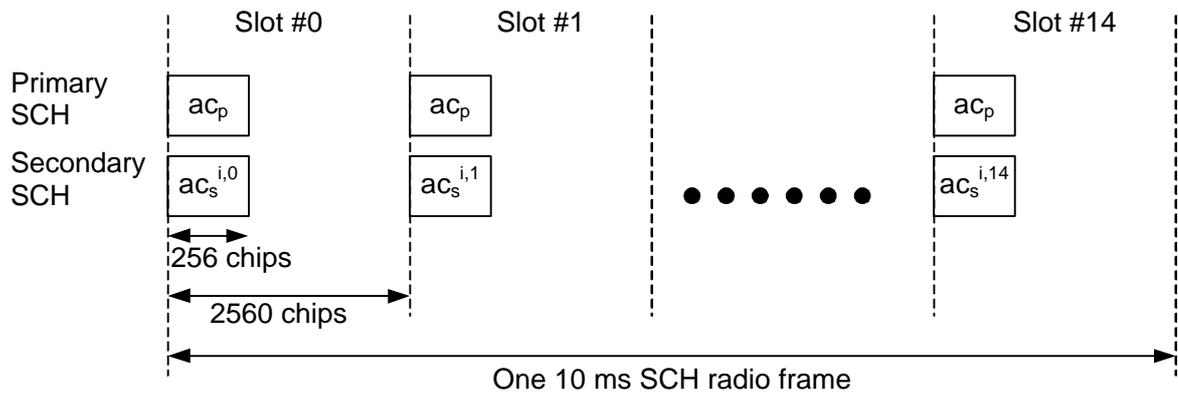
Figure 16: Structure of Synchronisation Channel (SCH)

The Primary SCH consists of a modulated code of length 256 chips, the Primary Synchronisation Code (PSC) denoted c_p in figure 16, transmitted once every slot. The PSC is the same for every cell in the system.

The Secondary SCH consists of repeatedly transmitting a length 15 sequence of modulated codes of length 256 chips, the Secondary Synchronisation Codes (SSC), transmitted in parallel with the Primary SCH. The SSC is denoted $c_s^{i,k}$ in figure 17, where $i = 1, 2, \ldots, 64$ is the number of the scrambling code group, and $k = 0, 1, \ldots, 14$ is the slot number. Each SSC is chosen from a set of 16 different codes of length 256. This sequence on the Secondary SCH indicates which of the code groups the cell's downlink scrambling code belongs to.

The primary and secondary synchronization codes are modulated by the symbol a shown in figure 17, which indicates the presence/ absence of STTD encoding on the P-CCPCH and is given by the following table:

P-CCPCH STTD encoded	a = +1
P-CCPCH not STTD encoded	a = -1

5.3.3.4.1 SCH transmitted by TSTD

Figure 17 illustrates the structure of the SCH transmitted by the TSTD scheme. In even numbered slots both PSC and SSC are transmitted on antenna 1, and in odd numbered slots both PSC and SSC are transmitted on antenna 2.
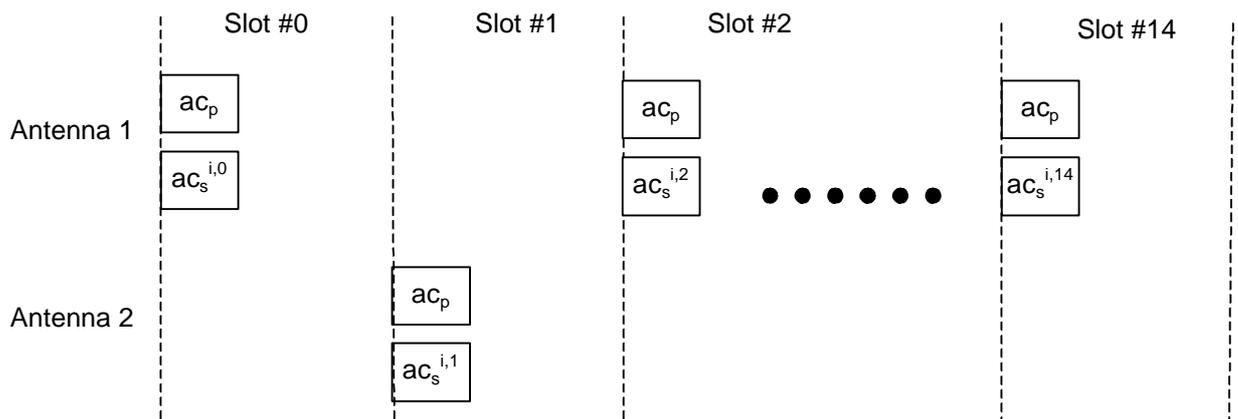
Figure 17: Structure of SCH transmitted by TSTD scheme

5.3.3.5 Physical Downlink Shared Channel (PDSCH)

The Physical Downlink Shared Channel (PDSCH), used to carry the Downlink Shared Channel (DSCH), is shared by users based on code multiplexing. As the DSCH is always associated with a DCH, the PDSCH is always associated with a downlink DPCH.

The frame and slot structure of the PDSCH are shown on figure 18.
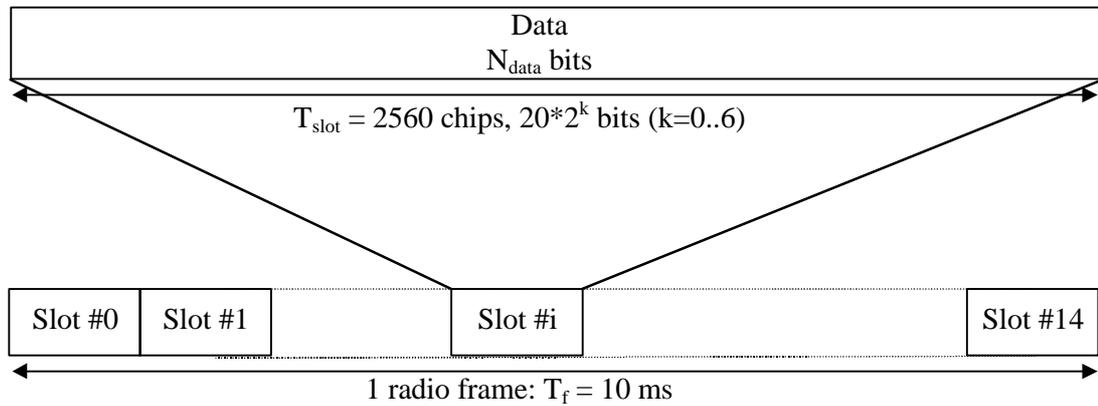
Figure 18: Frame structure for the PDSCH

To indicate for UE that there is data to decode on the DSCH, two signalling methods are possible, either using the TFCI field, or higher layer signalling.

The PDSCH transmission with associated DPCH is a special case of multicode transmission. The PDSCH and DPCH do not have necessary the same spreading factors and for PDSCH the spreading factor may vary from frame to frame. The relevant Layer 1 control information is transmitted on the DPCCH part of the associated DPCH, the PDSCH does not contain physical layer information. The channel bit and symbol rates for PDSCH are given in table 19.

For PDSCH the allowed spreading factors may vary from 256 to 4.

If the spreading factor and other physical layer parameters can vary on a frame-by-frame basis, the TFCI shall be used to inform the UE what are the instantaneous parameters of PDSCH including the channelisation code from the PDSCH OVSF code tree.

A DSCH may be mapped to multiple parallel PDSCHs as well, as negotiated at higher layer prior to starting data transmission. In such a case the parallel PDSCHs shall be operated with frame synchronization between each other.

Table 19: PDSCH fields

Slot format #i	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}
0	30	15	256	300	20	20
1	60	30	128	600	40	40
2	120	60	64	1200	80	80
3	240	120	32	2400	160	160
4	480	240	16	4800	320	320
5	960	480	8	9600	640	640
6	1920	960	4	19200	1280	1280

When transmit diversity is employed for the PDSCH, STTD encoding is used on the data bits as described in section 5.3.1.1.1.

5.3.3.6   Acquisition Indicator Channel (AICH)

The Acquisition Indicator channel (AICH) is a physical channel used to carry Acquisition Indicators (AI). Acquisition Indicator AI_s corresponds to signature s on the PRACH or PCPCH. Note that for PCPCH, the AICH either corresponds to an access preamble or a CD preamble. The AICH corresponding to the access preamble is an AP-AICH and the AICH corresponding to the CD preamble is a CD-AICH. The AP-AICH and CD-AICH use different channelization codes, see further[4], Section 4.3.3.2.

Figure 19 illustrates the structure of the AICH. The AICH consists of a repeated sequence of 15 concecutive *access slots* (AS), each of length 40 bit intervals. Each access slot consists of two parts, an *Acquisition-Indicator* (AI) part consisting of 32 real-valued symbols $a_0, \ldots, a_{31}$ and an unused part consisting of 8 real-valued symbols $a_{32}, \ldots, a_{39}$.

The phase reference for the AICH is the Primary CPICH.

Figure 19: Structure of Acquisition Indicator Channel (AICH)

The real-valued symbols $a_0, a_1, \ldots, a_{31}$ in Figure 19 are given by

$$a_j = \sum_{s=0}^{15} AI_s b_{s,j}$$

where AI_s, taking the values +1, -1, and 0, is the acquisition indicator corresponding to signature s and the sequence $b_{s,0}, \ldots, b_{s,31}$ is given by Table 20.

The real-valued symbols $a_{32}, a_{33}, \ldots, a_{39}$ in Figure 19 are undefined.

In case STTD-based open-loop transmit diversity is applied to AICH, STTD encoding according to section 5.3.1.1.1 is applied to each sequence $b_{s,0}, b_{s,1}, ..., b_{s,31}$ separately before the sequences are combined into AICH symbols $a_0, \ldots, a_{31}$.

Table 20: AICH signature patterns

s	$b_{s,0}, b_{s,1}\ldots, b_{s,31}$																															
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1
2	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1
3	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1
4	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1
5	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1
6	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1
7	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1
8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
9	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1
10	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1
11	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1
12	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1
13	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1
14	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1
15	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1

5.3.3.7   Page Indicator Channel (PICH)

The Page Indicator Channel (PICH) is a fixed rate (SF=256) physical channel used to carry the Page Indicators (PI). The PICH is always associated with an S-CCPCH to which a PCH transport channel is mapped.

Figure 20 illustrates the frame structure of the PICH. One PICH frame of length 10 ms consists of 300 bits ($b_0, b_1, \ldots, b_{299}$). Of these, 288 bits ($b_0, b_1, \ldots, b_{287}$) are used to carry Page Indicators. The remaining 12 bits ($b_{288}, b_{289}, \ldots, b_{299}$) are undefined.

Figure 20: Structure of Page Indicator Channel (PICH)

N Page Indicators $\{PI_0, \ldots, PI_{N-1}\}$ are transmitted in each PICH frame, where N=18, 36, 72, or 144.

The PI calculated by higher layers for use for a certain UE, is mapped to the paging indicator PI_p, where p is computed as a function of the PI computed by higher layers, the SFN of the P-CCPCH radio frame during which the start of the PICH radio frame occurs, and the number of paging indicators per frame (N):

$$p = \left(PI + \left\lfloor \left((18 \times (SFN + \lfloor SFN/8 \rfloor + \lfloor SFN/64 \rfloor + \lfloor SFN/512 \rfloor)) \bmod 144 \right) \times \frac{N}{144} \right\rfloor \right) \bmod N .$$

The mapping from $\{PI_0, \ldots, PI_{N-1}\}$ to the PICH bits $\{b_0, \ldots, b_{287}\}$ are according to table 21.

Table 21: Mapping of Page Indicators (PI) to PICH bits

Number of PI per frame (N)	$PI_p = 1$	$PI_p = 0$
N=18	$\{b_{16p}, \ldots, b_{16p+15}\} = \{1,1,\ldots,1\}$	$\{b_{16p}, \ldots, b_{16p+15}\} = \{0,0,\ldots,0\}$
N=36	$\{b_{8p}, \ldots, b_{8p+7}\} = \{1,1,\ldots,1\}$	$\{b_{8p}, \ldots, b_{8p+7}\} = \{0,0,\ldots,0\}$
N=72	$\{b_{4p}, \ldots, b_{4p+3}\} = \{1, 1,\ldots,1\}$	$\{b_{4p}, \ldots, b_{4p+3}\} = \{0, 0,\ldots,0\}$
N=144	$\{b_{2p}, b_{2p+1}\} = \{1,1\}$	$\{b_{2p}, b_{2p+1}\} = \{0,0\}$

If a Paging Indicator in a certain frame is set to "1" it is an indication that UEs associated with this Page Indicator should read the corresponding frame of the associated S-CCPCH.

When transmit diversity is employed for the PICH, STTD encoding is used on the PICH bits as described in section 5.3.1.1.1.

6 Mapping of transport channels onto physical channels

Figure 21 summarises the mapping of transport channels onto physical channels.

Transport Channels   **Physical Channels**

DCH ——————————— Dedicated Physical Data Channel (DPDCH)

Dedicated Physical Control Channel (DPCCH)

RACH——————————— Physical Random Access Channel (PRACH)

CPCH ——————————— Physical Common Packet Channel (PCPCH)

Common Pilot Channel (CPICH)

BCH ——————————— Primary Common Control Physical Channel (P-CCPCH)

FACH——————————— Secondary Common Control Physical Channel (S-CCPCH)

PCH ——

Synchronisation Channel (SCH)

DSCH ——————————— Physical Downlink Shared Channel (PDSCH)

Acquisition Indication Channel (AICH)

Page Indication Channel (PICH)

Figure 21: Transport-channel to physical-channel mapping

The DCHs are coded and multiplexed as described in [3] , and the resulting data stream is mapped sequentially (first-in-first-mapped) directly to the physical channel(s). The mapping of BCH and FACH/PCH is equally straightforward, where the data stream after coding and interleaving is mapped sequentially to the Primary and Secondary CCPCH respectively. Also for the RACH, the coded and interleaved bits are sequentially mapped to the physical channel, in this case the message part of the random access burst on the PRACH.

7 Timing relationship between physical channels

7.1 General

The P-CCPCH, on which the cell SFN is transmitted, is used as timing reference for all the physical channels, directly for downlink and indirectly for uplink.

Figure 22 below describes the frame timing of the downlink physical channels. For the AICH the access slot timing is included. Timing for uplink physical channels is given by the downlink timing, as described in the following sections.
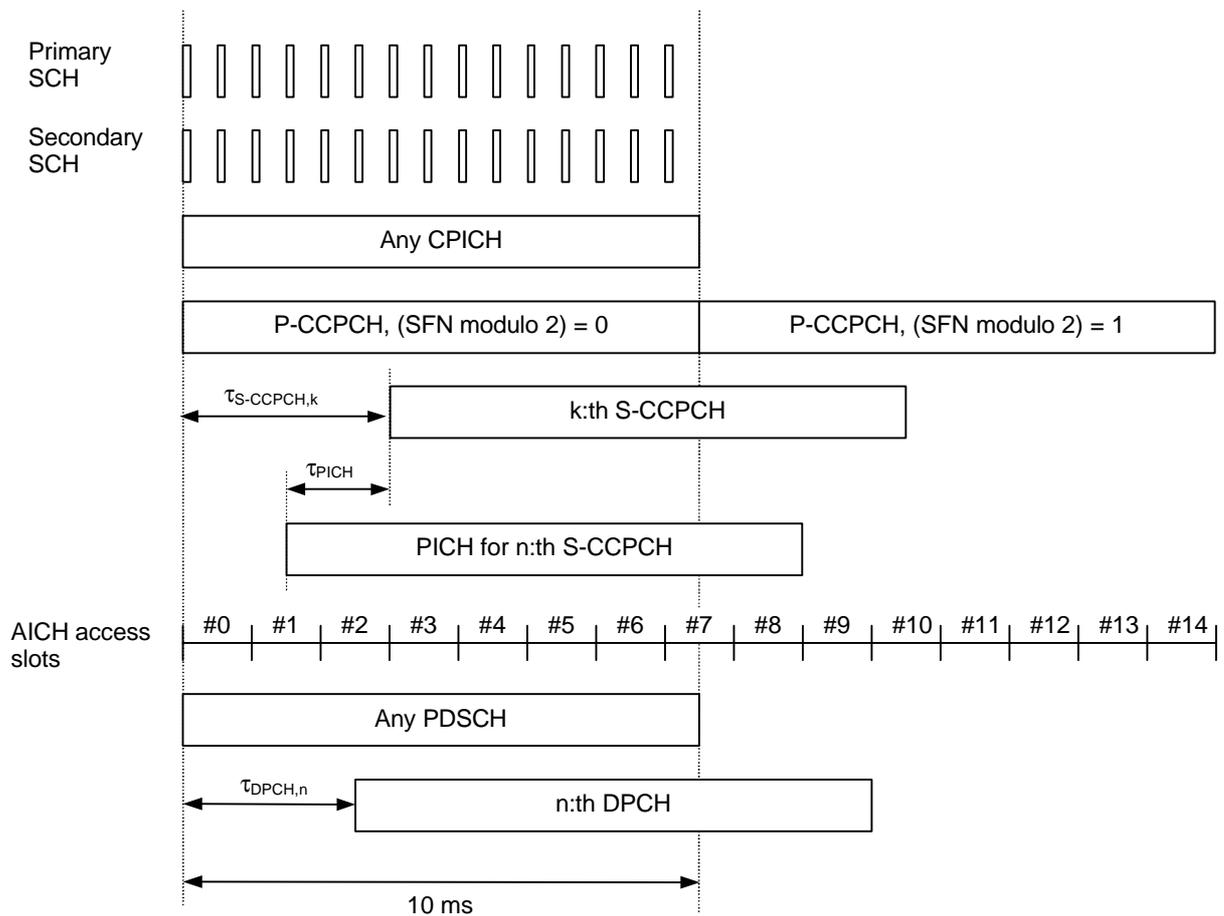
Figure 22: Frame timing and access slot timing of downlink physical channels

In figure 22 the following applies:

- SCH (primary and secondary), CPICH (primary and secondary), P-CCPCH, and PDSCH have identical frame timings.

- The S-CCPCH timing may be different for different S-CCPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{\text{S-CCPCH},k} = T_k \times 256$ chip, $T_k \in \{0, 1, \ldots, 149\}$.

- The PICH timing is $\tau_{\text{PICH}} = 7680$ chips prior to its corresponding S-CCPCH frame timing. The PICH timing relation to the S-CCPCH is described more in section 7.2.

- The AICH access slot #0 starts the same time as a P-CCPCH frame with (SFN modulo 2) = 0. The AICH/PRACH and AICH/PCPCH timing is described in sections 7.3 and 7.4 respectively.

- The PDSCH timing relative the DPCH timing is described in section 7.5.

- The DPCH timing may be different for different DPCHs, but the offset from the P-CCPCH frame timing is a multiple of 256 chips, i.e. $\tau_{\text{DPCH},n} = T_n \times 256$ chip, $T_n \in \{0, 1, \ldots, 149\}$. The DPCH (DPCCH/DPDCH) timing relation with uplink DPCCH/DPDCHs is described in section 7.6.

7.2 PICH/S-CCPCH timing relation

Figure 23 illustrates the timing between a PICH frame and its associated S-CCPCH frame. A paging indicator set in a PICH frame means that the paging message is transmitted on the PCH in the S-CCPCH frame starting τ_{PICH} chips after the transmitted PICH frame. τ_{PICH} is defined in section 7.1.
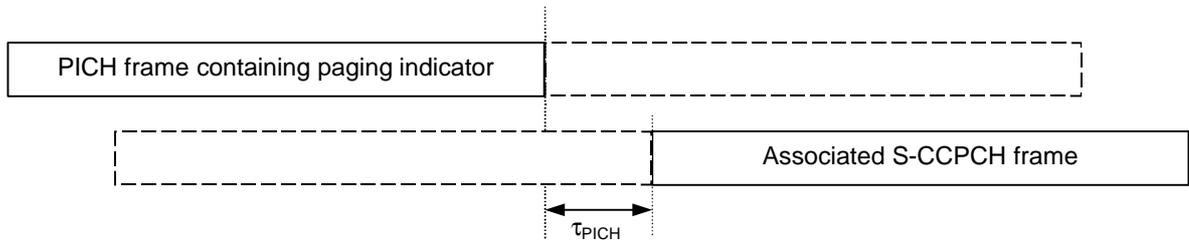
Figure 23: Timing relation between PICH frame and associated S-CCPCH frame

7.3 PRACH/AICH timing relation

The downlink AICH is divided into downlink access slots, each access slot is of length 5120 chips. The downlink access slots are time aligned with the P-CCPCH as described in section 7.1.

The uplink PRACH is divided into uplink access slots, each access slot is of length 5120 chips. Uplink access slot number n is transmitted from the UE τ_{p-a} chips prior to the reception of downlink access slot number n, $n = 0, 1, \ldots, 14$.

Transmission of downlink acquisition indicators may only start at the beginning of a downlink access slot. Similarly, transmission of uplink RACH preambles and RACH message parts may only start at the beginning of an uplink access slot.

The PRACH/AICH timing relation is shown in figure 24.
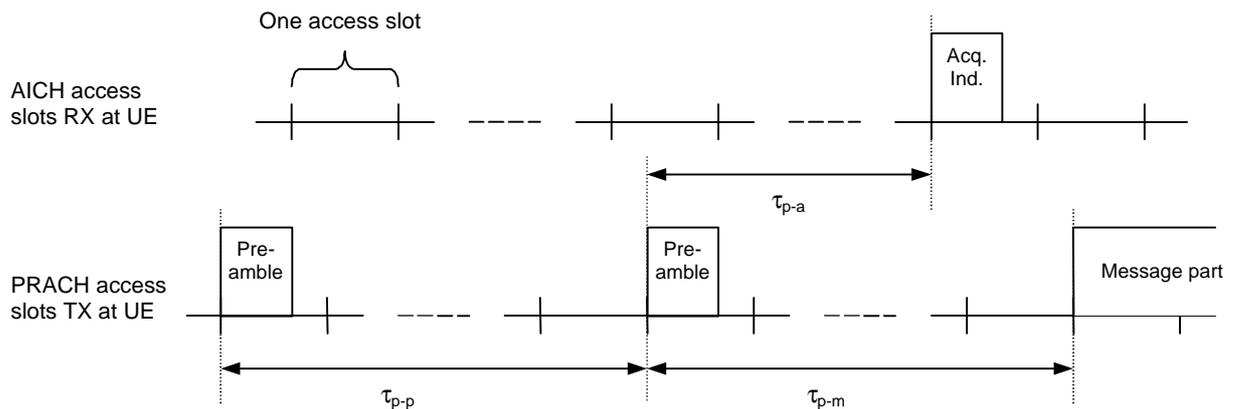
Figure 24: Timing relation between PRACH and AICH as seen at the UE

The preamble-to-preamble distance τ_{p-p} shall be larger than or equal to the minimum preamble-to-preamble distance $\tau_{p-p,min}$, i.e. $\tau_{p-p} \geq \tau_{p-p,min}$.

In addition to $\tau_{p-p,min}$, the preamble-to-AI distance τ_{p-a} and preamble-to-message distance τ_{p-a} are defined as follows:

- when AICH_Transmission_Timing is set to 0, then

    $\tau_{p-p,min} = 15360$ chips (3 access slots)

    $\tau_{p-a} = 7680$ chips

    $\tau_{p-m} = 15360$ chips (3 access slots)

- when AICH_Transmission_Timing is set to 1, then

    $\tau_{p-p,min} = 20480$ chips (4 access slots)

    $\tau_{p-a} = 12800$ chips

    $\tau_{p-m} = 20480$ chips (4 access slots)

7.4 PCPCH/AICH timing relation

Transmission of random access bursts on the PCPCH is aligned with access slot times. The timing of the access slots is derived from the received Primary CCPCH timing The transmit timing of access slot n starts n×20/15 ms after the frame boundary of the received Primary CCPCH, where n = 0, 1, …,14. In addition, transmission of access preambles in PCPCH is limited to the allocated access slot subchannel group which is assigned by higher layer signalling to each CPCH set. Twelve access slot subchannels are defined and PCPCH may be allocated all subchannel slots or any subset of the twelve subchannel slots. The access slot subchannel identification is identical to that for the RACH and is described in table 6 of section 6.1 of [5].

Everything in the previous section [PRACH/AICH] applies to this section as well. The timing relationship between preambles, AICH, and the message is the same as PRACH/AICH. Note that the collision resolution preambles follow the access preambles in PCPCH/AICH. However, the timing relationships between CD-Preamble and CD-AICH is identical to RACH Preamble and AICH. The timing relationship between CD-AICH and the Power Control Preamble in CPCH is identical to AICH to message in RACH. The T_{cpch} timing parameter is identical to the PRACH/AICH transmission timing parameter. When T_{cpch} is set to zero or one, the following PCPCH/AICH timing values apply:

Note that a1 corresponds to AP-AICH and a2 corresponds to CD-AICH.

τ_{p-p} =   Time to next available access slot, between Access Preambles.

         Minimum time = 15360 chips + 5120 chips X Tcpch

         Maximum time = 5120 chips X 12 = 61440 chips

         Actual time is time to next slot (which meets minimum time criterion) in allocated access slot subchannel group.

τ_{p-a1} =   Time between Access Preamble and AP-AICH has two alternative values: 7680 chips or 12800 chips, depending on T_{cpch}

τ_{a1-cdp} =   Time between receipt of AP-AICH and transmission of the CD Preamble has one value: 7680 chips.

τ_{p-cdp} =   Time between the last AP and CD Preamble. is either 3 or 4 access slots, depending on T_{cpch}

τ_{cdp-a2} =   Time between the CD Preamble and the CD-AICH has two alternative values: 7680 chips or 12800 chips,   depending on T_{cpch}

$\tau_{cdp-pcp}$ =   Time between CD Preamble and the start of the Power Control Preamble is either 3 or 4 access slots, depending on T_{cpch}.

Figure 25 illustrates the PCPCH/AICH timing relationship when T_{cpch} is set to 0 and all access slot subchannels are available for PCPCH.
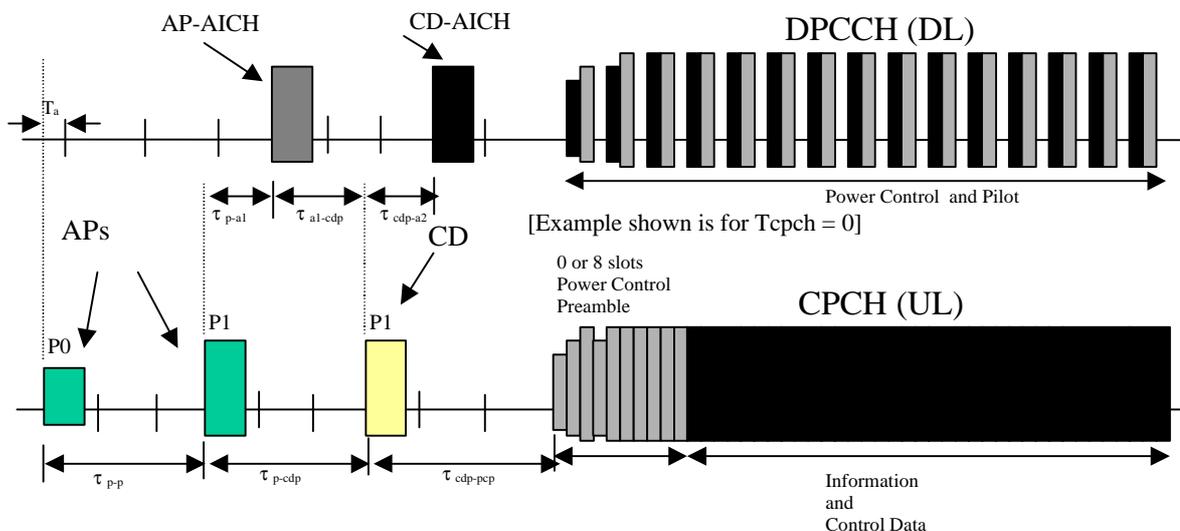

Figure 25: Timing of PCPCH and AICH transmission as seen by the UE, with $T_{cpch}= 0$

7.5 DPCH/PDSCH timing

The relative timing between a DPCH frame and the associated PDSCH frame is shown in figure 26.
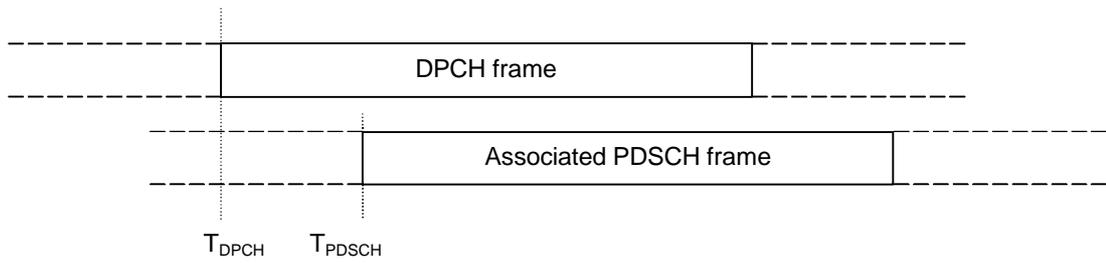
Figure 26: Timing relation between DPCH frame and associated PDSCH frame

The start of a DPCH frame is denoted T_{DPCH} and the start of the associated PDSCH frame is denoted T_{PDSCH}. Any DPCH frame is associated to one PDSCH frame through the relation -35840 chips $< T_{DPCH} - T_{PDSCH} \leq 2560$ chips, i.e. the associated PDSCH frame starts anywhere between 1 slot before or up to 14 slots behind the DPCH.

7.6 DPCCH/DPDCH timing relations

7.6.1 Uplink

In uplink the DPCCH and all the DPDCHs transmitted from one UE have the same frame timing.

7.6.2 Downlink

In downlink, the DPCCH and all the DPDCHs carrying CCTrCHs of dedicated type to one UE have the same frame timing.

7.6.3 Uplink/downlink timing at UE

At the UE, the uplink DPCCH/DPDCH frame transmission takes place approximately T_0 chips after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame. T_0 is a constant defined to be 1024 chips. More information about the uplink/downlink timing relation and meaning of T_0 can be found in [5].

~~In case of USTS, the uplink DPCCH/DPDCH frame transmission for Initial synchronization takes place $T_0+T_{INIT\_SYNC}$ after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame where T_{INIT_SYNC} is Initial synchronization time delivered by UTRAN. However the uplink DPCCH/DPDCH frame transmission for Tracking of USTS takes place approximately $T_0+T_{INIT\_SYNC}\pm\delta T$ after the reception of the first significant path of the corresponding downlink DPCCH/DPDCH frame where δT is the resultant timing adjustment due to the timing control by TAB command bits. More information on T_{INIT_SYNC} and δT can be found in section 9.2 and 9.3 of [5]~~

7.7 Timing relations for initialisation of channels

Figure 27 shows the timing relationships between the physical channels involved in the initialisation of a DCH.

The maximum time permitted for the UE to decode the relevant FACH frame before the first frame of the DPCCH is received shall be $T_{B-min} = 38400$ chips (i.e.15 slots).

The downlink DPCCH shall commence at a time T_B after the end of the relevant FACH frame, where $T_B \geq T_{B-min}$ according to the following equation:

$$T_B = (T_n - T_k) \times 256 - N_{pcp} \times 2560 + N_{offset\_1} \times 38400 \text{ chips}, \text{ where:}$$

N_{pcp} is a higher layer parameter set by the network, and represents the length (in slots) of the power control preamble (see [5], section 5.1.2.4).

N_{offset_1} is a parameter derived from the activation time set by higher layers. In order that $T_B \geq T_{B-min}$, N_{offset_1} shall be an integer number of frames such that:

$$N_{\text{offset\_1}} \geq \begin{cases} 1 & \text{when } T_n - T_k \geq \dfrac{T_{B-\min}}{256} + 10 N_{pcp} - 150 \\[3mm] 2 & \text{when } \dfrac{T_{B-\min}}{256} + 10 N_{pcp} - 300 \leq T_n - T_k < \dfrac{T_{B-\min}}{256} + 10 N_{pcp} - 150 \\[3mm] 3 & \text{when } T_n - T_k < \dfrac{T_{B-\min}}{256} + 10 N_{pcp} - 300 \end{cases}$$

T_n and T_k are parameters defining the timing of the frame boundaries on the DL DPCCH and S-CCPCH respectively (see section 7.1). These parameters are provided by higher layers.

The uplink DPCCH shall commence at a time T_C after the end of the relevant FACH frame, where

$T_C = T_B + T_0 + N_{offset\_2} \times 38400$ chips , where T_0 is as in section 7.6.3 and $N_{\text{offset\_2}}$ is a UE-specific higher-layer parameter which shall be an integer number of frames greater than or equal to zero.

3GPP TSG RAN WG1 Meeting #11
San Diego, USA, Feb 29th – Mar 3rd 2000

Document **R1-00-0422**
e.g. for 3GPP use the format TP-99xxx
or for SMG, use the format P-99-xxx

CHANGE REQUEST

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25.213	CR	**032**	Current Version:	3.1.1

GSM (AA.BB) or 3G (AA.BBB) specification number ↑ 　　　 *↑ CR number as allocated by MCC support team*

For submission to:　**TSG-RAN #7**　　for approval **X**　　　　strategic ☐　*(for SMG*
list expected approval meeting # here　　for information ☐　　　non-strategic ☐　*use only)*
　　　　↑

Form: CR cover sheet, version 2 for 3GPP and SMG　*The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc*

Proposed change affects:　　(U)SIM ☐　ME **X**　UTRAN / Radio **X**　Core Network ☐
(at least one should be marked with an X)

Source:	SK Telecom	**Date:**	2000-03-03

Subject:	Clean up of USTS related specifications

Work item:	

Category:　F Correction　　　　　　　　　　　　　　**X**　**Release:**　Phase 2 ☐
　　　　　　　A Corresponds to a correction in an earlier release ☐　　　　Release 96 ☐
(only one category　B Addition of feature ☐　　　　　　　　　　　　　Release 97 ☐
shall be marked　C Functional modification of feature ☐　　　　　　Release 98 ☐
with an X)　　D Editorial modification ☐　　　　　　　　　　　Release 99 **X**
　　　　　　　　　　　　　　　　　　　　　　　　　　　　Release 00 ☐

Reason for change:	USTS is Release-00 item. Therefore USTS related specifications shall be removed in Release-99.

Clauses affected:	3.2 4.3.1.2

Other specs affected:　Other 3G core specifications ☐　→ List of CRs:
　　　　　　　　Other GSM core specifications ☐　→ List of CRs:
　　　　　　　　MS test specifications ☐　→ List of CRs:
　　　　　　　　BSS test specifications ☐　→ List of CRs:
　　　　　　　　O&M specifications ☐　→ List of CRs:

Other comments:	

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<--------- double-click here for help and instructions on how to create a CR.

1   Scope

The present document describes spreading and modulation for UTRA Physical Layer FDD mode.

2   References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.

- For a specific reference, subsequent revisions do not apply.

- For a non-specific reference, the latest version applies.

[1]   3G TS 25.201: "Physical layer - general description".

[2]   3G TS 25.211: "Physical channels and mapping of transport channels onto physical channels (FDD) ."

[3]   3G TS 25.101: "UE Radio transmission and Reception (FDD)".

[4]   3G TS 25.104: "UTRA (BS) FDD; Radio transmission and Reception".

3   Symbols and abbreviations

3.1   Symbols

For the purposes of the present document, the following symbols apply:

$C_{ch,SF,n}$:	n:th channelisation code with spreading factor SF
$C_{pre,n,s}$:	PRACH preamble code for n:th preamble scrambling code and signature s
$C_{c\text{-}acc,n,s}$:	PCPCH access preamble code for n:th preamble scrambling code and signature s
$C_{c\text{-}cd,n,s}$:	PCPCH CD preamble code for n:th preamble scrambling code and signature s
$C_{sig,s}$:	PRACH/PCPCH signature code for signature s
$S_{long,n}$:	n:th DPCCH/DPDCH long uplink scrambling code
$S_{short,n}$:	n:th DPCCH/DPDCH short uplink scrambling code
$S_{r\text{-}pre,n}$:	n:th PRACH preamble scrambling code
$S_{r\text{-}msg,n}$:	n:th PRACH message scrambling code
$S_{c\text{-}acc}$:	n:th PCPCH access preamble scrambling code
$S_{c\text{-}cd}$:	n:th PCPCH CD preamble scrambling code
$S_{c\text{-}msg,n}$:	n:th PCPCH message scrambling code
$S_{dl,n}$:	DL scrambling code
C_{psc}:	PSC code
$C_{ssc,n}$:	n:th SSC code

3.2   Abbreviations

For the purposes of the present document, the following abbreviations apply:

AICH	Acquisition Indicator Channel
AP	Access Preamble
BCH	Broadcast Control Channel
CCPCH	Common Control Physical Channel
CD	Collision Detection
CPCH	Common Packet Channel
CPICH	Common Pilot Channel
DCH	Dedicated Channel

DPCH	Dedicated Physical Channel
DPCCH	Dedicated Physical Control Channel
DPDCH	Dedicated Physical Data Channel
FDD	Frequency Division Duplex
Mcps	Mega Chip Per Second
OVSF	Orthogonal Variable Spreading Factor (codes)
PDSCH	Physical Dedicated Shared Channel
PICH	Page Indication Channel
PRACH	Physical Random Access Channel
PSC	Primary Synchronisation Code
RACH	Random Access Channel
SCH	Synchronisation Channel
SSC	Secondary Synchronisation Code
SF	Spreading Factor
UE	User Equipment
~~USTS~~	~~Uplink Synchronous Transmission Scheme~~

4 Uplink spreading and modulation

4.1 Overview

Spreading is applied to the physical channels. It consists of two operations. The first is the channelization operation, which transforms every data symbol into a number of chips, thus increasing the bandwidth of the signal. The number of chips per data symbol is called the Spreading Factor (SF). The second operation is the scrambling operation, where a scrambling code is applied to the spread signal.

With the channelization, data symbols on so-called I- and Q-branches are independently multiplied with an OVSF code. With the scrambling operation, the resultant signals on the I- and Q-branches are further multiplied by complex-valued scrambling code, where I and Q denote real and imaginary parts, respectively.

4.2 Spreading

4.2.1 DPCCH/DPDCH)

Figure 1 illustrates the principle of the uplink spreading of DPCCH and DPDCHs. The binary DPCCH and DPDCHs to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, while the binary value "1" is mapped to the real value –1. The DPCCH is spread to the chip rate by the channelization code c_c, while the n:th DPDCH called $DPDCH_n$ is spread to the chip rate by the channelization code $c_{d,n}$. One DPCCH and up to six parallel DPDCHs can be transmitted simultaneously, i.e. $0 \leq n \leq 6$.
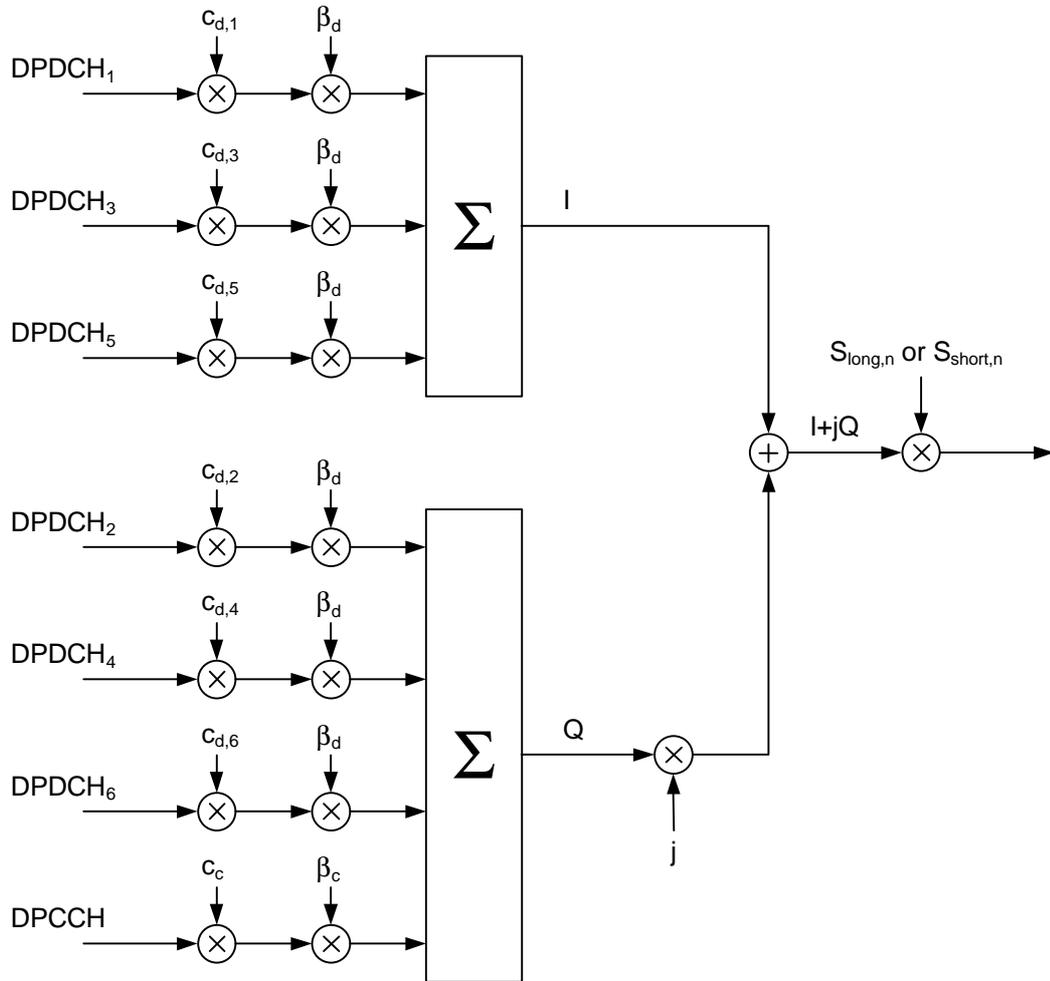
Figure 1: Spreading for uplink DPCCH and DPDCHs

After channelization, the real-valued spread signals are weighted by gain factors, β_c for DPCCH and β_d for all DPDCHs.

At every instant in time, at least one of the values β_c and β_d has the amplitude 1.0. The β-values are quantized into 4 bit words. The quantization steps are given in table 1.

Table 1: The quantization of the gain parameters

Signalling values for β_c and β_d	Quantized amplitude ratios β_c and β_d
15	1.0
14	0.9333
13	0.8666
12	0.8000
11	0.7333
10	0.6667
9	0.6000
8	0.5333
7	0.4667
6	0.4000
5	0.3333
4	0.2667
3	0.2000
2	0.1333
1	0.0667
0	Switch off

After the weighting, the stream of real-valued chips on the I- and Q-branches are then summed and treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code

$S_{long,n}$ or $S_{short,n}$, depending on if long or short scrambling codes are used. The scrambling code is applied aligned with the radio frames, i.e. the first scrambling chip corresponds to the beginning of a radio frame.

4.2.2   PRACH

4.2.2.1   PRACH preamble part

The PRACH preamble part consist of a complex-valued code, described in section 4.3.3.

4.2.2.2   PRACH message part

Figure 2 illustrates the principle of the spreading and scrambling of the PRACH message part, consisting of data and control parts. The binary control and data parts to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, while the binary value "1" is mapped to the real value –1. The control part is spread to the chip rate by the channelization code c_c, while the data part is spread to the chip rate by the channelization code c_d.
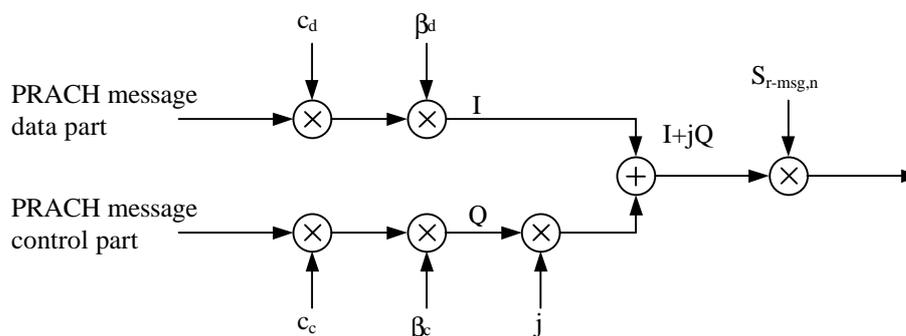

Figure 2: Spreading of PRACH message part

After channelization, the real-valued spread signals are weighted by gain factors, β_c for the control part and β_d for the data part. At every instant in time, at least one of the values β_c and β_d has the amplitude 1.0. The β-values are quantized into 4 bit words. The quantization steps are given in section 4.2.1.

After the weighting, the stream of real-valued chips on the I- and Q-branches are treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code $S_{r-msg,n}$. The 10 ms scrambling code is applied aligned with the 10 ms message part radio frames, i.e. the first scrambling chip corresponds to the beginning of a message part radio frame.

4.2.3   PCPCH

4.2.3.1   PCPCH preamble part

The PCPCH preamble part consist of a complex-valued code, described in section 4.3.4.

4.2.3.2   PCPCH message part

Figure 3 illustrates the principle of the spreading of the PCPCH message part, consisting of data and control parts. The binary control and data parts to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, while the binary value "1" is mapped to the real value –1. The control part is spread to the chip rate by the channelization code c_c, while the data part is spread to the chip rate by the channelization code c_d.
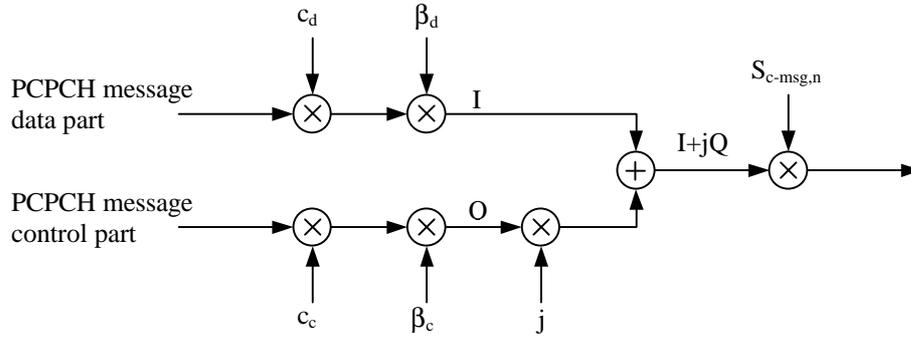
Figure 3: Spreading of PCPCH message part

After channelization, the real-valued spread signals are weighted by gain factors, β_c for the control part and β_d for the data part. At every instant in time, at least one of the values β_c and β_d has the amplitude 1.0. The β-values are quantized into 4 bit words. The quantization steps are given in section 4.2.1.

After the weighting, the stream of real-valued chips on the I- and Q-branches are treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code $S_{c\text{-msg,}n}$. The 10 ms scrambling code is applied aligned with the 10 ms message part radio frames, i.e. the first scrambling chip corresponds to the beginning of a message part radio frame.

4.3 Code generation and allocation

4.3.1 Channelization codes

4.3.1.1 Code definition

The channelization codes of figure 1 are Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between a user's different physical channels. The OVSF codes can be defined using the code tree of figure 4.
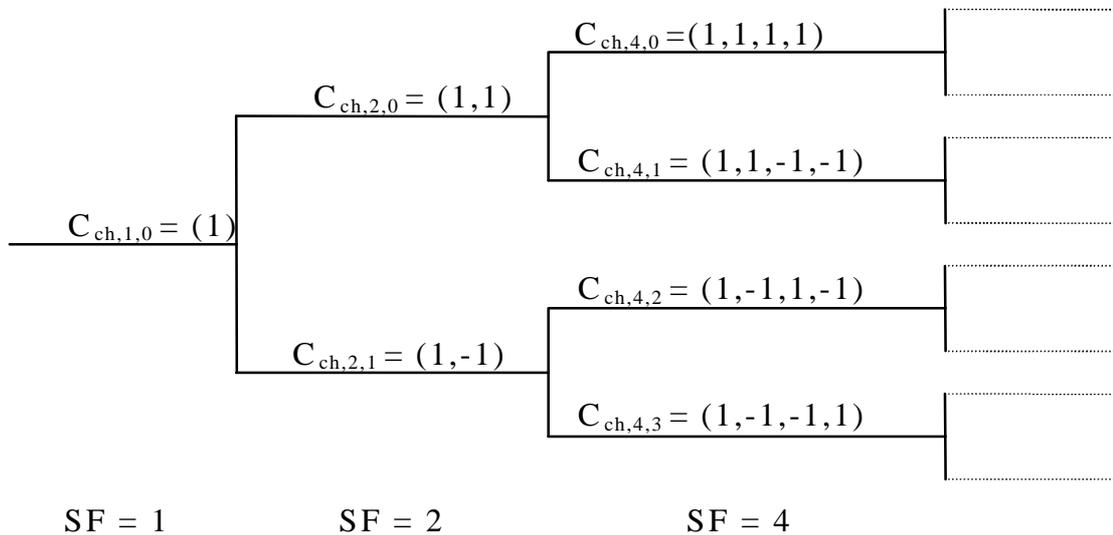

Figure 4: Code-tree for generation of Orthogonal Variable Spreading Factor (OVSF) codes

In figure 4, the channelization codes are uniquely described as $C_{ch,SF,k}$, where SF is the spreading factor of the code and k is the code number, $0 \leq k \leq SF\text{-}1$.

Each level in the code tree defines channelization codes of length SF, corresponding to a spreading factor of SF in figure 4.

The generation method for the channelization code is defined as:

$$C_{ch,1,0} = 1,$$

$$\begin{bmatrix} C_{ch,2,0} \\ C_{ch,2,1} \end{bmatrix} = \begin{bmatrix} C_{ch,1,0} & C_{ch,1,0} \\ C_{ch,1,0} & -C_{ch,1,0} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$\begin{bmatrix} C_{ch,2^{(n+1)},0} \\ C_{ch,2^{(n+1)},1} \\ C_{ch,2^{(n+1)},2} \\ C_{ch,2^{(n+1)},3} \\ \vdots \\ C_{ch,2^{(n+1)},2^{(n+1)}-2} \\ C_{ch,2^{(n+1)},2^{(n+1)}-1} \end{bmatrix} = \begin{bmatrix} C_{ch,2^n,0} & C_{ch,2^n,0} \\ C_{ch,2^n,0} & -C_{ch,2^n,0} \\ C_{ch,2^n,1} & C_{ch,2^n,1} \\ C_{ch,2^n,1} & -C_{ch,2^n,1} \\ \vdots & \vdots \\ C_{ch,2^n,2^n-1} & C_{ch,2^n,2^n-1} \\ C_{ch,2^n,2^n-1} & -C_{ch,2^n,2^n-1} \end{bmatrix}$$

The leftmost value in each channelization code word corresponds to the chip transmitted first in time.

4.3.1.2 Code allocation for DPCCH/DPDCH

For the DPCCH and DPDCHs the following applies:

- The DPCCH is always spread by code $c_c = C_{ch,256,0}$.

- When only one DPDCH is to be transmitted, DPDCH$_1$ is spread by code $c_{d,1} = C_{ch,SF,k}$ where SF is the spreading factor of DPDCH$_1$ and k= SF / 4

- When more than one DPDCH is to be transmitted, all DPDCHs have spreading factors equal to 4. DPDCH$_n$ is spread by the the code $c_{d,n} = C_{ch,4,k}$, where $k = 1$ if $n \in \{1, 2\}$, $k = 3$ if $n \in \{3, 4\}$, and $k = 2$ if $n \in \{5, 6\}$.

~~In case of USTS, for the DPCCH, the UTRAN assigns a node number v_c ($0 \le v_c \le 255$) in the code-tree that corresponds to a channelization code of length 256. For a DPDCH, the UTRAN assigns a node number v_d ($0 \le v_d \le L-1$) in the code tree that corresponds to a channelization code of length L (i.e., SF for the UE). The sub-tree below the assigned node is used for spreading of DPDCH. When more than one DPDCH is to be transmitted, all DPDCHs have spreading factors equal to 4. In this case, the UTRAN assigns node numbers v_{d1}, v_{d2}, and v_{d3} ($0 \le v_{d1}, v_{d2},$ and $v_{d3} \le 3$) that correspond to channelization codes of length 4. The DPCCH is always spread by code $C_{ch,0} = C_{ch,256,k}$, where k=v_c.~~

- ~~When only one DPDCH is to be transmitted, DPDCH$_1$ is spread by code $C_{ch,SF,k}$, where SF is the spreading factor of DPDCH$_1$ and k= v_d*SF/L.~~

- ~~When more than one DPDCH is to be transmitted, all DPDCHs have spreading factors equal to 4 (i.e., L=4). DPDCH$_n$ is spread by the code $C_{ch,n} = C_{ch,4,k}$, where $k = v_{d1}$ if $n \in \{1, 2\}$, $k = v_{d2}$ if $n \in \{3, 4\}$, and $k = v_{d3}$ if $n \in \{5, 6\}$.~~

4.3.1.3 Code allocation for PRACH message part

The preamble signature s, $1 \le s \le 16$, points to one of the 16 nodes in the code-tree that corresponds to channelization codes of length 16. The sub-tree below the specified node is used for spreading of the message part. The control part is spread with the channelization code c_c (as shown in section 4.2.2.2) of spreading factor 256 in the lowest branch of the sub-tree, i.e. $c_c = C_{ch,256,m}$ where m = 16(s – 1) + 15. The data part uses any of the channelization codes from spreading factor 32 to 256 in the upper-most branch of the sub-tree. To be exact, the data part is spread by channelization code $c_d = C_{ch,SF,m}$ and SF is the spreading factor used for the data part and m = SF×(s – 1)/16.

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25.214 CR **083**   Current Version: 3.1.1

GSM (AA.BB) or 3G (AA.BBB) specification number ↑   *↑ CR number as allocated by MCC support team*

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list expected approval meeting # here   for information ☐   non-strategic ☐ *use only)*
↑

Form: CR cover sheet, version 2 for 3GPP and SMG   The latest version of this form is available from: ftp://ftp.3gpp.org/Information/CR-Form-v2.doc

Proposed change affects: (U)SIM ☐   ME **X**   UTRAN / Radio **X**   Core Network ☐
(at least one should be marked with an X)

Source: SK Telecom   **Date:**   2000-03-03

Subject: Clean up of USTS related specifications

Work item:

Category:					**Release:**		
	F	Correction		**X**		Phase 2	☐
	A	Corresponds to a correction in an earlier release		☐		Release 96	☐
(only one category	B	Addition of feature		☐		Release 97	☐
shall be marked	C	Functional modification of feature		☐		Release 98	☐
with an X)	D	Editorial modification		☐		Release 99	**X**
						Release 00	☐

Reason for change: USTS is Release-00 item. Therefore USTS related specifications shall be removed in Release-99.

Clauses affected: 9

Other specs affected:	Other 3G core specifications	☐	→ List of CRs:	
	Other GSM core specifications	☐	→ List of CRs:	
	MS test specifications	☐	→ List of CRs:	
	BSS test specifications	☐	→ List of CRs:	
	O&M specifications	☐	→ List of CRs:	

Other comments:

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9 Uplink synchronous transmission

9.1 General

<Note: This scheme is not a base-line implementation capability.>

UplinkSynchronous Transmission Scheme(USTS) is an alternative technology applicable for low mobility terminals. USTS can reduce uplink intra-cell interference by means of making a cell receive orthogonalized signals from UEs. To orthogonalize receiving signals from UEs,

- the same scrambling code is allocated to all dedicated physical channels in a cell,

- different channelization codes are allocated to all dedicated physical channels across all UEs in a cell and the spreading factor and code number of channelization code are delivered from network to each UE

- the channelization codes for DPDCH and DPCCH in a UE are chosen from either upper half part or the lower half part of the OVSF code tree in a UE to reduce peak to average power ratio,

- additional scrambling codes can be allocated if all channelization codes are occupied, and

- the signal transmission time of each UE is adjusted.

The spreading and modulation scheme for USTS is same as section 4 of TS 25.213. In case of USTS, the long scrambling code described in section 4.3.2.2. of TS 25.213 is used. However, this long scrambling code is not UE specific, but cell specific. In order to generate the cell specific long scrambling code, the initial loading value of PN generator is determined by the network

The channelization codes are Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between USTS uplink channels of different rates and spreading factors.

The transmission time control is carried out by two steps. The first step is initial synchronization and the second is tracking.

1) Initial synchronization: Adjust transmission time through the initial timing control message over FACH

2) Tracking Process (Closed Loop Timing control): Adjust the transmission time through the Time Alignment Bit (TAB) over DPCCH.

9.2 Initial synchronisation

- When the cellreceives signal from UE over RACH, cell measures the difference in time between the received timing and the reference time in the unit of 1/8 chip duration..

- The message for initial synchronization, which contains the difference in time, is delivered to UE via FACH.

- UE adjust its transmission time according to the message.

9.3 Tracking process

- Cell periodically compares the reference time with received signal timing from UE.

- When the received timing is earlier than the reference time, Time Alignment Bit (TAB) = "0". When this is later than the reference time, TAB = "1".

- TAB replaces the TPC bit every timing control period of 20 msecand the last TPC bit of every two frames is replaced by TAB.

- At the UE, hard decision on the TAB shall be performed, and when it is judged as "0", the transmission time shall be delayed by 1/8 chip, whereas if it is judged as "1", the transmission time shall be advanced by 1/8 chip.