TSG-RAN Working Group 1 meeting #11 **TSGR1#11(00)0284**

San Diego, USA, February 28- March 3, 2000

Agenda Item:
Source: CWTS
To: TSG RAN WG1
Title: Frame Structure for low chip rate TDD option
Document for: Approval

Introduction

In 3GPP, there are two options for TDD mode. They are high chip rate option (3.84Mcps) and low chip rate option (1.28Mcps). The current specifications for TDD mode are mainly suitable for the high chip rate option. Due to the difference of the chip rate, a new frame structure for low chip rate TDD option will be proposed in this proposal. To enable the low chip rate with it's specific features and properties, other proposals will also be proposed later on by CWTS.

In WG1 meeting #10, the Tdoc R1-00-0092 for proposal of 'frame structure for low chip rate TDD option' is fully discussed. In this document, some background information, explanations and clarifications are added.

Conclusion

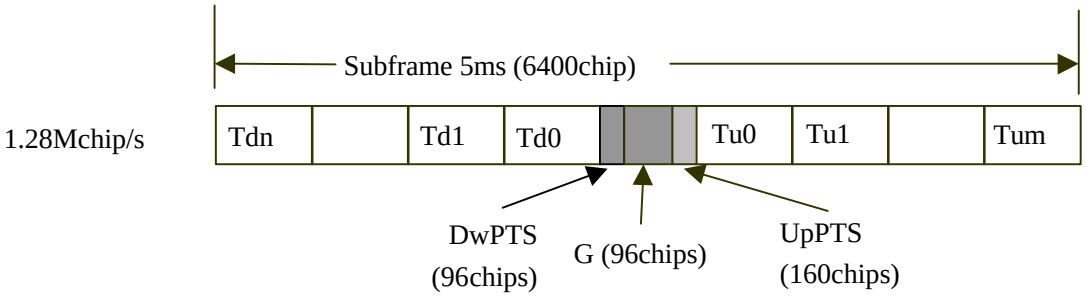
Based on the discussion and the common understanding, it is proposed to add the following text in section 5.2.1 of TR 25.928

---------- changes to TR25.928 begin ----------

5.2.1.1 Frame structure for low chiprate option

For both high chip rate option and low chip rate option, the frame length is 10ms. And for low chip rate option, this 10ms frame is divided into 2 sub-frames of 5ms to allow the fast update of power control and smart antenna beamforming. The frame structure for each sub-frame in the 10ms frame length is the same.

The frame structure for each sub-frame is shown in Figure 1.



Where n+m+2=7

Figure 1 Frame structure for low chip rate option

Tdn: the nth normal downlink time slot, 864 chips duration;

Tun: the nth normal uplink time slot, 864 chips duration;
DwPTS: downlink pilot time slot, 96 chips duration;
UpPTS: uplink pilot time slot, 160 chips duration;
G: main guard period for TDD operation, 96 chips duration;

In Figure 1, the total number of normal traffic time slot for uplink and downlink is 7, and the length for each normal time slot is 864 chips duration. Between the downlink time slot and uplink time slot, the special period is the switching point to separate the uplink and downlink. In each sub-frame of 5ms for low chip rate option, there is only one switching point. The proposed frame structure has taken some new technologies into consideration, either the smart antenna (beam forming) technology or the uplink synchronization will be well supported.

Using the above frame structure, the low chip rate TDD option can operate on both symmetric and asymmetric mode by shift the position of the switching point. It should be noted that in asymmetric operation mode, at least one normal uplink time slot and one downlink time slot will be allocated for traffic. The guard period G of 96 chips can support the cell radius of up to about 11km for uplink synchronization operation where the uplink transmission is advanced in macro-, micro- and pico- cell of small cells in cities or large cells in rural areas.

5.2.1.2 Burst structure for low chip rate option

In correspond to the frame structure described above, the burst structures for Tdn, Tun, DwPTS and UpPTS are proposed. The burst structure for normal time slot (Tdn, Tun) is described in Figure 2.

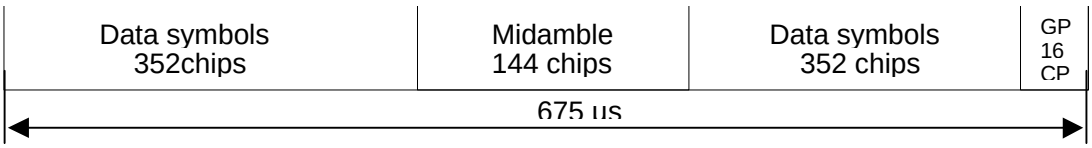


Figure 2 Burst structure for normal traffic time slot

In Figure 2, the data symbols in each side of the midamble is 352 chips (with spreading factor of 16). The TPC bits for power control, the TFCI bits and the additional uplink synchronization bits are included in Data symbols fields of the burst.

The GP field in Figure 2 for each time slot is used for protection between time slots to avoid the long delay multi-path interference. It should be noted that the GP of the last normal traffic burst (Td0) together with the guard period in DwPTS is 48 chips long which is different with other normal guard period of 16 chips between time slots. This ‘super long’ guard period can be used to avoid the interference between the last normal downlink time slot and the downlink synchronization pilot burst. Other wise, the interference to the last downlink time slot from the strong powered pilot will be serious to the traffic; vice versa, the interference to the downlink pilot burst from the last downlink time slot will decrease the performance on downlink synchronization and cell search.

The structure for DwPTS and UpPTS is described in Figure 3 and Figure 4.

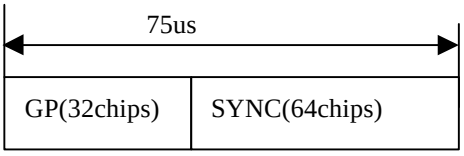


Figure 3 Structure for DwPTS

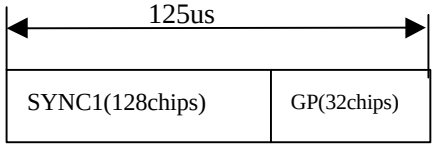


Figure 4 Structure for UpPTS

In DwPTS and UpPTS, the content of SYNC and SYNC1 field are used for downlink and uplink pilot. The GP fields are used to separate the downlink (uplink) pilot from the normal downlink (uplink) time slot.

It should be point out that the uplink synchronization burst (SYNC1) is not followed

by a RACH immediately. The transmission order is first UL synchronization burst from UE side for timing and power adjustment and then RACH burst is transmitted as a normal burst with payload. This two phase procedure which is different with the GSM of one phase procedure has better performance than the classical approach as used in GSM. In this case, the normal traffic burst and access burst can be active in the same time slot and the interference is reduced for each other if they are time-aligned.

The proposed frame structure and the related burst structure for low chip rate option can full fill the requirements for 3rd generation services and can provide the data services up to 2Mbps in a single 1.6MHz carrier. And the proposed frame structure can support all the environments of macro-, micro- and pico- cells. In vehicular environment, the speed can be more than 120km/h. Also in the proposed frame structure, some specific properties for low chip rate option such as smart antenna technology, uplink synchronisation, beamforming, etc can be well supported.

---------- changes to TR25.928 end ----------