**3****GPP TSG RAN WG1 #107-e R1-xxxxxx**

**e-Meeting, November 11th – 19th, 2021**

***Agenda item:*** ***8.14.1***

**Title: [DRAFT] TR section – Power evaluation**

**Source: Moderator (Qualcomm)**

**Document for: Discussion**

This document, if agreed, is going to be the power consumption evaluation section 9.3 of R17 XR TR.

*(Moderator’s note: In the text in this document, the source index and the corresponding component will be further updated as the following table. Note that in the final TR, the number could be revised to be consistent with other section if needed. )*

|  |  |
| --- | --- |
| Source 1 | Apple |
| Source 2 | AT&T |
| Source 3 | CATT |
| Source 4 | CEWiT |
| Source 5 | China Unicom |
| Source 6 | CMCC |
| Source 7 | Ericsson |
| Source 8 | FUTUREWEI |
| Source 9 | Huawei |
| Source 10 | Intel |
| Source 11 | InterDigital |
| Source 12 | ITRI |
| Source 13 | LG |
| Source 14 | MediaTek |
| Source 15 | Nokia, NSB |
| Source 16 | Qualcomm |
| Source 17 | OPPO |
| Source 18 | vivo |
| Source 19 | Xiaomi |
| Source 20 | ZTE |

**=============== Start of Text update for TR section – Capacity Results in 9.3 =====================**

## UE Power Consumption Evaluation

### Baseline Power Evaluation Results

This section includes the baseline power consumption results. PS schemes considered in this section includes AlwaysOn, R15/16/17 power saving schemes such as CDRX, cross slot scheduling and MIMO layer adaptation by BWP switching, PDCCH skipping.

* AlwaysOn: In this scheme, UE is always available for scheduling (i.e., no DRX off period). When UE is not receiving/transmitting DL/UL data, UE is assumed to keep monitoring PDCCH.
* R15/16 CDRX: Connected mode DRX scheme is assumed. (Note that no R16 wake up signal is considered.)
* Cross slot scheduling and MIMO layer adaptation by BWP switching: R16 dynamic BWP switching across different BWP with different configuration of minimum K0 and maximum MIMO layers.
* R17 PDCCH monitoring adaptation: UE skipping PDCCH monitoring based on a dynamically indicated PDCCH skipping indication and/or search space set group switching (SSSG) indication.
* Genie: UE is assumed to be in a sleep state (e.g., micro/light/deep sleep as defined in TR38.840) whenever there is neither DL data reception nor UL transmission.

#### FR1

##### DL+UL Joint Evaluation

###### DU

Table 1 Summary of FR1, DL+UL joint power evaluation results for DU

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS Gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| DU | VR | 30 | R15/16 CDRX | High | 3.94 | 2.24 ~ 7.0 | vivo, Ericsson, QC |
| Low | 3 | 2.44 ~ 3.56 | vivo |
| R17 PDCCH skipping | High | 19.98 |  | vivo |
| Low | 21.06 |  | vivo |
| 45 | R15/16 CDRX | High | 3.04 |  | QC |
| Low |  |  |  |
| CG | 30 | R15/16 CDRX | High | 4.52 | 2.85~7 | Ericsson, QC |
| Low |  |  |  |
| AR (UL 1 stream) | 30 | R15/16 CDRX | High | 2.1 | 1.62 ~ 2.58 | vivo |
| Low | 3.09 | 2.39 ~ 3.79 | vivo |
| R17 PDCCH skipping | High | 12.25 |  | vivo |
| Low | 18.26 |  | vivo |
| AR (UL 2 streams) | 30 | R15/16 CDRX | High | 2.57 | 0.79 ~ 4.29 | vivo, QC |
| Low | 1.27 | 0.91 ~ 1.63 | vivo |
| R17 PDCCH skipping | High | 11.25 |  | vivo |
| Low | 12.12 |  | vivo |
| Note 1: PSG was computed for the cases only with marginal loss in % of DL+UL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | | |

VR

**Observations**

* In FR1, DL+UL joint evaluation, DU, VR30 and high load, it is identified from Source vivo, QC that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 8/6/6) provides the mean power saving gain of 3.94% in the range of 2.24 ~ 7.00% with *marginal*[[1]](#footnote-1) loss in DL+UL UE satisfied rate.
* In FR1, DL+UL joint evaluation, DU, VR30 and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain is 19.98% with marginal loss in DL+UL UE satisfied rate.

Table 2 Source specific data: FR1, DL+UL, DU, VR 30Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 244 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 13 | 13 |  |  | 92.43% |  |
| vivo | 245 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 13 | 13 |  |  | 90.11% | 3.31% |
| vivo | 246 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 13 | 13 |  |  | 91.58% | 2.24% |
| vivo | 250 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 13 | 13 |  |  | 92.19% | 19.98% |
| Ericsson | 10 | R1-2112160 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 4 | 4 |  |  | 90.00% | 0.00% |
| Ericsson | 11 | R1-2112160 | Genie | 0 | 0 | 0 | 0 | H | 4 | 4 |  |  | 90.00% | 17.00% |
| Ericsson | 12 | R1-2112160 | R15/16CDRX | 4 | 3 | 0 | 0 | H | 4 | 4 |  |  | 80.00% | 7.00% |
| QC | 5 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 11 | 11 | 95.33% | 99.74% | 95.33% | 0.00% |
| QC | 6 | R1-2110402 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 11 | 11 | 94.37% | 99.74% | 94.37% | 3.22% |
| QC | 7 | R1-2110402 | R15/16CDRX | 8 | 6 | 4 | 0 | H | 11 | 11 | 91.00% | 50.82% | 47.53% | 7.30% |
| QC | 8 | R1-2110402 | Genie | 0 | 0 | 0 | 0 | H | 11 | 11 | 95.33% | 99.74% | 95.33% | 18.18% |
| QC | 54 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 11 | 11 | 97.14% | 100.00% | 97.14% | 0.00% |
| QC | 55 | R1-2110402 | R15/16CDRX | 16 | 12 | 12 | 0 | H | 11 | 11 | 89.35% | 79.83% | 69.87% | 1.78% |
| QC | 58 | R1-2110402 | Genie | 0 | 0 | 0 | 0 | H | 11 | 11 | 97.14% | 100.00% | 97.14% | 24.62% |
| \*data row index N means it is the N’th row in the results sheet each company has provided. | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL joint evaluation, DU, VR30, low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 3% in the range of 2.44 ~ 3.56% with marginal loss in DL+UL UE satisfied rate.
* In FR1, DL+UL joint evaluation, DU, VR30, low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 21.06% with marginal loss in DL+UL UE satisfied rate.

Table 3 Source specific data: FR1, DL+UL, DU, VR 30Mbps, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 236 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 7 | 13 |  |  | 100.00% |  |
| vivo | 237 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 7 | 13 |  |  | 100.00% | 3.56% |
| vivo | 238 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 7 | 13 |  |  | 100.00% | 2.44% |
| vivo | 242 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 7 | 13 |  |  | 100.00% | 21.06% |

**Observations**

* In FR1, DL+UL joint evaluation, DU, VR45, high load, it is identified from Source QC that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (8/6/6) provides the mean power saving gain of 3.04% with marginal loss in DL+UL UE satisfied rate.

Table 4 Source specific data: FR1, DL+UL, DU, VR 45Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| QC | 17 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 7 | 7 | 95.13% | 100.00% | 95.13% | 0.00% |
| QC | 18 | R1-2110402 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 7 | 7 | 94.29% | 100.00% | 94.29% | 3.04% |
| QC | 19 | R1-2110402 | R15/16CDRX | 8 | 6 | 4 | 0 | H | 7 | 7 | 89.66% | 47.62% | 43.54% | 7.08% |
| QC | 20 | R1-2110402 | Genie | 0 | 0 | 0 | 0 | H | 7 | 7 | 95.13% | 100.00% | 95.13% | 17.36% |

No results available for the case of FR1, DL+UL, DU, VR 45Mbps, low load.

CG

**Observations**

* In FR1, DL+UL joint evaluation, DU, CG30, high load, it is identified from Source Ericsson, QC that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (4/3/0, 8/4/6, 8/6/6) provides the mean power saving gain is 4.52% in the range of 2.85 ~ 7% with marginal loss in DL+UL UE satisfied rate.

Table 5 Source specific data: FR1, DL+UL, DU, CG 30Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| Ericsson | 1 | R1-2112160 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 4 | 4 |  |  | 90.00% | 0.00% |
| Ericsson | 2 | R1-2112160 | Genie | 0 | 0 | 0 | 0 | H | 4 | 4 |  |  | 90.00% | 17.00% |
| Ericsson | 3 | R1-2112160 | R15/16CDRX | 4 | 3 | 0 | 0 | H | 4 | 4 |  |  | 89.00% | 7.00% |
| QC | 29 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 15 | 15 | 91.75% | 99.87% | 91.75% | 0.00% |
| QC | 30 | R1-2110402 | R15/16CDRX | 8 | 6 | 4 | 0 | H | 15 | 15 | 91.68% | 51.05% | 47.05% | 6.66% |
| QC | 31 | R1-2110402 | R15/16CDRX | 8 | 4 | 6 | 0 | H | 15 | 15 | 91.62% | 99.87% | 91.62% | 3.73% |
| QC | 32 | R1-2110402 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 15 | 15 | 91.75% | 99.87% | 91.75% | 2.85% |
| QC | 33 | R1-2110402 | Genie | 0 | 0 | 0 | 0 | H | 15 | 15 | 91.75% | 99.87% | 91.75% | 17.74% |

No results available for FR1, DL+UL, DU, CG30, low load

AR

AR with UL 1 stream

**Observations**

* In FR1, DL+UL joint evaluation, DU, AR30 w/ UL 1 stream, high load, it is identified from Source vivo that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain is 2.1% in the range of 1.62 ~ 2.58% with marginal loss in DL+UL UE satisfied rate.
* In FR1, DL+UL joint evaluation, DU, AR30 w/ UL 1 stream, high load, it is identified from Source vivo that the R17 PDCCH skipping provides the mean power saving gain is 12.25% with marginal loss in DL+UL UE satisfied rate.

Table 6 Source specific data: FR1, DL+UL, DU, AR 30Mbps w/ UL 1 stream, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 276 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 9 | 9 |  |  | 92.59% | - |
| vivo | 277 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 9 | 9 |  |  | 91.89% | 2.58% |
| vivo | 278 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 9 | 9 |  |  | 92.06% | 1.62% |
| vivo | 282 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 9 | 9 |  |  | 92.24% | 12.25% |

**Observations**

* In FR1, DL+UL joint evaluation, DU, AR30 w/ UL 1 stream, low load, it is identified from Source vivo that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain is 3.09% in the range of 2.39 ~ 3.79% with marginal loss in DL+UL UE satisfied rate.
* In FR1, DL+UL joint evaluation, DU, AR30 w/ UL 1 stream, low load, it is identified from Source vivo that the R17 PDCCH skipping provides the mean power saving gain is 18.26% with marginal loss in DL+UL UE satisfied rate.

Table 7 Source specific data: FR1, DL+UL, DU, AR 30Mbps w/ UL 1 stream, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 268 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 5 | 9 |  |  | 96.51% | - |
| vivo | 269 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 5 | 9 |  |  | 96.19% | 3.79% |
| vivo | 270 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 5 | 9 |  |  | 96.51% | 2.39% |
| vivo | 274 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 5 | 9 |  |  | 96.19% | 18.26% |

AR with UL 2 streams

**Observations**

* In FR1, DL+UL joint evaluation, DU, AR30 w/ UL 2 streams, high load, it is identified from Source vivo, QC that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 8/4/6, 8/6/6) provides the mean power saving gain is 2.57% in the range of 0.79 ~ 4.29% with marginal loss in DL+UL UE satisfied rate.
* In FR1, DL+UL joint evaluation, DU, AR30 w/ UL 2 streams, high load, it is identified from Source vivo that the R17 PDCCH skipping provides the mean power saving gain is 11.25% with marginal loss in DL+UL UE satisfied rate.

Table 8 Source specific data: FR1, DL+UL, DU, AR 30Mbps w/ UL 2 stream, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 308 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 7 | 7 |  |  | 92.06% | - |
| vivo | 309 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 7 | 7 |  |  | 91.16% | 1.51% |
| vivo | 310 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 7 | 7 |  |  | 91.61% | 0.79% |
| vivo | 314 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 7 | 7 |  |  | 91.61% | 11.25% |
| QC | 44 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 3 | 3 | 99.80% | 94.05% | 93.85% | 0.00% |
| QC | 45 | R1-2110402 | R15/16CDRX | 8 | 6 | 4 | 0 | H | 3 | 3 | 99.80% | 44.44% | 44.44% | 7.80% |
| QC | 46 | R1-2110402 | R15/16CDRX | 8 | 4 | 6 | 0 | H | 3 | 3 | 99.80% | 94.44% | 94.25% | 4.29% |
| QC | 47 | R1-2110402 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 3 | 3 | 99.77% | 94.33% | 94.10% | 3.67% |

**Observations**

* In FR1, DL+UL joint evaluation, DU, AR30 w/ UL 2 streams, low load, it is identified from Source vivo that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain is 1.27% in the range of 0.91% ~ 1.63% with marginal loss in DL+UL UE satisfied rate.
* In FR1, DL+UL joint evaluation, DU, AR30 w/ UL 2 streams, low load, it is identified from Source vivo that the R17 PDCCH skipping provides the mean power saving gain is 12.12% with marginal loss in DL+UL UE satisfied rate.

Table 9 Source specific data: FR1, DL+UL, DU, AR 30Mbps w/ UL 2 stream, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 300 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 4 | 7 |  |  | 100.00% | - |
| vivo | 301 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 4 | 7 |  |  | 100.00% | 1.63% |
| vivo | 302 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 4 | 7 |  |  | 100.00% | 0.91% |
| vivo | 306 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 4 | 7 |  |  | 100.00% | 12.12% |

###### InH

Table 10 Summary of FR1, DL+UL joint power evaluation results for InH

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS Gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| InH | VR | 30 | R15/16 CDRX | High | 4.19 | 2.33 ~6 | Vivo, QC, ZTE |
| Low | 3.18 | 2.64 ~ 3.71 | vivo |
| R17 PDCCH skipping | High | 21.78 |  | vivo |
| Low | 22.35 |  | vivo |
| 45 | R15/16 CDRX | High | 5.78 | 2.91 ~ 7.22 | QC, ZTE |
| Low |  |  |  |
| CG | 30 | R15/16 CDRX | High | 3.88 | 2.85 ~ 4.5 | QC, ZTE |
| Low |  |  |  |
| AR (UL 1 stream) | 30 | R15/16 CDRX | High | 2.16 | 1.69 ~ 2.62 | vivo |
| Low | 3.4 | 2.59 ~ 4.2 | vivo |
| R17 PDCCH skipping | High | 13.28 |  | vivo |
| Low | 21.17 |  | vivo |
| AR (UL 2 streams) | 30 | R15/16 CDRX | High | 3.72 | 0.83 ~ 8.04 | vivo, QC |
| Low | 1.42 | 1.02 ~ 1.81 | vivo |
| R17 PDCCH skipping | High | 12.51 |  | vivo |
| Low | 14.47 |  | vivo |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL+UL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | | |

VR

**Observations**

* In FR1, DL+UL joint evaluation, InH, VR30, high load, it is identified from Source vivo, ZTE, QC that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 10/8/4, 8/6/6) provides the mean power saving gain is 4.19% in the range of 2.33 ~ 6% with marginal loss in DL+UL UE satisfied rate.
* In FR1, DL+UL joint evaluation, InH, VR30, high load, it is identified from Source vivo that the R17 PDCCH skipping provides the mean power saving gain is 21.78% with marginal loss in DL+UL UE satisfied rate.

Table 11 Source specific data: FR1, DL+UL, InH, VR 30Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 228 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 10 | 10 |  |  | 92.50% | - |
| vivo | 229 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 10 | 10 |  |  | 91.25% | 3.45% |
| vivo | 230 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 10 | 10 |  |  | 91.81% | 2.33% |
| vivo | 234 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 10 | 10 |  |  | 91.81% | 21.78% |
| ZTE, Sanechips | 1 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | Note 1, 2 | H | 11 | 11 | 93.18% | 100.00% | 93.18% | 0.00% |
| ZTE, Sanechips | 2 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | Note 1, 3 | H | 11 | 11 | 93.18% | 100.00% | 93.18% | 0.00% |
| ZTE, Sanechips | 5 | R1-2111351 | R15 CDRX | 10 | 8 | 4 | Note 1, 2 | H | 11 | 11 | 90.15% | 100.00% | 90.15% | 6.00% |
| ZTE, Sanechips | 6 | R1-2111351 | R15 CDRX | 10 | 8 | 4 | Note 1, 3 | H | 11 | 11 | 90.15% | 100.00% | 90.15% | 6.00% |
| QC | 9 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 9 | 9 | 92.73% | 100.00% | 92.73% | 0.00% |
| QC | 10 | R1-2110402 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 9 | 9 | 92.59% | 100.00% | 92.59% | 3.18% |
| QC | 11 | R1-2110402 | R15/16CDRX | 8 | 6 | 4 | 0 | H | 9 | 9 | 89.29% | 49.74% | 43.92% | 7.18% |
| QC | 12 | R1-2110402 | Genie | 0 | 0 | 0 | 0 | H | 9 | 9 | 92.73% | 100.00% | 92.73% | 20.38% |
| Note 1. DL and UL were simulated separately and collected traces are combined as a single timeline for DL+UL joint power evaluation.  Note 2. Option 2(Linear interpolation in linear domain) for UL power model  Note 3. Option 1(two-step Quantization) for UL power model | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL joint evaluation, InH, VR30, low load, it is identified from Source vivo that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain is 3.18% in the range of 2.64 ~ 3.71% with marginal loss in DL+UL UE satisfied rate.
* In FR1, DL+UL joint evaluation, InH, VR30, low load, it is identified from Source vivo that the R17 PDCCH skipping provides the mean power saving gain is 22.35% with marginal loss in DL+UL UE satisfied rate.

Table 12 Source specific data: FR1, DL+UL, InH, VR 30Mbps, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 220 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 5 | 10 |  |  | 100.00% | - |
| vivo | 221 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 5 | 10 |  |  | 100.00% | 3.71% |
| vivo | 222 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 5 | 10 |  |  | 100.00% | 2.64% |
| vivo | 226 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 5 | 10 |  |  | 100.00% | 22.35% |
| ZTE, Sanechips | 3 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | Note 1, 2 | L | 10 | 11 | 93.00% | 100.00% | 93.00% | 0.00% |
| ZTE, Sanechips | 4 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | Note 1, 3 | L | 10 | 11 | 93.00% | 100.00% | 93.00% | 0.00% |
| Note 1. DL and UL were simulated separately and collected traces are combined as a single timeline for DL+UL joint power evaluation.  Note 2. Option 2(Linear interpolation in linear domain) for UL power model  Note 3. Option 1(two-step Quantization) for UL power model | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL joint evaluation, InH, VR45, high load, it is identified from Source ZTE, QC that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 8/6/6) provides the mean power saving gain is 5.78% in the range of 2.91% ~ 7.22% with marginal loss in DL+UL UE satisfied rate.

Table 13 Source specific data: FR1, DL+UL, InH, VR 45Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| ZTE, Sanechips | 11 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | Note 1, 2 | H | 7 | 7 | 91.00% | 100.00% | 91.00% | 0.00% |
| ZTE, Sanechips | 12 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | Note 1,3 | H | 7 | 7 | 91.00% | 100.00% | 91.00% | 0.00% |
| ZTE, Sanechips | 13 | R1-2111351 | R15 CDRX | 10 | 8 | 4 | Note 1, 2 | H | 7 | 7 | 87.00% | 100.00% | 87.00% | 7.22% |
| ZTE, Sanechips | 14 | R1-2111351 | R15 CDRX | 10 | 8 | 4 | Note 1,3 | H | 7 | 7 | 87.00% | 100.00% | 87.00% | 7.22% |
| QC | 21 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 6 | 6 | 90.59% | 100.00% | 90.59% | 0.00% |
| QC | 22 | R1-2110402 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 6 | 6 | 89.82% | 100.00% | 89.82% | 2.91% |
| QC | 23 | R1-2110402 | R15/16CDRX | 8 | 6 | 4 | 0 | H | 6 | 6 | 82.56% | 49.69% | 40.59% | 6.69% |
| QC | 24 | R1-2110402 | Genie | 0 | 0 | 0 | 0 | H | 6 | 6 | 90.59% | 100.00% | 90.59% | 19.34% |
| QC | 24 | R1-2110216 | Genie | 0 | 0 | 0 |  | H | 6 | 6 | 90.59% | 100.00% | 90.59% | 19.34% |
| Note 1. DL and UL were simulated separately and collected traces are combined as a single timeline for DL+UL joint power evaluation. Note 2. Option 2(Linear interpolation in linear domain) for UL power model  Note 3. Option 1(two-step Quantization) for UL power model | | | | | | | | | | | | | | |

No results available for FR1, DL+UL, InH, VR45, low load case.

CG

**Observations**

* In FR1, DL+UL joint evaluation, InH, CG30, high load, it is identified from Source ZTE. QC that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 8/4/6, 8/6/6) provides the mean power saving gain is 3.88% in the range of 2.85 ~ 4.5% with marginal loss in DL+UL UE satisfied rate.

Table 14 Source specific data: FR1, DL+UL, InH, CG 30Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| ZTE, Sanechips | 19 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | Note 1, 2 | H | 12 | 12 | 96.53% | 100.00% | 96.53% | 0.00% |
| ZTE, Sanechips | 20 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | Note 1, 3 | H | 12 | 12 | 96.53% | 100.00% | 96.53% | 0.00% |
| ZTE, Sanechips | 21 | R1-2111351 | R15 CDRX | 10 | 8 | 4 | Note 1, 2 | H | 12 | 12 | 88.88% | 100.00% | 88.88% | 4.50% |
| ZTE, Sanechips | 22 | R1-2111351 | R15 CDRX | 10 | 8 | 4 | Note 1, 3 | H | 12 | 12 | 88.88% | 100.00% | 88.88% | 4.50% |
| QC | 34 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 11 | 11 | 91.36% | 100.00% | 91.36% | 0.00% |
| QC | 35 | R1-2110402 | R15/16CDRX | 8 | 6 | 4 | 0 | H | 11 | 11 | 91.67% | 49.09% | 45.15% | 6.69% |
| QC | 36 | R1-2110402 | R15/16CDRX | 8 | 4 | 6 | 0 | H | 11 | 11 | 91.97% | 100.00% | 91.97% | 3.68% |
| QC | 37 | R1-2110402 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 11 | 11 | 91.36% | 100.00% | 91.36% | 2.85% |
| QC | 38 | R1-2110402 | Genie | 0 | 0 | 0 | 0 | H | 11 | 11 | 91.36% | 100.00% | 91.36% | 19.70% |
| Note 1. DL and UL were simulated separately and collected traces are combined as a single timeline for DL+UL joint power evaluation.  Note 2. Option 2(Linear interpolation in linear domain) for UL power model  Note 3. Option 1(two-step Quantization) for UL power model | | | | | | | | | | | | | | |

No results available for FR1, DL+UL, InH, CG30, low load case.

AR

AR with UL 1 stream

**Observations**

* In FR1, DL+UL joint evaluation, InH, AR30 w/ UL 1 stream, high load, it is identified from Source vivo that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain is 2.16% in the range of 1.69 ~ 2.62% with marginal loss in DL+UL UE satisfied rate.
* In FR1, DL+UL joint evaluation, InH, AR30 w/ UL 1 stream, high load, it is identified from Source vivo that the R17 PDCCH skipping provides the mean power saving gain is 13.28% with marginal loss in DL+UL UE satisfied rate.

Table 15 Source specific data: FR1, DL+UL, InH, AR 30Mbps, UL 1 stream, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 260 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 10 | 10 |  |  | 92.50% | - |
| vivo | 261 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 10 | 10 |  |  | 91.67% | 2.62% |
| vivo | 262 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 10 | 10 |  |  | 91.94% | 1.69% |
| vivo | 266 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 10 | 10 |  |  | 91.94% | 13.28% |

**Observations**

* In FR1, DL+UL joint evaluation, InH, AR30 w/ UL 1 stream, low load, it is identified from Source vivo that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain is 3.4% in the range of 2.59 ~ 4.2% with marginal loss in DL+UL UE satisfied rate.
* In FR1, DL+UL joint evaluation, InH, AR30 w/ UL 1 stream, low load, it is identified from Source vivo that the R17 PDCCH skipping provides the mean power saving gain is 21.17% with marginal loss in DL+UL UE satisfied rate.

Table 16 Source specific data: FR1, DL+UL, InH, AR 30Mps, UL 1 stream, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 252 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 5 | 10 |  |  | 100.00% | - |
| vivo | 253 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 5 | 10 |  |  | 100.00% | 4.20% |
| vivo | 254 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 5 | 10 |  |  | 100.00% | 2.59% |
| vivo | 258 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 5 | 10 |  |  | 100.00% | 21.17% |

AR with UL 2 streams

**Observations**

* In FR1, DL+UL joint evaluation, InH, AR30 w/ UL 2 streams, high load, it is identified from Source vivo, QC that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 8/4/6, 8/6/6) provides the mean power saving gain is 2.64% in the range of 0.83 ~ 4.41% with marginal loss in DL+UL UE satisfied rate.

**Observations**

* In FR1, DL+UL joint evaluation, InH, AR30 w/ UL 2 streams, high load, it is identified from Source vivo that the R17 PDCCH skipping provides the mean power saving gain is 12.51% with marginal loss in DL+UL UE satisfied rate.

Table 17 Source specific data: FR1, DL+UL, InH, AR 30Mbps, UL 2 streams, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 292 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 10 | 10 |  |  | 92.22% | - |
| vivo | 293 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 10 | 10 |  |  | 90.83% | 1.59% |
| vivo | 294 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 10 | 10 |  |  | 91.67% | 0.83% |
| vivo | 298 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 10 | 10 |  |  | 91.67% | 12.51% |
| QC | 49 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 3 | 3 | 99.44% | 94.44% | 93.89% | 0.00% |
| QC | 50 | R1-2110402 | R15/16CDRX | 8 | 6 | 4 | 0 | H | 3 | 3 | 99.44% | 44.44% | 44.44% | 8.04% |
| QC | 51 | R1-2110402 | R15/16CDRX | 8 | 4 | 6 | 0 | H | 3 | 3 | 99.72% | 94.17% | 93.89% | 4.41% |
| QC | 52 | R1-2110402 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 3 | 3 | 99.44% | 94.72% | 94.44% | 3.72% |
| QC | 53 | R1-2110402 | Genie | 0 | 0 | 0 | 0 | H | 3 | 3 | 99.44% | 94.44% | 93.89% | 20.44% |

**Observations**

* In FR1, DL+UL joint evaluation, InH, AR30 w/ UL 2 streams, low load, it is identified from Source vivo that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain is 1.42% in the range of 1.02 ~ 1.81% with marginal loss in DL+UL UE satisfied rate.
* In FR1, DL+UL joint evaluation, InH, AR30 w/ UL 2 streams, low load, it is identified from Source vivo that the R17 PDCCH skipping provides the mean power saving gain is 14.47% with marginal loss in DL+UL UE satisfied rate.

Table 18 Source specific data: FR1, DL+UL, InH, AR 30Mbps, UL 2 streams, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 284 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 5 | 10 |  |  | 100.00% | - |
| vivo | 285 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 5 | 10 |  |  | 100.00% | 1.81% |
| vivo | 286 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 5 | 10 |  |  | 100.00% | 1.02% |
| vivo | 290 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 5 | 10 |  |  | 100.00% | 14.47% |

###### UMa

Table 19 Summary of FR1, DL+UL joint power evaluation results for UMa

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS Gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| UMa | VR | 30 | R15/16 CDRX | High | 3.89 |  | QC |
| 45 | R15/16 CDRX | High | 3.52 |  | QC |
| CG | 30 | R15/16 CDRX | High | 4.1 |  | QC |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL+UL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | | |

VR

**Observations**

* In FR1, DL+UL joint evaluation, UMa, VR30, high load, it is identified from Source QC that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (8/6/6) provides the mean power saving gain is 3.89% with marginal loss in DL+UL UE satisfied rate.

Table 20 Source specific data: FR1, DL+UL, UMa, VR 30Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| QC | 13 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 4 | 4 | 93.37% | 94.22% | 93.20% | 0.00% |
| QC | 14 | R1-2110402 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 4 | 4 | 93.20% | 93.71% | 93.71% | 3.89% |
| QC | 15 | R1-2110402 | R15/16CDRX | 8 | 6 | 4 | 0 | H | 4 | 4 | 92.86% | 50.00% | 49.66% | 8.19% |
| QC | 16 | R1-2110402 | Genie | 0 | 0 | 0 | 0 | H | 4 | 4 | 93.37% | 94.22% | 93.20% | 8.79% |

No results available for FR1, DL+UL, UMa, VR30, low load

**Observations**

* In FR1, DL+UL joint evaluation, UMa, VR45, high load, it is identified from Source QC that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (8/6/6) provides the mean power saving gain is 3.52% with marginal loss in DL+UL UE satisfied rate.

Table 21 Source specific data: FR1, DL+UL, UMa, VR 45Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| QC | 25 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 3 | 3 | 91.59% | 95.08% | 91.59% | 0.00% |
| QC | 26 | R1-2110402 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 3 | 3 | 91.59% | 94.92% | 91.59% | 3.52% |
| QC | 27 | R1-2110402 | R15/16CDRX | 8 | 6 | 4 | 0 | H | 3 | 3 | 90.00% | 48.73% | 45.87% | 7.71% |
| QC | 28 | R1-2110402 | Genie | 0 | 0 | 0 | 0 | H | 3 | 3 | 91.59% | 95.08% | 91.59% | 8.70% |

No results available for FR1, DL+UL, UMa, VR45, low load

CG

**Observations**

* In FR1, DL+UL joint evaluation, UMa, CG30, high load, it is identified from Source QC that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (8/4/6, 8/6/6) provides the mean power saving gain is 4.10% in the range of 3.51% ~ 4.69% with marginal loss in DL+UL UE satisfied rate.

Table 22 Source specific data: FR1, DL+UL, UMa, CG 30Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| QC | 39 | R1-2110402 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 6 | 6 | 91.95% | 92.86% | 91.16% | 0.00% |
| QC | 40 | R1-2110402 | R15/16CDRX | 8 | 6 | 4 | 0 | H | 6 | 6 | 92.06% | 45.58% | 44.79% | 7.72% |
| QC | 41 | R1-2110402 | R15/16CDRX | 8 | 4 | 6 | 0 | H | 6 | 6 | 92.29% | 92.63% | 91.38% | 4.69% |
| QC | 42 | R1-2110402 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 6 | 6 | 92.40% | 92.29% | 91.16% | 3.51% |
| QC | 43 | R1-2110402 | Genie | 0 | 0 | 0 | 0 | H | 6 | 6 | 91.95% | 92.86% | 91.16% | 9.04% |

No results available for FR1, DL+UL, UMa, CG30, low load

AR

No results are available.

##### DL-only Evaluation

###### DU

Table 23 Summary of FR1, DL-only power evaluation results for DU

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS Gain (%), Note 1 | | source |
| Mean (%) | Range (%) |  |
| DU | VR/AR | 30 | R15/16 CDRX | High | 8.45 | 3.03 ~ 21.0 | HW, vivo, Nokia, E///, intel |
| Low | 4.64 | 3.57 ~ 5.76 | HW, vivo |
| R17 PDCCH skipping | High | 18.86 |  | vivo |
| Low | 22.65 |  | vivo |
| 45 | R15/16 CDRX | High | 4.40 | 3.1~4.61 | Vivo, MTK, Nokia |
| Low | 4.55 | 3.53~5.56 | Vivo, intel |
| R17 PDCCH skipping | High | 15.69 | 12.66~18.73 | vivo |
| Low | 21.95 |  | vivo |
| cross-slot scheduling + MIMO layer adaptation by BWP switching | High | 9.33 |  | MTK |
| cross-slot scheduling + MIMO layer adaptation + PDCCH skipping by BWP switching | High | 9.78 |  | MTK |
| CG | 30 | R15/16 CDRX | High | 8.4 | 3.3 ~ 20 | HW, MTK, Nokia, E///, intel |
| Low | 10.3 | 3.57 ~ 15.7 | HW, intel |
| R17 PDCCH skipping | High | 12.86 |  | MTK |
| Low |  |  |  |
| cross-slot scheduling + MIMO layer adaptation by BWP switching | High | 8.13 |  | MTK |
| Low |  |  |  |
| cross-slot scheduling + MIMO layer adaptation + PDCCH skipping by BWP switching | High | 8.53 |  | MTK |
| Low |  |  |  |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | |  |

VR/AR

**Observations**

* In FR1, DL only evaluation, DU, VR/AR30 and high load, it is identified from Source HW, vivo, Intel, Nokia, Ericsson, QC that the R15/16CDRX with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 8/6/6, 8/4/6, 4/2/2, 10/8/2, 10/8/3) scheme provides the mean power saving gain of 8.45% in the range of 3.03 ~ 21.00% with *marginal[[2]](#footnote-2)* loss in DL UE satisfied rate.
* The choice of a particular R15/16 CDRX configuration (cycle, on duration, and inactivity timer) greatly affects the PS gain.
* In FR1, DL only evaluation, DU, VR/AR30 and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 18.86% with *marginal* loss in DL UE satisfied rate.

Table 24 Source specific data: FR1, DL-only, DU, AR/VR 30Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| Huawei | 1 | R1-2110811 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 5 | 5 | 92.00% | 0.00% |
| Huawei | 2 | R1-2110811 | R15/16CDRX | 10 | 5 | 4 | 0 | H | 5 | 5 | 61.05% | 14.68% |
| Huawei | 3 | R1-2110811 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 5 | 5 | 88.29% | 5.53% |
| Huawei | 4 | R1-2110811 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 5 | 5 | 0.00% | 10.70% |
| Huawei | 5 | R1-2110811 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 5 | 5 | 90.67% | 3.46% |
| vivo | 41 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 13 | 13 | 92.43% | - |
| vivo | 42 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 13 | 13 | 90.11% | 4.70% |
| vivo | 43 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 13 | 13 | 91.58% | 3.03% |
| vivo | 47 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 13 | 13 | 92.43% | 18.86% |
| Intel | 1 | R1-2111521 | Always On | 0 | 0 | 0 | 0 | H | 4 | 5 | 96.00% | 0.00% |
| Intel | 2 | R1-2111521 | Genie | 0 | 0 | 0 | 0 | H | 4 | 5 | 96.00% | 58.30% |
| Intel | 3 | R1-2111521 | CDRX | 8 | 6 | 6 | 0 | H | 4 | 5 | 94.00% | 10.80% |
| Intel | 4 | R1-2111521 | CDRX | 8 | 4 | 6 | 0 | H | 4 | 5 | 82.75% | 15.70% |
| Xiaomi | 3 | R1-2112573 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 7 | 7 | 92.44% | - |
| Xiaomi | 4 | R1-2112573 | Genie | 0 | 0 | 0 | 0 | H | 7 | 7 | 92.44% | 41.71% |
| Nokia | 36 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 6 | 6 | 83.00% | 21.00% |
| Nokia | 37 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 6 | 6 | 61.00% | 18.00% |
| Nokia | 38 | R1-2111828 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 6 | 6 | 0.00% | 15.80% |
| Nokia | 39 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 6 | 6 | 93.00% | 9.20% |
| Nokia | 40 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 6 | 6 | 52.00% | 17.00% |
| Interdigital | 21 | R1-2111830 | AlwaysOn - baseline | - | - | - | 0 | H | 3 | 3 | 100.00% | 0.00% |
| Interdigital | 22 | R1-2111830 | R15/16CDRX | 16 | 12 | 4 | 0 | H | 3 | 3 | 75.00% | 6.925%\* |
| Interdigital | 23 | R1-2111830 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 3 | 3 | 76.00% | 16.758%\* |
| Interdigital | 24 | R1-2111830 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 3 | 3 | 20.00% | 10.945%\* |
| Interdigital | 25 | R1-2111830 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 3 | 3 | 88.33% | 7.221%\* |
| Ericsson | 14 | R1-2112160 | AlwaysOn – baseline | 0 | 0 | 0 | 0 | H | 4 | 4 | 90.00% | 0.00% |
| Ericsson | 15 | R1-2112160 | Genie | 0 | 0 | 0 | 0 | H | 4 | 4 | 90.00% | 41.00% |
| Ericsson | 16 | R1-2112160 | R15/16CDRX | 10 | 8 | 3 | 0 | H | 4 | 4 | 84.00% | 4.00% |
| Ericsson | 17 | R1-2112160 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 4 | 4 | 29.00% | 8.00% |
| QC | 60 | R1-2110402 | ALWAYS ON | 0 | 0 | 0 | 0 | H | 11 | 11 | 97.75% | 0.00% |

**Observations**

* In FR1, DL only evaluation, DU, VR/AR30 and low load, it is identified from Source HW, vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 10/8/4, 16/14/4) provides the mean power saving gain of 4.64% in the range of 3.57 ~ 5.76% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, DU, VR/AR30 and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 22.65% with *marginal* loss in DL UE satisfied rate.

Table 25 Source specific data: FR1, DL-only, DU, AR/VR 30Mbps, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| Huawei | 16 | R1-2110811 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 3 | 5 | 98.41% | 0.00% |
| Huawei | 17 | R1-2110811 | R15/16CDRX | 10 | 5 | 4 | 0 | L | 3 | 5 | 78.25% | 15.24% |
| Huawei | 18 | R1-2110811 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 3 | 5 | 97.78% | 5.76% |
| Huawei | 19 | R1-2110811 | R15/16CDRX | 16 | 8 | 8 | 0 | L | 3 | 5 | 0.00% | 11.01% |
| Huawei | 20 | R1-2110811 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 3 | 5 | 97.94% | 3.57% |
| vivo | 33 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 7 | 13 | 100.00% | - |
| vivo | 34 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 7 | 13 | 100.00% | 5.57% |
| vivo | 35 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 7 | 13 | 100.00% | 3.65% |
| vivo | 39 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 7 | 13 | 100.00% | 22.65% |
| Xiaomi | 1 | R1-2112573 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 4 | 7 | 99.50% | - |
| Xiaomi | 2 | R1-2112573 | Genie | 0 | 0 | 0 | 0 | L | 4 | 7 | 99.50% | 44.24% |

**Observations**

* In FR1, DL only evaluation, DU, VR/AR45 and high load, it is identified from Source vivo, Nokia, ID that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 10/8/2) provides the mean power saving gain of 4.40% in the range of 3.10 ~ 6.61% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, DU, VR/AR45 and high load, it is identified from Source vivo, MTK that the R17 PDCCH skipping scheme provides the mean power saving gain of 15.69% in the range of 12.66~18.73% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, DU, VR/AR45 and high load, it is identified from Source MTK that the cross-slot scheduling + MIMO layer adaptation by BWP switching provides the mean power saving gain of 9.33% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, DU, VR/AR45 and high load, it is identified from Source MTK that the cross-slot scheduling + MIMO layer adaptation + PDCCH skipping by BWP switching provides the mean power saving gain of 9.78% with *marginal* loss in DL UE satisfied rate.

Table 26 Source specific data: FR1, DL-only, DU, AR/VR 45Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 57 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 6 | 6 | 95.63% | - |
| vivo | 58 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 6 | 6 | 93.12% | 4.69% |
| vivo | 59 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 6 | 6 | 94.18% | 3.10% |
| vivo | 63 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 6 | 6 | 94.44% | 18.73% |
| ZTE, Sanechips | 40 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | 0 | H | 7 | 7 | 96.60% | 0.00% |
| Xiaomi | 11 | R1-2112573 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 5 | 5 | 94.71% | - |
| Xiaomi | 12 | R1-2112573 | Genie | 0 | 0 | 0 | 0 | H | 5 | 5 | 94.71% | 39.55% |
| Nokia | 41 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 4 | 4 | 69.00% | 14.50% |
| Nokia | 42 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 4 | 4 | 40.00% | 10.80% |
| Nokia | 43 | R1-2111828 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 4 | 4 | 0.00% | 7.90% |
| Nokia | 44 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 4 | 4 | 88.00% | 3.20% |
| Nokia | 45 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 4 | 4 | 24.00% | 9.50% |
| Interdigital | 26 | R1-2111830 | AlwaysOn - baseline | - | - | - | 0 | H | 2 | 2 | 95.00% | 0.00% |
| Interdigital | 27 | R1-2111830 | R15/16CDRX | 16 | 12 | 4 | 0 | H | 2 | 2 | 63.00% | 6.30%\* |
| Interdigital | 28 | R1-2111830 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 2 | 2 | 63.00% | 15.54%\* |
| Interdigital | 29 | R1-2111830 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 2 | 2 | 13.00% | 9.67%\* |
| Interdigital | 30 | R1-2111830 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 2 | 2 | 80.00% | 6.61%\* |
| MTK | 6 | R1-2109555 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 7 | 7 | 91.75% | 0.00% |
| MTK | 7 | R1-2109555 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 7 | 7 | 68.01% | 5.73% |
| MTK | 8 | R1-2109555 | Custom : cross-slot  + MIMO layer adaptation  by BWP switching | 0 | 0 | 0 | 0 | H | 7 | 7 | 88.93% | 9.33% |
| MTK | 9 | R1-2109555 | Custom : cross-slot  + MIMO layer adaptation  + PDCCH skipping  by BWP switching | 0 | 0 | 0 | 0 | H | 7 | 7 | 86.12% | 9.78% |
| MTK | 10 | R1-2109555 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 7 | 7 | 90.00% | 12.66% |

**Observations**

* In FR1, DL only evaluation, DU, VR/AR45 and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 4.55% in the range of 3.53 ~ 5.56% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL-only evaluation, DU, VR/AR45 and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 21.95% with *marginal* loss in DL UE satisfied rate.

Table 27 Source specific data: FR1, DL-only, DU, AR/VR 45Mbps, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 49 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 3 | 6 | 100.00% | - |
| vivo | 50 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 3 | 6 | 100.00% | 5.56% |
| vivo | 51 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 3 | 6 | 100.00% | 3.53% |
| vivo | 55 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 3 | 6 | 100.00% | 21.95% |
| Xiaomi | 9 | R1-2112573 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 3 | 5 | 99.7% | - |
| Xiaomi | 10 | R1-2112573 | Genie | 0 | 0 | 0 | 0 | L | 3 | 5 | 99.7% | 43.73% |

CG

**Observations**

* In FR1, DL only evaluation, DU, CG30 and high load, it is identified from Source HW, Nokia, ID, Ericsson, MTK that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 4/2/2, 8/4/4, 10/8/2, 16/12/4, 10/8/2, 10/8/3, 10/5/5) provides the mean power saving gain of 8.4% in the range of 3.3 ~ 20.0% with *marginal* loss in DL UE satisfied rate.
* The choice of a particular R15/16 CDRX configuration (cycle, on duration, and inactivity timer) greatly affects the PS gain.
* In FR1, DL only evaluation, DU, CG30 and high load, it is identified from Source MTK that the R17 PDCCH skipping scheme provides the mean power saving gain of 12.86% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, DU, CG30 and high load, it is identified from Source MTK that the cross-slot scheduling + MIMO layer adaptation by BWP switching provides the mean power saving gain of 8.13% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, DU, CG30 and high load, it is identified from Source MTK that the cross-slot scheduling + MIMO layer adaptation + PDCCH skipping by BWP switching provides the mean power saving gain of 8.53% with *marginal* loss in DL UE satisfied rate.

Table 28 Source specific data: FR1, DL-only, DU, CG 30Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| Huawei | 31 | R1-2110811 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 7 | 7 | 90.88% | 0.00% |
| Huawei | 32 | R1-2110811 | R15/16CDRX | 10 | 5 | 4 | 0 | H | 7 | 7 | 77.96% | 13.83% |
| Huawei | 33 | R1-2110811 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 7 | 7 | 90.00% | 5.26% |
| Huawei | 34 | R1-2110811 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 7 | 7 | 74.42% | 9.71% |
| Huawei | 35 | R1-2110811 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 7 | 7 | 89.96% | 3.30% |
| Xiaomi | 7 | R1-2112573 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 8 | 8 | 92.88% | - |
| Xiaomi | 8 | R1-2112573 | Genie | 0 | 0 | 0 | 0 | H | 8 | 8 | 92.88% | 39.83% |
| Nokia | 31 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 8 | 8 | 88.00% | 20.00% |
| Nokia | 32 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 8 | 8 | 84.00% | 16.70% |
| Nokia | 33 | R1-2111828 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 8 | 8 | 70.00% | 13.60% |
| Nokia | 34 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 8 | 8 | 93.00% | 8.80% |
| Nokia | 35 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 8 | 8 | 76.00% | 15.40% |
| Interdigital | 16 | R1-2111830 | AlwaysOn - baseline | - | - | - | 0 | H | 5 | 5 | 96.00% | 0.00% |
| Interdigital | 17 | R1-2111830 | R15/16CDRX | 16 | 12 | 4 | 0 | H | 5 | 5 | 84.50% | 6.31%\* |
| Interdigital | 18 | R1-2111830 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 5 | 5 | 76.25% | 14.73%\* |
| Interdigital | 19 | R1-2111830 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 5 | 5 | 64.25% | 9.53%\* |
| Interdigital | 20 | R1-2111830 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 5 | 5 | 86.25% | 5.98%\* |
| Ericsson | 5 | R1-2112160 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 4 | 4 | 90.00% | 0.00% |
| Ericsson | 6 | R1-2112160 | Genie | 0 | 0 | 0 | 0 | H | 4 | 4 | 90.00% | 41.00% |
| Ericsson | 7 | R1-2112160 | R15/16CDRX | 10 | 8 | 3 | 0 | H | 4 | 4 | 89.00% | 4.00% |
| Ericsson | 8 | R1-2112160 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 4 | 4 | 83.00% | 8.00% |
| MTK | 1 | R1-2109555 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 13 | 13 | 91.48% | 0.00% |
| MTK | 2 | R1-2109555 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 13 | 13 | 80.00% | 5.63% |
| MTK | 3 | R1-2109555 | Custom : cross-slot  + MIMO layer adaptation  by BWP switching | 0 | 0 | 0 | 0 | H | 13 | 13 | 90.74% | 8.13% |
| MTK | 4 | R1-2109555 | Custom : cross-slot  + MIMO layer adaptation  +PDCCH skipping by BWP switching | 0 | 0 | 0 | 0 | H | 13 | 13 | 90.04% | 8.53% |
| MTK | 5 | R1-2109555 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 13 | 13 | 90.29% | 12.86% |

**Observations**

* In FR1, DL only evaluation, DU, CG30 and low load, it is identified from Source HW, Intel that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/5/4, 10/8/4, 16/8/8, 16/14/4, 8/6/6/, 8/4/6) provides the mean power saving gain of 10.3% in the range of 3.57 ~ 15.7% with *marginal* loss in DL UE satisfied rate.

Table 29 Source specific data: FR1, DL-only, DU, CG 30Mbps, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| Huawei | 46 | R1-2110811 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 3 | 7 | 99.68% | 0.00% |
| Huawei | 47 | R1-2110811 | R15/16CDRX | 10 | 5 | 4 | 0 | L | 3 | 7 | 99.21% | 15.20% |
| Huawei | 48 | R1-2110811 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 3 | 7 | 99.64% | 5.75% |
| Huawei | 49 | R1-2110811 | R15/16CDRX | 16 | 8 | 8 | 0 | L | 3 | 7 | 97.62% | 10.79% |
| Huawei | 50 | R1-2110811 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 3 | 7 | 99.64% | 3.57% |
| Intel | 5 | R1-2111521 | Always On | 0 | 0 | 0 | 0 | L | 4 | 6 | 98.00% | 0.00% |
| Intel | 6 | R1-2111521 | Genie | 0 | 0 | 0 | 0 | L | 4 | 6 | 98.00% | 58.30% |
| Intel | 7 | R1-2111521 | CDRX | 8 | 6 | 6 | 0 | L | 4 | 6 | 95.00% | 10.80% |
| Intel | 8 | R1-2111521 | CDRX | 8 | 4 | 6 | 0 | L | 4 | 6 | 92.00% | 15.70% |
| Xiaomi | 5 | R1-2112573 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 4 | 8 | 100.00% | - |
| Xiaomi | 6 | R1-2112573 | Genie | 0 | 0 | 0 | 0 | L | 4 | 8 | 100.00% | 44.24% |

###### InH

Table 30 Summary of FR1, DL-only power evaluation results for InH

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| InH | VR/AR | 30 | R15/16 CDRX | High | 9.67 | 2.39 ~ 20.90 | vivo, CATT, Nokia, ID, ITRI, ZTE |
| Low | 4.7 | 3.67 ~ 5.72 | vivo |
| R17 PDCCH skipping | High | 20.73 |  | vivo |
| Low | 23.33 |  | vivo |
| VR/AR | 45 | R15/16 CDRX | High | 7.61 | 2.83 ~ 15.7 | vivo, ZTE, Nokia, ID |
| low | 4.39 | 3.46 ~ 5.32 | vivo |
| R17 PDCCH skipping | High | 17.15 | 14.41 ~ 19.89 | vivo, MTK |
| Low | 22.16 |  | vivo |
| Cross-slot + MIMO layer adaptation by BWP switching | High | 8.84 |  | MTK |
| Cross-slot + MIMO layer adaptation + PDCCH skipping by BWP switching | High | 9.31 |  | MTK |
| CG | 30 | R15/16 CDRX | High | 13.11 | 4.2 ~ 20.9 | Nokia, ZTE, ID |
| Low |  |  |  |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | | |

VR/AR

**Observations**

* In FR1, DL only evaluation, InH, VR/AR30 and high load, it is identified from Source vivo, CATT, Nokia, ID, ITRI, ZTE that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 16/12/4, 6/4/2, 10/8/4, 4/2/2, 8/4/4, 10/8/2, 16/8/8, 16/8/4, 16/8/6, 16/10/8, 16/12/8) provides the mean power saving gain of 9.67% in the range of 2.39 ~ 20.90% with *marginal* loss in DL UE satisfied rate.
* The choice of a particular R15/16 CDRX configuration (cycle, on duration, and inactivity timer) greatly affects the PS gain.
* In FR1, DL only evaluation, InH, VR/AR30 and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 20.73% with *marginal* loss in DL UE satisfied rate.

Table 31 Source specific data: FR1, DL-only, InH, VR/AR 30Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 9 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 10 | 10 | 92.50% | - |
| vivo | 10 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 10 | 10 | 91.25% | 4.88% |
| vivo | 11 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 10 | 10 | 91.81% | 3.24% |
| vivo | 15 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 10 | 10 | 92.17% | 20.73% |
| CATT | 1 | R1-2111234 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 12 | 12 | 95.83% | 0.00% |
| CATT | 2 | R1-2111234 | R15/16CDRX | 16 | 12 | 4 | 0 | H | 12 | 12 | 90.97% | 2.39% |
| CATT | 3 | R1-2111234 | R15/16CDRX | 6 | 4 | 2 | 0 | H | 12 | 12 | 88.89% | 6.14% |
| ZTE, Sanechips | 27 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | 0 | H | 11 | 11 | 93.18% | 0.00% |
| ZTE, Sanechips | 28 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | 0 | H | 10 | 11 | 93.00% | 0.00% |
| ZTE, Sanechips | 29 | R1-2111351 | R15 CDRX | 10 | 8 | 4 | 0 | H | 11 | 11 | 90.15% | 6.20% |
| Nokia | 6 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 5 | 5 | 90.00% | 20.90% |
| Nokia | 7 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 5 | 5 | 83.00% | 18.20% |
| Nokia | 8 | R1-2111828 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 5 | 5 | 0.00% | 16.20% |
| Nokia | 9 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 5 | 5 | 93.00% | 9.30% |
| Nokia | 10 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 5 | 5 | 74.00% | 17.30% |
| Interdigital | 6 | R1-2111830 | AlwaysOn - baseline | - | - | - | 0 | H | 5 | 5 | 96.80% | 0.00% |
| Interdigital | 7 | R1-2111830 | R15/16CDRX | 16 | 12 | 4 | 0 | H | 5 | 5 | 58.00% | 6.14% |
| Interdigital | 8 | R1-2111830 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 5 | 5 | 57.60% | 15.5% |
| Interdigital | 9 | R1-2111830 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 5 | 5 | 14.40% | 8.77% |
| Interdigital | 10 | R1-2111830 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 5 | 5 | 82.80% | 6.55% |
| ITRI | 12 | R1-2112175 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 4 | 4 | 97.91% | 14.86% |
| ITRI | 13 | R1-2112175 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 4 | 4 | 95.83% | 13.28% |
| ITRI | 14 | R1-2112175 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 4 | 4 | 85.42% | 10.22% |
| ITRI | 15 | R1-2112175 | R15/16CDRX | 16 | 8 | 2 | 0 | H | 4 | 4 | 68.75% | 16.31% |
| ITRI | 16 | R1-2112175 | R15/16CDRX | 16 | 8 | 4 | 0 | H | 4 | 4 | 81.25% | 14.79% |
| ITRI | 17 | R1-2112175 | R15/16CDRX | 16 | 8 | 6 | 0 | H | 4 | 4 | 83.33% | 12.46% |
| ITRI | 18 | R1-2112175 | R15/16CDRX | 16 | 2 | 8 | 0 | H | 4 | 4 | 12.50% | 27.51% |
| ITRI | 19 | R1-2112175 | R15/16CDRX | 16 | 4 | 8 | 0 | H | 4 | 4 | 35.42% | 20.18% |
| ITRI | 20 | R1-2112175 | R15/16CDRX | 16 | 6 | 8 | 0 | H | 4 | 4 | 58.33% | 14.87% |
| ITRI | 21 | R1-2112175 | R15/16CDRX | 16 | 10 | 8 | 0 | H | 4 | 4 | 95.83% | 5.97% |
| ITRI | 22 | R1-2112175 | R15/16CDRX | 16 | 12 | 8 | 0 | H | 4 | 4 | 100.00% | 5.30% |

**Observations**

* In FR1, DL only evaluation, InH, VR/AR30 and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4,16/14/4) provides the mean power saving gain of 4.7% in the range of 3.67 ~ 5.72% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, InH, VR/AR30 and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 23.33% with *marginal* loss in DL UE satisfied rate.

Table 32 Source specific data: FR1, DL-only, InH, VR/AR 30Mbps, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 1 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 5 | 10 | 100.00% | - |
| vivo | 2 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 5 | 10 | 100.00% | 5.72% |
| vivo | 3 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 5 | 10 | 100.00% | 3.67% |
| vivo | 7 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 5 | 10 | 100.00% | 23.33% |

**Observations**

* In FR1, DL only evaluation, InH, VR/AR45 and high load, it is identified from Source vivo, ZTE, Nokia, ID that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 10/8/4, 4/2/2, 8/4/4, 10/8/2) provides the mean power saving gain of 7.61% in the range of 2.83 ~ 15.7% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, InH, VR/AR45 and high load, it is identified from Source vivo, MTK that the R17 PDCCH skipping scheme provides the mean power saving gain of 17.15% in the range of 14.41% ~ 19.89% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, InH, VR/AR45 and high load, it is identified from Source MTK that cross-slot + MIMO layer adaptation by BWP switching scheme provides the mean power saving gain of 8.84% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, InH, VR/AR45 and high load, it is identified from Source MTK that cross-slot + MIMO layer adaptation + PDCCH skipping by BWP switching scheme provides the mean power saving gain of 9.31% with *marginal* loss in DL UE satisfied rate.

Table 33 Source specific data: FR1, DL-only, InH, VR/AR 45Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 25 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 5 | 5 | 96.67% | - |
| vivo | 26 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 5 | 5 | 92.78% | 4.68% |
| vivo | 27 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 5 | 5 | 94.44% | 2.83% |
| vivo | 31 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 5 | 5 | 96.67% | 19.89% |
| ZTE, Sanechips | 32 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | 0 | H | 7 | 7 | 91.00% | 0.00% |
| ZTE, Sanechips | 33 | R1-2111351 | R15 CDRX | 10 | 8 | 4 | 0 | H | 7 | 7 | 87.00% | 7.40% |
| Nokia | 11 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 3 | 3 | 95.00% | 15.70% |
| Nokia | 12 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 3 | 3 | 84.70% | 12.10% |
| Nokia | 13 | R1-2111828 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 3 | 3 | 0.00% | 9.40% |
| Nokia | 14 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 3 | 3 | 97.00% | 4.00% |
| Nokia | 15 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 3 | 3 | 63.00% | 10.80% |
| Interdigital | 11 | R1-2111830 | AlwaysOn - baseline | - | - | - | 0 | H | 3 | 3 | 98.00% | 0.00% |
| Interdigital | 12 | R1-2111830 | R15/16CDRX | 16 | 12 | 4 | 0 | H | 3 | 3 | 63.34% | 5.76% |
| Interdigital | 13 | R1-2111830 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 3 | 3 | 63.34% | 15.12% |
| Interdigital | 14 | R1-2111830 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 3 | 3 | 14.67% | 8.53% |
| Interdigital | 15 | R1-2111830 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 3 | 3 | 85.30% | 6.54% |
| MTK | 11 | R1-2109555 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 4 | 4 | 91.67% | 0.00% |
| MTK | 12 | R1-2109555 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 4 | 4 | 70.83% | 4.45% |
| MTK | 13 | R1-2109555 | Custom : cross-slot  + MIMO layer adaptation  by BWP switching | 0 | 0 | 0 | 0 | H | 4 | 4 | 88.73% | 8.84% |
| MTK | 14 | R1-2109555 | Custom : cross-slot  + MIMO layer adaptation  +PDCCH skipping by BWP switching | 0 | 0 | 0 | 0 | H | 4 | 4 | 84.80% | 9.31% |
| MTK | 15 | R1-2109555 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 4 | 4 | 90.00% | 14.41% |

**Observations**

* In FR1, DL only evaluation, InH, VR/AR45 and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4,16/14/4) provides the mean power saving gain of 4.39% in the range of 3.46 ~ 5.32% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, InH, VR/AR45 and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 22.16% with *marginal* loss in DL UE satisfied rate.

Table 34 Source specific data: FR1, DL-only, InH, VR/AR 45Mbps, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 23 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 3 | 5 | 100% | - |
| vivo | 24 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 3 | 5 | 100% | 5.32% |
| vivo | 25 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 3 | 5 | 100% | 3.46% |
| vivo | 29 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 3 | 5 | 100% | 22.16% |

CG

**Observations**

* In FR1, DL only evaluation, InH, CG30 and high load, it is identified from Source ZTE, Nokia, ID that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 4/2/2, 8/4/4, 16/8/8, 10/8/2, 10/5/5, 10/8/2) provides the mean power saving gain of 13.11% in the range of 4.2 ~ 20.90% with *marginal* loss in DL UE satisfied rate.
* The choice of a particular R15/16 CDRX configuration (cycle, on duration, and inactivity timer) greatly affects the PS gain.

Table 35 Source specific data: FR1, DL-only, InH, CG 30Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| ZTE, Sanechips | 36 | R1-2111351 | AlwaysOn-baseline | 0 | 0 | 0 | 0 | H | 12 | 12 | 96.53% | 0.00% |
| ZTE, Sanechips | 37 | R1-2111351 | R15 CDRX | 10 | 8 | 4 | 0 | H | 12 | 12 | 88.88% | 4.20% |
| Nokia | 1 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 5 | 5 | 96.80% | 20.90% |
| Nokia | 2 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 5 | 5 | 96.70% | 18.20% |
| Nokia | 3 | R1-2111828 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 5 | 5 | 95.00% | 16.20% |
| Nokia | 4 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 5 | 5 | 98.50% | 9.30% |
| Nokia | 5 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 5 | 5 | 96.30% | 17.30% |
| Interdigital | 1 | R1-2111830 | AlwaysOn - baseline | - | - | - | 0 | H | 7 | 7 | 97.57% | 0.00% |
| Interdigital | 2 | R1-2111830 | R15/16CDRX | 16 | 12 | 4 | 0 | H | 7 | 7 | 79.90% | 5.52%\* |
| Interdigital | 3 | R1-2111830 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 7 | 7 | 64.71% | 13.63%\* |
| Interdigital | 4 | R1-2111830 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 7 | 7 | 55.70% | 6.95%\* |
| Interdigital | 5 | R1-2111830 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 7 | 7 | 83.30% | 5.68%\* |
| ITRI | 1 | R1-2112175 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 9 | 9 | 57.40% | 14.51% |
| ITRI | 2 | R1-2112175 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 9 | 9 | 56.40% | 12.62% |
| ITRI | 3 | R1-2112175 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 9 | 9 | 46.29% | 9.74% |
| ITRI | 4 | R1-2112175 | R15/16CDRX | 16 | 8 | 2 | 0 | H | 9 | 9 | 20.37% | 15.35% |
| ITRI | 5 | R1-2112175 | R15/16CDRX | 16 | 8 | 4 | 0 | H | 9 | 9 | 29.63% | 13.37% |
| ITRI | 6 | R1-2112175 | R15/16CDRX | 16 | 8 | 6 | 0 | H | 9 | 9 | 39.81% | 11.42% |
| ITRI | 7 | R1-2112175 | R15/16CDRX | 16 | 2 | 8 | 0 | H | 9 | 9 | 5.56% | 28.88% |
| ITRI | 8 | R1-2112175 | R15/16CDRX | 16 | 4 | 8 | 0 | H | 9 | 9 | 10.18% | 20.03% |
| ITRI | 9 | R1-2112175 | R15/16CDRX | 16 | 6 | 8 | 0 | H | 9 | 9 | 27.78% | 14.39% |
| ITRI | 10 | R1-2112175 | R15/16CDRX | 16 | 10 | 8 | 0 | H | 9 | 9 | 53.70% | 5.37% |
| ITRI | 11 | R1-2112175 | R15/16CDRX | 16 | 12 | 8 | 0 | H | 9 | 9 | 70.37% | 4.92% |

No input for FR1, DL-only, CG30, low load case

###### UMa

Table 36 Summary of FR1, DL-only power evaluation results for UMa

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| UMa | VR/AR | 30 | R15/16 CDRX | High | 4.13 | 3.23 ~ 5.02 | vivo |
| Low | 5.16 | 4.05 ~ 6.26 | vivo |
| R17 PDCCH skipping | High | 20.54 |  | vivo |
| Low | 25.15 |  | vivo |
| 45 | R15/16 CDRX | High | 4.03 | 3.13 ~ 4.92 | vivo |
| Low | 4.89 | 3.97 ~ 5.81 | vivo |
| R17 PDCCH skipping | High | 20.17 |  | vivo |
| Low | 23.25 |  | vivo |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | | |

VR/AR

**Observations**

* In FR1, DL only evaluation, UMa, VR/AR30 and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/8, 16/14/4) provides the mean power saving gain of 4.13% in the range of 3.23 ~ 5.02% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, UMa, VR/AR30 and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 20.54% with *marginal* loss in DL UE satisfied rate.

Table 37 Source specific data: FR1, DL-only, UMa, VR/AR, 30Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 73 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 8 | 8 | 93.75% | - |
| vivo | 74 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 8 | 8 | 91.47% | 5.02% |
| vivo | 75 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 8 | 8 | 92.85% | 3.23% |
| vivo | 79 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 8 | 8 | 93.75% | 20.54% |

**Observations**

* In FR1, DL only evaluation, UMa, VR/AR30 and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 5.16% in the range of 4.05 ~ 6.26% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, UMa, VR/AR30 and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 25.15% with *marginal* loss in DL UE satisfied rate.

Table 38 Source specific data: FR1, DL-only, UMa, VR/AR, 30Mbps, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 65 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 4 | 8 | 98.81% | - |
| vivo | 66 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 4 | 8 | 98.41% | 6.26% |
| vivo | 67 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 4 | 8 | 98.81% | 4.05% |
| vivo | 71 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 4 | 8 | 98.81% | 25.15% |

**Observations**

* In FR1, DL only evaluation, UMa, VR/AR45 and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 4.03% in the range of 3.13 ~ 4.92% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, UMa, VR/AR45 and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 20.17% with *marginal* loss in DL UE satisfied rate.

Table 39 Source specific data: FR1, DL-only, UMa, VR/AR, 45Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 89 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 4 | 4 | 94.05% | - |
| vivo | 90 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 4 | 4 | 92.46% | 4.92% |
| vivo | 91 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 4 | 4 | 93.25% | 3.13% |
| vivo | 95 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 4 | 4 | 93.33% | 20.17% |

**Observations**

* In FR1, DL only evaluation, UMa, VR/AR45 and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4/, 16/14/4) provides the mean power saving gain of 4.89% in the range of 3.97 ~ 5.81% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, UMa, VR/AR45 and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 23.25% with *marginal* loss in DL UE satisfied rate.

Table 40 Source specific data: FR1, DL-only, UMa, VR/AR, 45Mbps, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 81 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 2 | 4 | 96.83% | - |
| vivo | 82 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 2 | 4 | 96.83% | 5.81% |
| vivo | 83 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 2 | 4 | 96.83% | 3.97% |
| vivo | 87 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 2 | 4 | 96.83% | 23.25% |

CG

No results were submitted

##### UL-only Evaluation

###### DU

Table 41 Summary of FR1, UL-only power evaluation results for DU

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | UL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS gain (%), Note 1 | | source |
| Mean (%) | Range (%) |  |
| DU | VR/CG UL Pose | 0.2 | R15/16 CDRX | High | 31.95 | 26.62 ~ 37.27 | vivo |
| Low |  |  |  |
| 0.048 | R16 cross slot scheduling | High | 20.84 |  | MTK |
| R17 PDCCH skipping | High | 15.32 |  | MTK |
| R17 PDCCH skipping + R16 cross slot scheduling | High | 28.58 |  | MTK |
|  | AR UL 1 stream (scene) | 10 | R15/16 CDRX | High | 8.48 | 4.25 ~ 14.6 | Vivo, Nokia |
| Low | 5.62 | 4.26 ~ 6.97 | vivo |
| R17 PDCCH skipping | High | 26.76 | 19.36 ~ 34.15 | Vivo, MTK |
| Low | 35.84 |  | vivo |
| R16 cross slot scheduling | high | 24.33 |  | MTK |
| R17 PDCCH skipping + cross slot scheduling | high | 32.80 |  | MTK |
| AR UL 2 streams (pose, scene) | 10.2 | R15/16 CDRX | High | 2.17 | 1.99 ~ 3.43 | vivo |
| Low | 2.51 | 1.79 ~ 3.23 | vivo |
| R17 PDCCH skipping | High | 23.02 |  | vivo |
| Low | 24.16 |  | vivo |
| Note 1 : PSG was computed for the cases only with marginal loss in % of UL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | | |

VR/CG

**Observations**

* In FR1, UL only evaluation, DU, VR/CG UL pose (250Hz) and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (4/2/1, 8/3/1) provides the mean power saving gain of 31.95% in the range of 26.62 ~ 37.27% with *marginal[[3]](#footnote-3)* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, DU, VR/CG UL pose (60Hz) and high load, it is identified from Source MTK that the R16 cross slot scheduling scheme provides the mean power saving gain of 20.48% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, DU, VR/CG UL pose (60Hz) and high load, it is identified from Source MTK that the R17 PDCCH skipping scheme provides the mean power saving gain of 15.32% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, DU, VR/CG UL pose (60Hz) and high load, it is identified from Source MTK that the R17 PDCCH skipping + cross slot scheduling scheme provide the mean power saving gain of 28.58% with *marginal* loss in UL UE satisfied rate.

Table 42 Source specific data: FR1, UL-only, DU, VR/CG-Pose only, 0.2Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 158 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | UL pose rate 250Hz | H | 20 | 20 | 99.99% | - |
| vivo | 159 | R1-2111046 | R15/16CDRX | 4 | 2 | 1 | UL pose rate 250Hz | H | 20 | 20 | 94.84% | 26.62% |
| vivo | 160 | R1-2111046 | R15/16CDRX | 8 | 3 | 1 | UL pose rate 250Hz | H | 20 | 20 | 93.81% | 37.27% |
| MTK | 16 | R1-2109555 | AlwaysOn - baseline | 0 | 0 | 0 | UL pose rate 60Hz | H | 13 | 13 | 100.00% | 0.00% |
| MTK | 17 | R1-2109555 | Cross slot scheduling | 0 | 0 | 0 | UL pose rate 60Hz | H | 13 | 13 | 100.00% | 20.48% |
| MTK | 18 | R1-2109555 | R17 PDCCH skipping | 0 | 0 | 0 | UL pose rate 60Hz | H | 13 | 13 | 100.00% | 15.32% |
| MTK | 19 | R1-2109555 | Custom : R17 PDCCH skipping  + cross slot | 0 | 0 | 0 | UL pose rate 60Hz | H | 13 | 13 | 100.00% | 28.58% |

AR

AR with UL 1 stream

**Observations**

* In FR1, UL only evaluation, DU, AR UL 1 stream and high load, it is identified from Source vivo, Nokia that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 4/2/2, 8/4/4, 16/8/8, 10/8/2, 10/5/5) provides the mean power saving gain of 8.48% in the range of 4.25 ~ 14.60% with *marginal* loss in UL UE satisfied rate.
* The choice of a particular R15/16 CDRX configuration (cycle, on duration, and inactivity timer) greatly affects the PS gain.
* In FR1, UL only evaluation, DU, AR UL 1 stream and high load, it is identified from Source vivo, MTK that the R17 PDCCH skipping scheme provides the mean power saving gain of 26.76% in the range of 19.36 ~ 34.15% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, DU, AR UL 1 stream and high load, it is identified from Source MTK that the cross-slot scheduling scheme provides the mean power saving gain of 24.33% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, DU, AR UL 1 stream and high load, it is identified from Source MTK that the R16 PDCCH skipping + cross slot scheduling scheme provides the mean power saving gain of 32.80% with *marginal* loss in UL UE satisfied rate.

Table 43 Source specific data: FR1, UL-only, DU, AR UL 1 stream, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 166 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 9 | 9 | 92.95% | - |
| vivo | 167 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 9 | 9 | 91.53% | 6.73% |
| vivo | 168 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 9 | 9 | 91.17% | 4.25% |
| vivo | 170 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 9 | 9 | 91.77% | 34.15% |
| Nokia | 46 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 4 | 4 | 91.20% | 14.60% |
| Nokia | 47 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 4 | 4 | 91.40% | 10.80% |
| Nokia | 48 | R1-2111828 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 4 | 4 | 91.40% | 7.50% |
| Nokia | 49 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 4 | 4 | 91.30% | 5.80% |
| Nokia | 50 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 4 | 4 | 91.40% | 9.70% |
| MTK | 24 | R1-2109555 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 6 | 6 | 100.00% | 0.00% |
| MTK | 25 | R1-2109555 | Cross slot scheduling | 0 | 0 | 0 | 0 | H | 6 | 6 | 100.00% | 24.33% |
| MTK | 26 | R1-2109555 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 6 | 6 | 100.00% | 19.36% |
| MTK | 27 | R1-2109555 | Custom : R17 PDCCH skipping  + cross slot | 0 | 0 | 0 | 0 | H | 6 | 6 | 100.00% | 32.80% |

**Observations**

* In FR1, UL only evaluation, DU, AR UL 1 stream and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 5.62% in the range of 4.26 ~ 6.97% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, DU, AR UL 1 stream and low load, it is identified from Source vivo that the R16 PDCCH skipping scheme provides the mean power saving gain of 35.84% with *marginal* loss in UL UE satisfied rate.

Table 44 Source specific data: FR1, UL-only, DU, AR UL 1 stream, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 161 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 5 | 9 | 97.14% | - |
| vivo | 162 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 5 | 9 | 97.14% | 6.97% |
| vivo | 163 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 5 | 9 | 97.14% | 4.26% |
| vivo | 165 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 5 | 9 | 96.51% | 35.84% |

AR with UL 2 streams

**Observations**

* In FR1, UL only evaluation, DU, AR UL 2 stream and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 2.17% in the range of 1.99 ~ 3.43% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, DU, AR UL 2 stream and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 23.02% with *marginal* loss in UL UE satisfied rate.

Table 45 Source specific data: FR1, UL-only, DU, AR 2 streams, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 215 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 7 | 7 | 92.29% | - |
| vivo | 216 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 7 | 7 | 90.70% | 3.43% |
| vivo | 217 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 7 | 7 | 92.06% | 1.99% |
| vivo | 219 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 7 | 7 | 91.16% | 23.02% |

**Observations**

* In FR1, UL only evaluation, DU, AR UL 2 stream and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 2.51% in the range of 1.79 ~ 3.23% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, DU, AR UL 2 stream and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 24.16% with *marginal* loss in UL UE satisfied rate.

Table 46 Source specific data: FR1, UL-only, DU, AR 2 streams, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 210 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 4 | 7 | 100.00% | - |
| vivo | 211 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 4 | 7 | 100.00% | 3.23% |
| vivo | 212 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 4 | 7 | 100.00% | 1.79% |
| vivo | 214 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 4 | 7 | 100.00% | 24.16% |

###### InH

Table 47 Summary of FR1, UL-only power evaluation results for InH

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | UL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS gain (%), Note 1 | | source |
| Mean (%) | Range (%) |  |
| InH | VR/CG UL Pose | 0.2 | R15/16 CDRX | High | 31.58 | 26.33 ~ 36.83 | vivo |
| Low |  |  |  |
| 0.048 | Cross slot scheduling | High | 20.56 |  | MTK |
| Low |  |  |  |
| R17 PDCCH skipping | High | 15.29 |  | MTK |
| Low |  |  |  |
| R17 PDCCH skipping + cross slot scheduling | High | 28.60 |  | MTK |
| Low |  |  |  |
| AR UL 1 stream (scene) | 10 | R15/16 CDRX | High | 13.04 | 4.8 ~ 21.64 | vivo, Nokia |
| Low | 6.60 | 5.03 ~ 8.17 | vivo |
| R17 PDCCH skipping | High | 28.43 | 17.63 ~ 39.21 | Vivo, MTK |
| Low | 41.99 |  | vivo |
| R16 cross slot scheduling | High | 23.87 |  | MTK |
| Low |  |  |  |
| R17 PDCCH skipping + R16 cross slot scheduling | High | 31.56 |  | MTK |
| Low |  |  |  |
| AR UL 2 streams (pose, scene) | 10.2 | R15/16 CDRX | High | 3.16 | 2.34 ~ 3.97 | vivo |
| Low | 3.6 | 2.38 ~ 4.82 | vivo |
| R17 PDCCH skipping | High | 25.63 |  | vivo |
| Low | 28.15 |  | vivo |
| Note 1 : PSG was computed for the cases only with marginal loss in % of UL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | |  |

VR/CG

**Observations**

* In FR1, UL only evaluation, InH, VR/CG UL pose (250Hz) and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (4/2/1, 8/3/1) provides the mean power saving gain of 31.58% in the range of 26.33 ~ 36.83% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, InH, VR/CG UL pose (60Hz) and high load, it is identified from Source MTK that the cross-slot scheduling scheme provides the mean power saving gain of 20.56% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, InH, VR/CG UL pose (60Hz) and high load, it is identified from Source MTK that the R17 PDCCH skipping scheme provides the mean power saving gain of 15.29% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, InH, VR/CG UL pose (60Hz) and high load, it is identified from Source MTK that the R17 PDCCH skipping + cross slot scheduling scheme provides the mean power saving gain of 28.60% with *marginal* loss in UL UE satisfied rate.

Table 48 Source specific data: FR1, UL-only, InH, VR/CG Pose only, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 145 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | UL Pose rate  250Hz | H | 20 | 20 | 100.00% | - |
| vivo | 146 | R1-2111046 | R15/16CDRX | 4 | 2 | 1 | UL Pose rate  250Hz | H | 20 | 20 | 94.31% | 26.33% |
| vivo | 147 | R1-2111046 | R15/16CDRX | 8 | 3 | 1 | UL Pose rate  250Hz | H | 20 | 20 | 93.33% | 36.83% |
| MTK | 20 | R1-2109555 | AlwaysOn - baseline | 0 | 0 | 0 | UL Pose rate  60Hz | H | 9 | 9 | 100.00% | 0.00% |
| MTK | 21 | R1-2109555 | Cross slot scheduling | 0 | 0 | 0 | UL Pose rate  60Hz | H | 9 | 9 | 100.00% | 20.56% |
| MTK | 22 | R1-2109555 | R17 PDCCH skipping | 0 | 0 | 0 | UL Pose rate  60Hz | H | 9 | 9 | 100.00% | 15.29% |
| MTK | 23 | R1-2109555 | Custom : R17  PDCCH skipping  + cross slot | 0 | 0 | 0 | UL Pose rate  60Hz | H | 9 | 9 | 100.00% | 28.60% |

AR

AR with UL 1 stream

**Observations**

* In FR1, UL only evaluation, InH, AR UL 1 stream and high load, it is identified from Source vivo, Nokia that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 4/2/2, 8/4/4, 16/8/8/, 10/8/2, 10/5/5) provides the mean power saving gain of 13.04% in the range of 4.8 ~ 21.64% with *marginal* loss in UL UE satisfied rate.
* The choice of a particular R15/16 CDRX configuration (cycle, on duration, and inactivity timer) greatly affects the PS gain.
* In FR1, UL only evaluation, InH, AR UL 1 stream and high load, it is identified from Source vivo, MTK that the R17 PDCCH skipping scheme provides the mean power saving gain of 28.43% in the range of 17.65 ~ 39.21% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, InH, AR UL 1 stream and high load, it is identified from Source MTK that the R16 cross slot scheduling scheme provides the mean power saving gain of 23.87% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, InH, AR UL 1 stream and high load, it is identified from Source MTK that the R17 PDCCH skipping + R16 cross slot scheduling scheme provides the mean power saving gain of 31.56% with *marginal* loss in UL UE satisfied rate.

Table 49 Source specific data: FR1, UL-only, InH, AR UL 1 stream, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 153 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 13 | 13 | 93.59% | - |
| vivo | 154 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 13 | 13 | 92.22% | 7.71% |
| vivo | 155 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 13 | 13 | 92.86% | 4.80% |
| vivo | 157 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 13 | 13 | 92.65% | 39.21% |
| Nokia | 51 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 4 | 4 | 99.00% | 21.64% |
| Nokia | 52 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 4 | 4 | 99.00% | 18.27% |
| Nokia | 53 | R1-2111828 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 4 | 4 | 99.00% | 13.50% |
| Nokia | 54 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 4 | 4 | 99.00% | 8.67% |
| Nokia | 55 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 4 | 4 | 99.00% | 16.67% |
| MTK | 28 | R1-2109555 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 4 | 4 | 100.00% | 0.00% |
| MTK | 29 | R1-2109555 | Cross slot scheduling | 0 | 0 | 0 | 0 | H | 4 | 4 | 100.00% | 23.87% |
| MTK | 30 | R1-2109555 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 4 | 4 | 100.00% | 17.65% |
| MTK | 31 | R1-2109555 | Custom : R17 PDCCH  skipping + cross slot | 0 | 0 | 0 | 0 | H | 4 | 4 | 100.00% | 31.56% |

**Observations**

* In FR1, UL only evaluation, InH, AR UL 1 stream and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 6.60% in the range of 5.03 ~ 8.17% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, InH, AR UL 1 stream and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 41.99% with *marginal* loss in UL UE satisfied rate.

Table 50 Source specific data: FR1, UL-only, InH, AR UL 1 stream, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 148 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 7 | 13 | 100% | - |
| vivo | 149 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 7 | 13 | 100% | 8.17% |
| vivo | 150 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 7 | 13 | 100% | 5.03% |
| vivo | 152 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 7 | 13 | 100% | 41.99% |

AR with UL 2 streams

**Observations**

* In FR1, UL only evaluation, InH, AR UL 2 streams and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 3.16% in the range of 2.34 ~ 3.97% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, InH, AR UL 2 streams and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 25.63% with *marginal* loss in UL UE satisfied rate.

Table 51 Source specific data: FR1, UL-only, InH, AR UL 2 stream, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 205 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 12 | 12 | 93.29% | - |
| vivo | 206 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 12 | 12 | 92.13% | 3.97% |
| vivo | 207 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 12 | 12 | 92.59% | 2.34% |
| vivo | 209 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 12 | 12 | 92.36% | 25.63% |

**Observations**

* In FR1, UL only evaluation, InH, AR UL 2 streams and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 3.6% in the range of 2.38 ~ 4.82% with *marginal* loss in UL UE satisfied rate.
* In FR1, UL only evaluation, InH, AR UL 2 streams and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 28.15% with *marginal* loss in UL UE satisfied rate.

Table 52 Source specific data: FR1, UL-only, InH, AR UL 2 stream, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 200 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 6 | 12 | 100.00% | - |
| vivo | 201 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 6 | 12 | 100.00% | 4.82% |
| vivo | 202 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 6 | 12 | 100.00% | 2.38% |
| vivo | 204 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 6 | 12 | 100.00% | 28.15% |

###### UMa

Table 53 Summary of FR1, UL-only power evaluation results for UMa

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | UL Bit rate (Mbps) | PS scheme | System Load | PS gain (%), Note 1 | | source |
| Mean (%) | Range (%) |  |
| UMa | VR/CG UL Pose | 0.2 | R15/16 CDRX | High | 33.52 | 28.1 ~ 38.93 | vivo |
| Low |  |  |  |
| Note 1 : PSG was computed for the cases only with marginal loss in % of UL satisfied UE. | | | | | | |  |

VR/CG

**Observations**

* In FR1, UL only evaluation, UMa, VR/CG Pose only and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (4/2/1, 8/3/1) provides the mean power saving gain of 33.52% in the range of 28.10 ~ 38.93% with *marginal* loss in UL UE satisfied rate.

Table 54 Source specific data: FR1, UL-only, UMa, VR/CG Pose only(250Hz), 0.2Mbps, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 171 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 20 | 20 | 97.70% | - |
| vivo | 172 | R1-2111046 | R15/16CDRX | 4 | 2 | 1 | 0 | H | 20 | 20 | 94.37% | 28.10% |
| vivo | 173 | R1-2111046 | R15/16CDRX | 8 | 3 | 1 | 0 | H | 20 | 20 | 92.94% | 38.93% |

AR

No results were submitted.

#### FR2

##### DL+UL Evaluation

No results submitted.

##### DL-only Evaluation

###### DU

Table 55 Summary of FR2, DL-only power evaluation results for DU

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS gain (%), Note 1 | | source |
| Mean (%) | Range (%) |  |
| DU | VR/AR | 30 | R15/16 CDRX | High | 7.73 | 5.96 ~ 9.5 | vivo, QC |
| Low | 8.28 | 6.4 ~ 10.15 | vivo |
| R17 PDCCH skipping | High | 31.24 |  | vivo |
| Low | 31.74 |  | vivo |
| 45 | R15/16 CDRX | High | 6.64 | 4.98 ~ 8.29 | vivo |
| Low | 7.63 | 6.06 ~ 9.2 | vivo |
| R17 PDCCH skipping | High | 26.33 |  | vivo |
| Low | 28.25 |  | vivo |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | | |

VR/AR

**Observations**

* In FR2, DL only evaluation, DU, VR/AR30 and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 7.73% in the range of 5.96 ~ 9.5% with *marginal*[[4]](#footnote-4) loss in DL UE satisfied rate.
* In FR2, DL only evaluation, DU, VR/AR30 and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 31.24% with *marginal* loss in DL UE satisfied rate.

Table 56 Source specific data: FR2, DL-only, DU, VR/AR30, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power  saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional  Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 127 | R1-2111046 | AlwaysOn  - baseline | 0 | 0 | 0 | 0 | H | 13 | 13 | 95.24% | - |
| vivo | 128 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 13 | 13 | 91.82% | 9.50% |
| vivo | 129 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 13 | 13 | 93.53% | 5.96% |
| vivo | 131 | R1-2111046 | R17 PDCCH  skipping | 0 | 0 | 0 | 0 | H | 13 | 13 | 95.00% | 31.24% |
| QC | 71 | R1-2112244 | ALWAYS ON | None | None | None | 0 | H | 7 | 7 | 90.00% | 0.00% |
| QC | 72 | R1-2112244 | CDRX | 16 | 4 | 4 | 0 | H | 7 | 7 | 0.00% | 26.77% |
| QC | 73 | R1-2112244 | CDRX | 16 | 8 | 8 | 0 | H | 7 | 7 | 45.00% | 8.77% |
| QC | 74 | R1-2112244 | CDRX | 16 | 8 | 16 | 0 | H | 7 | 7 | 60.00% | 3.34% |
| QC | 75 | R1-2112244 | Genie (CDRX  with ideal  PDCCH Skipping) | 16 | None | none | Genie is the  same  for all CDRX | H | 7 | 7 | 90.00% | 69.00% |

**Observations**

* In FR2, DL only evaluation, DU, VR/AR30 and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 8.28% in the range of 6.4 ~ 10.15% with *marginal* loss in DL UE satisfied rate.
* In FR2, DL only evaluation, DU, VR/AR30 and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 31.74% with *marginal* loss in DL UE satisfied rate.

Table 57 Source specific data: FR2, DL-only, DU, VR/AR30, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 121 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 7 | 13 | 99.55% | - |
| vivo | 122 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 7 | 13 | 98.64% | 10.15% |
| vivo | 123 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 7 | 13 | 99.32% | 6.40% |
| vivo | 125 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 7 | 13 | 99.32% | 31.74% |

**Observations**

* In FR2, DL only evaluation, DU, VR/AR45 and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4) provides the mean power saving gain of 6.64% in the range of 4.98 ~ 8.29% with *marginal* loss in DL UE satisfied rate.
* In FR2, DL only evaluation, DU, VR/AR45 and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 26.33% with *marginal* loss in DL UE satisfied rate.

Table 58 Source specific data: FR2, DL-only, DU, VR45, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 139 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 8 | 8 | 93.25% | - |
| vivo | 140 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 8 | 8 | 91.67% | 8.29% |
| vivo | 141 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 8 | 8 | 32.26% | 4.98% |
| vivo | 143 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 8 | 8 | 93.25% | 26.33% |

**Observations**

* In FR2, DL only evaluation, DU, VR/AR45 and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 7.63% in the range of 6.06 ~ 9.2% with *marginal* loss in DL UE satisfied rate.
* In FR2, DL only evaluation, DU, VR/AR45 and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 28.25% with *marginal* loss in DL UE satisfied rate.

Table 59 Source specific data: FR2, DL-only, DU, VR45, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 133 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 4 | 8 | 100.00% | - |
| vivo | 134 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 4 | 8 | 100.00% | 9.20% |
| vivo | 135 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 4 | 8 | 100.00% | 6.06% |
| vivo | 137 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 4 | 8 | 100.00% | 28.25% |

CG

No results available

###### InH

Table 60 Summary of FR2, DL-only power evaluation results for InH

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS gain (%), Note 1 | | source |
| Mean (%) | Range (%) |
| InH | VR/AR | 30 | R15/16 CDRX | High | 10.78 | 5.81 ~ 19.58 | vivo, Nokia, QC |
| Low | 8.17 | 6.28 ~ 10.06 | vivo |
| R17 PDCCH skipping | High | 32.69 |  | vivo |
| Low | 33.80 |  | vivo |
| 45 | R15/16 CDRX | High | 7.46 | 5.73 ~ 18.00 | Vivo, Nokia |
| Low | 7.75 | 5.98 ~ 9.52 | vivo |
| R17 PDCCH skipping | High | 28.58 | 27.36 ~ 29.8 | vivo, QC |
| Low | 28.87 |  | vivo |
| R16 cross slot scheduling | High | 12.20 |  | QC |
| R17 PDCCH skipping + cross slot scheduling | High | 30 |  | QC |
| CG | 30 | R15/16 CDRX | High | 13.03 | 3.79 ~ 22.66 | Nokia, QC |
| Low |  |  |  |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | | |

VR/AR

**Observations**

* In FR2, DL only evaluation, InH, VR/AR30 and high load, it is identified from Source vivo, Nokia, QC that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 4/2/2, 10/8/2) provides the mean power saving gain of 10.78% in the range of 5.81 ~ 19.58% with *marginal* loss in DL UE satisfied rate.
* The choice of a particular R15/16 CDRX configuration (cycle, on duration, and inactivity timer) greatly affects the PS gain.

**Observations**

* In FR2, DL only evaluation, DU, VR/AR30 and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 32.69% with *marginal* loss in DL UE satisfied rate.

Table 61 Source specific data: FR2, DL-only, InH, VR/AR30, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 103 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 8 | 8 | 92.01% | - |
| vivo | 104 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 8 | 8 | 90.63% | 9.53% |
| vivo | 105 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 8 | 8 | 91.37% | 5.81% |
| vivo | 107 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 8 | 8 | 92.01% | 32.69% |
| Nokia | 21 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 10 | 10 | 85.58% | 19.58% |
| Nokia | 22 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 10 | 10 | 20.66% | 16.41% |
| Nokia | 23 | R1-2111828 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 10 | 10 | 0.00% | 13.16% |
| Nokia | 24 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 10 | 10 | 92.41% | 8.21% |
| Nokia | 25 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 10 | 10 | 7.16% | 14.92% |
| QC | 66 | R1-2112244 | ALWAYS ON | None | None | None | 0 | H | 7 | 7 | 90.00% | 0.00% |
| QC | 67 | R1-2112244 | CDRX | 16 | 4 | 4 | 0 | H | 7 | 7 | 0.00% | 28.44% |
| QC | 68 | R1-2112244 | CDRX | 16 | 8 | 8 | 0 | H | 7 | 7 | 50.00% | 9.64% |
| QC | 69 | R1-2112244 | CDRX | 16 | 8 | 16 | 0 | H | 7 | 7 | 65.00% | 4.10% |
| QC | 70 | R1-2112244 | Genie (CDRX  with ideal  PDCCH  Skipping) | 16 | None | noe | Genie is  the same  for all CDRX | H | 7 | 7 | 90.00% | 73.50% |
| QC | 76 | R1-2112244 | ALWAYS ON | None | None | None | 0 | H | 7 | 7 | 90.00% | 0.00% |
| QC | 80 | R1-2112244 | ALWAYS ON | None | None | None | 0 | H | 7 | 7 | 90.00% | 0.00% |

**Observations**

* In FR2, DL only evaluation, InH, VR/AR30 and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 8.17% in the range of 6.28 ~ 10.06% with *marginal* loss in DL UE satisfied rate.

**Observations**

* In FR2, DL only evaluation, DU, VR/AR30 and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 33.80% with *marginal* loss in DL UE satisfied rate.

Table 62 Source specific data: FR2, DL-only, InH, VR/AR30, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 97 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 4 | 8 | 100.00% | - |
| vivo | 98 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 4 | 8 | 99.31% | 10.06% |
| vivo | 99 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 4 | 8 | 99.31% | 6.28% |
| vivo | 101 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 4 | 8 | 100.00% | 33.80% |

**Observations**

* In FR2, DL only evaluation, InH, VR/AR45 and high load, it is identified from Source vivo, Nokia that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4, 10/8/2) provides the mean power saving gain of 7.46% in the range of 5.73 ~ 9.15% with *marginal* loss in DL UE satisfied rate.
* The choice of a particular R15/16 CDRX configuration (cycle, on duration, and inactivity timer) greatly affects the PS gain.

**Observations**

* In FR2, DL only evaluation, InH, VR/AR45 and high load, it is identified from Source vivo, QC that the R17 PDCCH skipping scheme provides the mean power saving gain of 28.58% in the range of 27.36 ~ 29.8% with *marginal* loss in DL UE satisfied rate.
* In FR2, DL only evaluation, InH, VR/AR45 and high load, it is identified from Source QC that the R16 cross slot scheduling scheme provides the mean power saving gain of 12.20% with *marginal* loss in DL UE satisfied rate.
* In FR2, DL only evaluation, InH, VR/AR45 and high load, it is identified from Source QC that the R17 PDCCH skipping + cross slot scheduling scheme provides the mean power saving gain of 30.0% with *marginal* loss in DL UE satisfied rate.

Table 63 Source specific data: FR2, DL-only, InH, VR/AR45, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 115 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 4 | 4 | 94.44% | - |
| vivo | 116 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 4 | 4 | 91.67% | 9.15% |
| vivo | 117 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 4 | 4 | 93.75% | 5.73% |
| vivo | 119 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 4 | 4 | 93.75% | 27.36% |
| Nokia | 26 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 6 | 6 | 75.56% | 18.00% |
| Nokia | 27 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 6 | 6 | 9.40% | 15.00% |
| Nokia | 28 | R1-2111828 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 6 | 6 | 0.00% | 11.60% |
| Nokia | 29 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 6 | 6 | 90.00% | 7.50% |
| Nokia | 30 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 6 | 6 | 3.33% | 13.50% |
| QC | 1 | R1-2110402 | ALWAYS ON | Null | 0 | 0 | 0 | H | 3 | 3 | 90.00% | 0.00% |
| QC | 2 | R1-2110402 | Cross-slot scheduling | Null | 0 | 0 | 0 | H | 3 | 3 | 90.00% | 12.20% |
| QC | 3 | R1-2110402 | PDCCH Skipping | Null | 0 | 0 | 0 | H | 3 | 3 | 90.00% | 29.80% |
| QC | 4 | R1-2110402 | PDCCH Skipping  + Cross-slot skipping | Null | 0 | 0 | 0 | H | 3 | 3 | 90.00% | 30.00% |

**Observations**

* In FR2, DL only evaluation, InH, VR/AR45 and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 7.75% in the range of 5.98 ~ 9.52% with *marginal* loss in DL UE satisfied rate.
* In FR2, DL only evaluation, InH, VR/AR45 and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 28.87% with *marginal* loss in DL UE satisfied rate.

Table 64 Source specific data: FR2, DL-only, InH, VR45, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 109 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 2 | 4 | 100.00% | - |
| vivo | 110 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 2 | 4 | 98.61% | 9.52% |
| vivo | 111 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 2 | 4 | 98.61% | 5.98% |
| vivo | 113 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 2 | 4 | 98.61% | 28.87% |

CG

**Observations**

* In FR2, DL only evaluation, InH, CG30 and high load, it is identified from Source Nokia, QC that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (4/2/2, 8/4/4, 10/8/2, 10/5/5, 16/4/4, 16/8/8, 16/8/16) provides the mean power saving gain of 13.03% in the range of 3.79 ~ 22.66% with *marginal* loss in DL UE satisfied rate.
* The choice of a particular R15/16 CDRX configuration (cycle, on duration, and inactivity timer) greatly affects the PS gain.

Table 65 Source specific data: FR2, DL-only, InH, CG30, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| Nokia | 16 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 11 | 11 | 98.33% | 18.50% |
| Nokia | 17 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 11 | 11 | 98.00% | 15.40% |
| Nokia | 18 | R1-2111828 | R15/16CDRX | 16 | 8 | 8 | 0 | H | 11 | 11 | 78.10% | 11.60% |
| Nokia | 19 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 11 | 11 | 98.20% | 7.60% |
| Nokia | 20 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 11 | 11 | 96.00% | 13.70% |
| QC | 66 | R1-2112244 | ALWAYS ON | None | None | None | 0 | H | 7 | 7 | 90.00% | 0.00% |
| QC | 67 | R1-2112244 | CDRX | 16 | 4 | 4 | 0 | H | 7 | 7 | 80.00% | 22.66% |
| QC | 68 | R1-2112244 | CDRX | 16 | 8 | 8 | 0 | H | 7 | 7 | 90.00% | 9.56% |
| QC | 69 | R1-2112244 | CDRX | 16 | 8 | 16 | 0 | H | 7 | 7 | 90.00% | 3.79% |

##### UL-only Evaluation

###### DU

Table 66 Summary of FR2, UL-only, power evaluation results for DU

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | UL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS gain (%), Note 1 | | source |
| Mean (%) | Range (%) |
| DU | VR/CG UL Pose | 0.2 | R15/16 CDRX | High | 38.90 | 35.29 ~ 42.51 | vivo |
| AR UL 1 stream (scene) | 10 | R15/16 CDRX | High | 7.68 | 6.18 ~ 9.18 | vivo |
| Low | 7.89 | 6.41 ~ 9.36 | vivo |
| R17 PDCCH skipping | High | 46.21 | 46.21 ~ 51.42 | vivo |
| Low | 51.43 |  |  |
| Note 1 : PSG was computed for the cases only with marginal loss in % of UL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | | |

VR/CG

**Observations**

* In FR2, UL only evaluation, DU, VR/CG pose only and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (4/2/1,8/3/1) provides the mean power saving gain of 38.90% in the range of 35.29 ~ 42.51% with *marginal*[[5]](#footnote-5) loss in UL UE satisfied rate.

Table 67 Source specific data: FR2, UL-only, DU, VR/CG Pose only, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 187 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 20 | 20 | 96.51% | - |
| vivo | 188 | R1-2111046 | R15/16CDRX | 4 | 2 | 1 | 0 | H | 20 | 20 | 94.13% | 35.29% |
| vivo | 189 | R1-2111046 | R15/16CDRX | 8 | 3 | 1 | 0 | H | 20 | 20 | 92.30% | 42.51% |

No results available for FR2, UL-only, DU, VR/CG Pose only, low load

AR with UL 1 stream

**Observations**

* In FR2, UL only evaluation, DU, AR UL 1 stream, and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 7.68% in the range of 6.18 ~ 9.18% with *marginal* loss in UL UE satisfied rate.
* In FR2, UL only evaluation, DU, AR UL 1 stream and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 46.21% with *marginal* loss in UL UE satisfied rate.

Table 68 Source specific data: FR2, UL-only, DU, AR UL 1 stream, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 195 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 8 | 8 | 92.66% | - |
| vivo | 196 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 8 | 8 | 91.07% | 9.18% |
| vivo | 197 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 8 | 8 | 91.67% | 6.18% |
| vivo | 199 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 8 | 8 | 91.27% | 46.21% |

**Observations**

* In FR2, UL only evaluation, DU, AR UL 1 stream, and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/1) provides the mean power saving gain of 7.89% in the range of 6.41 ~ 9.36% with *marginal* loss in UL UE satisfied rate.
* In FR2, UL only evaluation, DU, AR UL 1 stream, and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 51.43% with marginal loss in DL UE satisfied rate.

Table 69 Source specific data: FR2, UL-only, DU, AR UL 1 stream, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 190 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 4 | 8 | 100.00% | - |
| vivo | 191 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 4 | 8 | 99.60% | 9.36% |
| vivo | 192 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 4 | 8 | 100.00% | 6.41% |
| vivo | 194 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 4 | 8 | 100.00% | 51.43% |

No results available for FR2, UL-only, DU, AR 2 streams.

###### InH

Table 70 Summary of FR2, UL-only power evaluation results for InH

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | UL Bit rate (Mbps) | PS scheme, Note 2 | System Load | PS gain (%), Note 1 | | source |
| Mean (%) | Range (%) |
| InH | VR/CG UL Pose | 0.2 | R15/16 CDRX | High | 40.53 | 35.99 ~ 45.07 | vivo |
| AR UL 1 stream (scene) | 10 | R15/16 CDRX | High | 8.16 | 6.58 ~ 9.74 | vivo |
| Low | 8.60 | 6.96 ~10.24 | vivo |
| R17 PDCCH skipping | High | 51.32 |  | vivo |
| Low | 52.35 |  | vivo |
| Note 1 : PSG was computed for the cases only with marginal loss in % of UL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | | |

VR/CG

**Observations**

* In FR2, UL only evaluation, InH, VR/CG pose only, and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (4/2/1, 8/3/1) provides the mean power saving gain of 40.53% in the range of 35.99 ~ 45.07% with *marginal* loss in UL UE satisfied rate.

Table 71 Source specific data: FR2, UL-only, InH, VR/CG Pose only, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 174 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 20 | 20 | 97.69% | - |
| vivo | 175 | R1-2111046 | R15/16CDRX | 4 | 2 | 1 | 0 | H | 20 | 20 | 95.90% | 35.99% |
| vivo | 176 | R1-2111046 | R15/16CDRX | 8 | 3 | 1 | 0 | H | 20 | 20 | 92.82% | 45.07% |

No results available for FR2, UL-only, DU, VR/CG Pose only, low load case

AR with UL 1 stream

**Observations**

* In FR2, UL only evaluation, InH, AR UL 1 stream, and high load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 8.16% in the range of 6.58 ~ 9.74% with *marginal* loss in UL UE satisfied rate.
* In FR2, UL only evaluation, InH, AR UL 1 stream, and high load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 46.21% with *marginal* loss in UL UE satisfied rate.

Table 72 Source specific data: FR2, UL-only, InH, AR 1 Stream, high load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 182 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | H | 8 | 8 | 95.14% | - |
| vivo | 183 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 8 | 8 | 92.71% | 9.74% |
| vivo | 184 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 8 | 8 | 94.10% | 6.58% |
| vivo | 186 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | H | 8 | 8 | 93.06% | 51.32% |

**Observations**

* In FR2, UL only evaluation, InH, AR UL 1 stream, and low load, it is identified from Source vivo that the R15/16CDRX scheme with configurations of (cycle/ODT/IAT) = (10/8/4, 16/14/4) provides the mean power saving gain of 8.60% in the range of 6.96 ~ 10.24% with *marginal* loss in UL UE satisfied rate.
* In FR2, UL only evaluation, InH, AR UL 1 stream, and low load, it is identified from Source vivo that the R17 PDCCH skipping scheme provides the mean power saving gain of 52.35% with *marginal* loss in UL UE satisfied rate.

Table 73 Source specific data: FR2, UL-only, InH, AR 1 Stream, low load

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 177 | R1-2111046 | AlwaysOn - baseline | 0 | 0 | 0 | 0 | L | 4 | 8 | 100.00% | - |
| vivo | 178 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | L | 4 | 8 | 100.00% | 10.24% |
| vivo | 179 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | L | 4 | 8 | 100.00% | 6.96% |
| vivo | 181 | R1-2111046 | R17 PDCCH skipping | 0 | 0 | 0 | 0 | L | 4 | 8 | 100.00% | 52.35% |

### Performance Comparison for Parameters/Modelling

#### Trade-off between Capacity and Power

This section captures the CDRX performance evaluation results showing the trade-off between capacity (% of satisfied UE) and power consumption.

**Observations**

* It is observed from the Source Intel, Nokia, vivo, HW, Ericsson, InterDigital that there is trade-off relation between % of satisfied UE (or capacity) and power saving gain, that is, in general, high power saving gain can be achieved with the lower % of satisfied UE for CDRX schemes.

Table 74 Source specific data, FR1, DL, DU, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | Mean PSG of all Ues (%) | % of DL satisfied UE |
| Intel | 3 | R1-2111521 | R15/16CDRX | 8 | 6 | 6 | 0 | H | 4 | 5 | 10.80% | 94.00% |
| Nokia | 39 | R1-2111828 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 6 | 6 | 9.20% | 93.00% |
| vivo | 43 | R1-2111046 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 13 | 13 | 3.03% | 91.58% |
| Huawei | 5 | R1-2110811 | R15/16CDRX | 16 | 14 | 4 | 0 | H | 5 | 5 | 3.46% | 90.67% |
| vivo | 42 | R1-2111046 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 13 | 13 | 4.70% | 90.11% |
| Interdigital | 25 | R1-2111830 | R15/16CDRX | 10 | 8 | 2 | 0 | H | 3 | 3 | 7.22% | 88.33% |
| Huawei | 3 | R1-2110811 | R15/16CDRX | 10 | 8 | 4 | 0 | H | 5 | 5 | 5.53% | 88.29% |
| Ericsson | 16 | R1-2112160 | R15/16CDRX | 10 | 8 | 3 | 0 | H | 4 | 4 | 4.00% | 84.00% |
| Nokia | 36 | R1-2111828 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 6 | 6 | 21.00% | 83.00% |
| Intel | 4 | R1-2111521 | R15/16CDRX | 8 | 4 | 6 | 0 | H | 4 | 5 | 15.70% | 82.75% |
| Interdigital | 23 | R1-2111830 | R15/16CDRX | 4 | 2 | 2 | 0 | H | 3 | 3 | 16.76% | 76.00% |
| Interdigital | 22 | R1-2111830 | R15/16CDRX | 16 | 12 | 4 | 0 | H | 3 | 3 | 6.93% | 75.00% |
| Huawei | 2 | R1-2110811 | R15/16CDRX | 10 | 5 | 4 | 0 | H | 5 | 5 | 14.68% | 61.05% |
| Nokia | 37 | R1-2111828 | R15/16CDRX | 8 | 4 | 4 | 0 | H | 6 | 6 | 18.00% | 61.00% |
| Nokia | 40 | R1-2111828 | R15/16CDRX | 10 | 5 | 5 | 0 | H | 6 | 6 | 17.00% | 52.00% |

#### Performance Comparison for Different DL Frame Generation Rates

In this section, we capture the data points showing the relation between DL frame generation rates and UE power consumption.

**Observations**

* Increasing application frame generation rate increases UE power consumption.
* In FR1, DL+UL evaluation, DU, AlwaysOn, it was identified from source QC that VR 30Mbps with 120fps increases power consumption by 6.45% w.r.t. 60fps case.

Table 75 Source specific data: FR1, DL+UL eval, DU, VR 30Mbps for different DL frame generation rates

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data point index | Tdoc source | Power saving scheme | Fps | Load H/L | N1 | C1 | % of DL+UL satisfied UE | Mean PSG of all UEs (%) |
| QC | 5 | R1-2110216 | AlwaysOn - baseline | 60 | H | 11 | 11 | 95.33% | 0.00% |
| QC | 130 | R1-2110216 | AlwaysOn - baseline | 120 | H | 11 | 11 | 98.87% | -6.45% |

#### Performance Comparison for Different Data Rates

In this section, we capture the evaluation results showing the relation between data rates and UE power consumption.

**Observations**

* Increasing application data(bit) rate increases UE power consumption.
* In FR1, DL+UL evaluation, DU, AlwaysOn, it was identified from Source QC that VR DL bit rate of 45Mbps and 60 Mbps increases power consumption by 2.14 and 4.21% compared to VR DL 30Mbps case.

Table 76 Source specific data: FR1, DL+UL, DU, VR 30Mbps for different data rates

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | DL bit rates | Additional Assumptions | Load H/L | N1 | C1 | % of DL+UL satisfied UE | PSG (%) |
| QC | 131 | R1-2110216 | AlwaysOn | 30Mbps |  | L | 1 | 11 | 100% | 0.00% |
| QC | 132 | R1-2110216 | AlwaysOn | 45Mbps |  | L | 1 | 11 | 98.09% | -2.14% |
| QC | 133 | R1-2110216 | AlwaysOn | 60Mbps |  | L | 1 | 11 | 95.71% | -4.21% |

#### Performance Comparison for Different Pose Periodicity

In this section, the impact of different pose periodicities on power consumption is evaluated.

Table 77 Summary of power performance for different periodicity.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | UL Bit rate (Mbps) | UL pose periodicity | PS scheme, Note 2 | PS gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| DU | VR/CG UL Pose | 0.2 | 4ms | AlwaysOn | 0 |  | QC |
| 0.1 | 8ms | AlwaysOn | 2.27 |  | QC |
| 0.048 | 16.67ms | AlwaysOn | 10.83 |  | QC |
| Note 1 : PSG was computed for the cases only with marginal loss in % of UL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered R15/16 CDRX configurations in this table are listed in the following tables. | | | | | | | |

**Observations**

* Reducing pose periodicity could decrease power consumption.
* In FR1, DL+UL evaluation, DU, Pose only, AlwaysOn, it was identified from Source QC the pose tx with periodicity of 8ms (or 125Hz) has power saving gain of 2.27% w.r.t AlwaysOn with periodicity of 4ms.
* In FR1, DL+UL evaluation, DU, Pose only, AlwaysOn, it was identified from Source QC the pose tx with periodicity of 16.67ms (or 60Hz) has power saving gain of 10.83% w.r.t AlwaysOn with periodicity of 4ms.

Table 78 Source specific data: FR1, DU, DL+UL, VR30, UL pose (periodicity = 4ms)

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | Pose Periodicity | Load H/L | N1 | C1 | % of DL+UL satisfied UE | Mean PSG of all UEs (%) |
| QC | 5 | R1-2110216 | AlwaysOn | 4ms | H | 11 | 11 | 95.49% | 0.00% |
| QC | 134 | R1-2110216 | AlwaysOn | 8ms | H | 11 | 11 | 95.15% | 2.27% |
| QC | 135 | R1-2110216 | AlwaysOn | 16.67ms | H | 11 | 11 | 95.75% | 10.83% |

### Potential Enhancements

#### Enhanced CDRX

In this section, we provide performance evaluation results of eCDRX where eCDRX is a set of enhanced CDRX mechanisms which solves that the mismatch between XR DL traffic arrival timing and CDRX On duration start time. This mismatch occurs because of that typical XR DL traffic periodicity (which is the inverse of frame generation rate) is non-integer multiples of 1ms (e.g., 16.67ms, 8.33ms, etc) whereas current R15/16/17 CDRX periodicities are defined in the unit of 1ms. The mismatch could be resolved by adjusting DRX On duration start time offset to be aligned with each DL traffic arrival time, or configure a CDRX cycle pattern with different cycle values instead of only one CDRX cycle, etc.

##### FR1

###### DL+UL joint evaluation

Table 79 Summary of FR1, DL+UL power evaluation results for eCDRX

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | PS Gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| DU | VR | 30 | eCDRX | 11.64 | 4.51 ~ 23.49 | Vivo, Ericsson, QC |
| CG | 30 | eCDRX | 6 |  | Ericsson |
| AR (UL 1/2 streams) | 30 | eCDRX | 11.06 | 4.6 ~ 20.77 | vivo |
| InH | VR | 30 | eCDRX | 17.63 | 7.23 ~ 25.12 | ZTE, vivo |
| 45 | eCDRX | 25.64 | 25.63 ~ 25.65 | ZTE |
| CG | 30 | eCDRX | 18.25 | 18.23 ~ 18.26 | ZTE |
| AR (UL 1/2 streams) | 30 | eCDRX | 12.23 | 4.82 ~ 23.61% | vivo |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL+UL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered eCDRX configurations in this table are listed in the following tables. Note 3: For comparison with R15/16 CDRX results, see sections 9.3.1 including baseline performance evaluation results. | | | | | | |

DU

**Observations**

* In FR1, DL+UL evaluation, DU, VR30, it was identified from source vivo, Ericsson, QC that the enhanced CDRX scheme provides the mean power saving gain of 11.64% in the range of 4.51 ~ 23.49% with *marginal* loss in DL+UL UE satisfied rate.

Table 80 Source specific data: eCDRX, FR1, DL+UL, DU, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 239 | R1-2111046 | Note 1 | 16 | 10 | 4 | 0 | L | 7 | 13 |  |  | 100.00% | 9.09% |
| vivo | 240 | R1-2111046 | Note 2 | 16 | 6 | 4 | 0 | L | 7 | 13 |  |  | 100.00% | 23.49% |
| vivo | 247 | R1-2111046 | Note 1 | 16 | 10 | 4 | 0 | H | 13 | 13 |  |  | 92.06% | 7.05% |
| vivo | 248 | R1-2111046 | Noe 2 | 16 | 6 | 4 | 0 | H | 13 | 13 |  |  | 91.21% | 21.93% |
| Ericsson | 13 | R1-2112160 | eCDRX | 16.6666 | 13 | 0 | 0 | H | 4 | 4 |  |  | 85.00% | 6.00% |
| QC | 56 | R1-2110402 | eCDRX | 16/17/17 | 10 | 10 | 0 | H | 11 | 11 | 97.66% | 84.85% | 82.86% | 9.43% |
| QC | 57 | R1-2110402 | eCDRX | 16/17/17 | 12 | 12 | 0 | H | 11 | 11 | 97.58% | 96.62% | 94.20% | 4.51% |
| Note 1. e-CDRX adapting to the lower boundary of jitter  Note 2. e-CDRX adapting to quasi (ideal)-period position | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, DU, CG30, it was identified from source Ericsson that the enhanced CDRX scheme provides the mean power saving gain of 6.0% with *marginal* loss in DL+UL UE satisfied rate.

Table 81 Source specific data: eCDRX, FR1, DL+UL, DU, CG30

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT  (ms) | Additional Assumptions | Load: H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL+UL satisfied UE | Mean PSG of all UEs (%) |
| Ericsson | 4 | R1-2112160 | eCDRX | 16.6666 | 13 | 0 |  | H | 4 | 4 |  |  | 87.00% | 6.00% |

**Observations**

* In FR1, DL+UL evaluation, DU, AR30, it was identified from source vivo that the enhanced CDRX scheme provides the mean power saving gain of 11.06% in the rage of 4.60 ~ 20.77% with *marginal* loss in DL+UL UE satisfied rate.

Table 82 Source specific data: eCDRX, FR1, DL+UL, DU, AR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 271 | R1-2111046 | Note 3 | 16 | 10 | 4 | Note 1 | L | 5 | 9 |  |  | 96.19% | 9.60% |
| vivo | 272 | R1-2111046 | Note 4 | 16 | 6 | 4 | Note 1 | L | 5 | 9 |  |  | 95.87% | 20.77% |
| vivo | 279 | R1-2111046 | Note 3 | 16 | 10 | 4 | Note 1 | H | 9 | 9 |  |  | 92.06% | 6.66% |
| vivo | 280 | R1-2111046 | Note 4 | 16 | 6 | 4 | Note 1 | H | 9 | 9 |  |  | 90.83% | 14.04% |
| vivo | 303 | R1-2111046 | Note 3 | 16 | 10 | 4 | Note 2 | L | 4 | 7 |  |  | 100.00% | 5.28% |
| vivo | 304 | R1-2111046 | Note 4 | 16 | 6 | 4 | Note 2 | L | 4 | 7 |  |  | 100.00% | 14.34% |
| vivo | 311 | R1-2111046 | Note 3 | 16 | 10 | 4 | Note 2 | H | 7 | 7 |  |  | 91.38% | 4.60% |
| vivo | 312 | R1-2111046 | Note 4 | 16 | 6 | 4 | Note 2 | H | 7 | 7 |  |  | 90.48% | 13.19% |
| Note 1 AR with single UL stream.  Note 2 AR with two UL streams.  Note 3 e-CDRX adapting to the lower boundary of jitter  Note 4 e-CDRX adapting to quasi (ideal)-period position | | | | | | | | | | | | | | |

InH

**Observations**

* In FR1, DL+UL evaluation, InH, VR30, it was identified from ZTE, vivo that the enhanced CDRX scheme provides the mean power saving gain of 17.63% in the range of 7.23 ~ 25.12% with *marginal* loss in DL+UL UE satisfied rate.

Table 83 Source specific data: eCDRX, FR1, DL+UL, InH, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 223 | R1-2111046 | Note 5 | 16 | 10 | 4 | 0 | L | 5 | 10 |  |  | 100.00% | 9.38% |
| vivo | 224 | R1-2111046 | Note 6 | 16 | 6 | 4 | 0 | L | 5 | 10 |  |  | 100.00% | 25.12% |
| vivo | 231 | R1-2111046 | Note 5 | 16 | 10 | 4 | 0 | H | 10 | 10 |  |  | 92.06% | 7.23% |
| vivo | 232 | R1-2111046 | Note 6 | 16 | 6 | 4 | 0 | H | 10 | 10 |  |  | 90.70% | 23.56% |
| ZTE, Sanechips | 7 | R1-2111351 | Note 4 | 16 | 8 | 4 | Note 1,2 | H | 11 | 11 | 86.36% | 100.00% | 86.36% | 20.24% |
| ZTE, Sanechips | 8 | R1-2111351 | Note 4 | 16 | 8 | 4 | Note 1,3 | H | 11 | 11 | 86.36% | 100.00% | 86.36% | 20.22% |
| Note 1. DL and UL were simulated separately and collected traces are combined as a single timeline for DL+UL joint power evaluation.  Note 2. Option 2(Linear interpolation in linear domain) for UL power model  Note 3. Option 1(two-step Qauntization) for UL power model  Note 4. eCDRX(change drx-startoffset per 100ms)  Note 5. e-CDRX adapting to the lower boundary of jitter  Note 6. e-CDRX adapting to quasi (ideal)-period position | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, InH, VR45, it was identified that Source ZTE that the enhanced CDRX scheme provides the mean power saving gain of 25.64% in the range of 25.63 ~ 25.65% with *marginal* loss in DL+UL UE satisfied rate.

Table 84 Source specific data: eCDRX, FR1, DL+UL, InH, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| ZTE, Sanechips | 15 | R1-2111351 | Note 4 | 16 | 8 | 4 | Note 1,2 | H | 7 | 7 | 80.00% | 100.00% | 80.00% | 25.65% |
| ZTE, Sanechips | 16 | R1-2111351 | Note 4 | 16 | 8 | 4 | Note 1,3 | H | 7 | 7 | 80.00% | 100.00% | 80.00% | 25.63% |
| Note 1. DL and UL were simulated separately and collected traces are combined as a single timeline for DL+UL joint power evaluation.  Note 2. Option 2(Linear interpolation in linear domain) for UL power model  Note 3. Option 1(two-step Qauntization) for UL power model  Note 4. eCDRX(change drx-startoffset per 100ms) | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, InH, CG30, it was identified from ZTE that the enhanced CDRX scheme provides the mean power saving gain of 18.25% in the range of 18.23 ~ 18.26% with *marginal* loss in DL+UL UE satisfied rate.

Table 85 Source specific data: eCDRX, FR1, DL+UL, InH, CG30

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| ZTE, Sanechips | 23 | R1-2111351 | Note 4 | 16 | 8 | 4 | Note 1,2 | H | 12 | 12 | 85.40% | 100.00% | 85.40% | 18.26% |
| ZTE, Sanechips | 24 | R1-2111351 | Note 4 | 16 | 8 | 4 | Note 1,3 | H | 12 | 12 | 85.40% | 100.00% | 85.40% | 18.23% |
| Note 1. DL and UL were simulated separately and merged for DL+UL joint power evaluation.  Note 2. Option 2(Linear interpolation in linear domain) for UL power model  Note 3. Option 1(two-step Qauntization) for UL power model  Note 4. eCDRX(change drx-startoffset per 100ms) | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, InH, AR30, it was identified from vivo that the enhanced CDRX scheme provides the mean power saving gain of 12.23% in the range of 4.82 ~ 23.61% with *marginal* loss in DL+UL UE satisfied rate.

Table 86 Source specific data: eCDRX, FR1, DL+UL, InH, AR30 (1 & 2 streams)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 255 | R1-2111046 | Note 1 | 16 | 10 | 4 | Note 3 | L | 5 | 10 |  |  | 100.00% | 10.76% |
| vivo | 256 | R1-2111046 | Note 2 | 16 | 6 | 4 | Note 3 | L | 5 | 10 |  |  | 100.00% | 23.61% |
| vivo | 263 | R1-2111046 | Note 1 | 16 | 10 | 4 | Note 3 | H | 10 | 10 |  |  | 91.90% | 6.95% |
| vivo | 264 | R1-2111046 | Note 2 | 16 | 6 | 4 | Note 3 | H | 10 | 10 |  |  | 90.83% | 14.77% |
| vivo | 287 | R1-2111046 | Note 1 | 16 | 10 | 4 | Note 4 | L | 5 | 10 |  |  | 100.00% | 6.29% |
| vivo | 288 | R1-2111046 | Note 2 | 16 | 6 | 4 | Note 4 | L | 5 | 10 |  |  | 100.00% | 16.65% |
| vivo | 295 | R1-2111046 | Note 1 | 16 | 10 | 4 | Note 4 | H | 10 | 10 |  |  | 91.59% | 4.82% |
| vivo | 296 | R1-2111046 | Note 2 | 16 | 6 | 4 | Note 4 | H | 10 | 10 |  |  | 90.56% | 13.96% |
| Note 1. e-CDRX adapting to the lower boundary of jitter  Note 2. e-CDRX adapting to quasi (ideal)-period position  Note 3. AR UL 1 stream  Note 4. AR UL 2 streams | | | | | | | | | | | | | | |

UMa

No results available for UMa

###### DL-only Evaluation

Table 87 Summary of FR1, DL-only power evaluation results for eCDRX

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | PS Gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| DU | VR | 30 | eCDRX | 15.70 | 5.76 ~ 34.95 | HW, Vivo, Ericsson, QC |
| 45 | eCDRX | 18.14 | 9.72 ~ 27.26 | vivo |
| InH | VR | 30 | eCDRX | 20.812 | 9.36 ~ 29.43 | ZTE, vivo |
| 45 | eCDRX | 19.96 | 9.42 ~ 29.1 | ZTE, vivo |
| CG | 30 | eCDRX | 26.38 | 26.38 | ZTE |
| UMa | VR | 30 | eCDRX | 18.88 | 10.05 ~ 29.06 | vivo |
| 45 | eCDRX | 18.22 | 9.86 ~ 27.33 | vivo |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered eCDRX configurations in this table are listed in the following tables. Note 3: For comparison with R15/16 CDRX results, see section 9.3.1 including baseline performance evaluation results. | | | | | | |

DU

**Observations**

* In FR1, DL only evaluation, DU, VR30, it was identified from Source Huawei, vivo, Ericsson, QC that the enhanced CDRX scheme provides the mean power saving gain of 15.70% in the range of 5.76 ~ 34.95% with *marginal* loss in DL UE satisfied rate.

Table 88 Source specific data: eCDRX, FR1, DL-only, DU, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| Huawei | 6 | R1-2110811 | eCDRX | 17/17/16 | 8 | 4 | OnDurationStartOffset=-3ms | H | 5 | 5 | 80.29% | 17.84% |
| Huawei | 7 | R1-2110811 | eCDRX | 17/17/16 | 8 | 4 | OnDurationStartOffset=-2ms | H | 5 | 5 | 86.10% | 19.29% |
| Huawei | 8 | R1-2110811 | eCDRX | 17/17/16 | 10 | 4 | OnDurationStartOffset=-4ms | H | 5 | 5 | 86.86% | 13.00% |
| Huawei | 9 | R1-2110811 | eCDRX | 17/17/16 | 8 | 8 | OnDurationStartOffset=-3ms | H | 5 | 5 | 85.43% | 7.93% |
| Huawei | 10 | R1-2110811 | eCDRX | 17/17/16 | 8 | 8 | OnDurationStartOffset=-2ms | H | 5 | 5 | 90.95% | 9.77% |
| Huawei | 11 | R1-2110811 | eCDRX | 17/17/16 | 10 | 8 | OnDurationStartOffset=-4ms | H | 5 | 5 | 91.62% | 5.76% |
| Huawei | 21 | R1-2110811 | eCDRX | 17/17/16 | 8 | 4 | OnDurationStartOffset=-3ms | L | 3 | 5 | 93.65% | 18.65% |
| Huawei | 22 | R1-2110811 | eCDRX | 17/17/16 | 8 | 4 | OnDurationStartOffset=-2ms | L | 3 | 5 | 96.51% | 20.17% |
| Huawei | 23 | R1-2110811 | eCDRX | 17/17/16 | 10 | 4 | OnDurationStartOffset=-4ms | L | 3 | 5 | 97.62% | 13.63% |
| Huawei | 24 | R1-2110811 | eCDRX | 17/17/16 | 8 | 8 | OnDurationStartOffset=-3ms | L | 3 | 5 | 95.40% | 8.46% |
| Huawei | 25 | R1-2110811 | eCDRX | 17/17/16 | 8 | 8 | OnDurationStartOffset=-2ms | L | 3 | 5 | 98.10% | 10.52% |
| Huawei | 26 | R1-2110811 | eCDRX | 17/17/16 | 10 | 8 | OnDurationStartOffset=-4ms | L | 3 | 5 | 98.41% | 6.26% |
| vivo | 36 | R1-2111046 | Note 1 | 16 | 10 | 4 | 0 | L | 7 | 13 | 100.00% | 12.49% |
| vivo | 37 | R1-2111046 | Note 2 | 16 | 6 | 4 | 0 | L | 7 | 13 | 100.00% | 27.49% |
| vivo | 44 | R1-2111046 | Note 1 | 16 | 10 | 4 | 0 | H | 13 | 13 | 91.70% | 8.67% |
| vivo | 45 | R1-2111046 | Note 2 | 16 | 6 | 4 | 0 | H | 13 | 13 | 91.21% | 21.72% |
| Ericsson | 18 | R1-2112160 | eCDRX | 16.6666 | 8 | 3 | 0 | H | 4 | 4 | 84.00% | 22.00% |
| QC | 61 | R1-2110402 | eCDRX | 16/17/17 | 4 | 6 | 0 | H | 11 | 11 | 95.76% | 34.95% |
| QC | 62 | R1-2110402 | eCDRX | 16/17/17 | 6 | 6 | 0 | H | 11 | 11 | 96.45% | 28.01% |
| QC | 63 | R1-2110402 | eCDRX | 16/17/17 | 8 | 8 | 0 | H | 11 | 11 | 96.79% | 19.98% |
| QC | 64 | R1-2110402 | eCDRX | 16/17/17 | 10 | 10 | 0 | H | 11 | 11 | 96.19% | 12.19% |
| QC | 65 | R1-2110402 | eCDRX | 16/17/17 | 12 | 12 | 0 | H | 11 | 11 | 96.80% | 6.66% |
| Note 1. e-CDRX adapting to the lower boundary of jitter  Note 2. e-CDRX adapting to quasi (ideal)-period position | | | | | | | | | | | | |

**Observations**

* In FR1, DL only evaluation, DU, VR45, it was identified from Source vivo that the enhanced CDRX scheme provides the mean power saving gain of 18.14% in the range of 9.72 ~ 27.26% with *marginal* loss in DL UE satisfied rate.

Table 89 Source specific data: eCDRX, FR1, DL-only, DU, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 52 | R1-2111046 | Note 1 | 16 | 10 | 4 | 0 | L | 3 | 6 | 98.94% | 12.61% |
| vivo | 53 | R1-2111046 | Note 2 | 16 | 6 | 4 | 0 | L | 3 | 6 | 99.47% | 27.26% |
| vivo | 60 | R1-2111046 | Note 1 | 16 | 10 | 4 | 0 | H | 6 | 6 | 95.63% | 9.72% |
| vivo | 61 | R1-2111046 | Note 2 | 16 | 6 | 4 | 0 | H | 6 | 6 | 94.18% | 22.95% |
| Note 1. e-CDRX adapting to the lower boundary of jitter  Note 2. e-CDRX adapting to quasi (ideal)-period position | | | | | | | | | | | | |

InH

**Observations**

* In FR1, DL only evaluation, InH, VR30, it was identified from Source vivo, ZTE that the enhanced CDRX scheme provides the mean power saving gain of 20.81% in the range of 9.36 ~ 29.43% with *marginal* loss in DL UE satisfied rate.

Table 90 Source specific data: eCDRX, FR1, DL-only, InH, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | | Load H/L | | N1 | C1 | % of DL satisfied UE | | Mean PSG of all Ues (%) |
| vivo | 4 | R1-2111046 | Note 1 | 16 | 10 | 4 | 0 | | L | | 5 | 10 | 100.00% | | 13.05% |
| vivo | 5 | R1-2111046 | Note 2 | 16 | 6 | 4 | 0 | | L | | 5 | 10 | 100.00% | | 28.38% |
| vivo | 12 | R1-2111046 | Note 1 | 16 | 10 | 4 | 0 | | H | | 10 | 10 | 91.94% | | 9.36% |
| vivo | 13 | R1-2111046 | Note 2 | 16 | 6 | 4 | 0 | | H | | 10 | 10 | 91.25% | | 23.84% |
| ZTE, Sanechips | 30 | R1-2111351 | Note 3 | 16 | 8 | 4 | 0 | H | 11 | 11 | | 86.36% | | 29.43% | |
| Note 1. e-CDRX adapting to the lower boundary of jitter  Note 2. e-CDRX adapting to quasi (ideal)-period position  Note 3. eCDRX(change drx-startoffset per 100ms) | | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL only evaluation, InH, VR45, it was identified from Source vivo, ZTE that the enhanced CDRX scheme provides the mean power saving gain of 19.96% in the range of 9.42 ~ 29.1% with *marginal* loss in DL UE satisfied rate.

Table 91 Source specific data: eCDRX, FR1, DL-only, InH, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 20 | R1-2111046 | Note 1 | 16 | 10 | 4 | 0 | L | 3 | 5 | 100.00% | 11.96% |
| vivo | 21 | R1-2111046 | Note 2 | 16 | 6 | 4 | 0 | L | 3 | 5 | 100.00% | 26.74% |
| vivo | 28 | R1-2111046 | Note 1 | 16 | 10 | 4 | 0 | H | 5 | 5 | 96.67% | 9.42% |
| vivo | 29 | R1-2111046 | Note 3 | 16 | 6 | 4 | 0 | H | 5 | 5 | 93.89% | 22.61% |
| ZTE, Sanechips | 34 | R1-2111351 | eCDRX(change drx-startoffset per 100ms) | 16 | 8 | 4 | 0 | H | 7 | 7 | 80% | 29.1% |
| Note 1. e-CDRX adapting to the lower boundary of jitter  Note 2. e-CDRX adapting to quasi (ideal) - period position  Note 3. e-CDRX adapting to quasi (ideal) - period position | | | | | | | | | | | | |

**Observations**

* In FR1, DL only evaluation, InH, CG30, it was identified from Source ZTE that the enhanced CDRX scheme provides the mean power saving gain of 26.38% with *marginal* loss in DL UE satisfied rate.

Table 92 Source specific data: eCDRX, FR1, DL-only, InH, CG30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| ZTE, Sanechips | 38 | R1-2111351 | eCDRX(change  drx-startoffset  per 100ms) | 16 | 8 | 4 | 0 | H | 12 | 12 | 85.40% | 26.38% |

UMa

**Observations**

* In FR1, DL only evaluation, UMa, VR30, it was identified from Source vivo that the enhanced CDRX scheme provides the mean power saving gain of 18.88% in the range of 10.05 ~ 29.06 % with *marginal* loss in DL UE satisfied rate.

Table 93 Source specific data: eCDRX, FR1, DL-only, UMa, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 68 | R1-2111046 | e-CDRX adapting to the lower boundary of jitter | 16 | 10 | 4 | 0 | L | 4 | 8 | 98.81% | 13.09% |
| vivo | 69 | R1-2111046 | e-CDRX adapting to quasi (ideal)-period position | 16 | 6 | 4 | 0 | L | 4 | 8 | 97.22% | 29.06% |
| vivo | 76 | R1-2111046 | e-CDRX adapting to the lower boundary of jitter | 16 | 10 | 4 | 0 | H | 8 | 8 | 93.35% | 10.05% |
| vivo | 77 | R1-2111046 | e-CDRX adapting to quasi (ideal)-period position | 16 | 6 | 4 | 0 | H | 8 | 8 | 91.87% | 23.33% |

**Observations**

* In FR1, DL only evaluation, UMa, VR45, it was identified from Source vivo that the enhanced CDRX scheme provides the mean power saving gain of 18.22% in the range of 9.86 ~ 27.33% with *marginal* loss in DL UE satisfied rate.

Table 94 Source specific data: eCDRX, FR1, DL-only, UMa, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 84 | R1-2111046 | e-CDRX adapting to the lower boundary of jitter | 16 | 10 | 4 | 0 | L | 2 | 4 | 96.83% | 12.09% |
| vivo | 85 | R1-2111046 | e-CDRX adapting to quasi (ideal)-period position | 16 | 6 | 4 | 0 | L | 2 | 4 | 96.83% | 27.33% |
| vivo | 92 | R1-2111046 | e-CDRX adapting to the lower boundary of jitter | 16 | 10 | 4 | 0 | H | 4 | 4 | 94.05% | 9.86% |
| vivo | 93 | R1-2111046 | e-CDRX adapting to quasi (ideal)-period position | 16 | 6 | 4 | 0 | H | 4 | 4 | 91.67% | 23.59% |

###### UL-only Evaluation

Table 95 Summary of FR1, UL-only power evaluation results for eCDRX

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | PS Gain (%), Note 1 | | source |
| Mean (%) | Range (%) |
| DU | AR UL 1 / 2 streams | 10.2 | eCDRX | 25.56% | 19.89 ~ 32.02% | vivo |
| InH | AR UL 1 / 2 streams | 10.2 | eCDRX | 28.67% | 22.66 ~ 35.24% | vivo |
| Note 1 : PSG was computed for the cases only with marginal loss in % of UL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered eCDRX configurations in this table are listed in the following tables. Note 3: For comparison with R15/16 CDRX results, see section 9.3.1 including baseline performance evaluation results. | | | | | | |

DU

No results are available for FR1, UL-only, DU, VR/CG Pose only

**Observations**

* In FR1, UL only evaluation, DU, AR UL 1 & 2 streams, it was identified from Source vivo that the enhanced CDRX scheme provides the mean power saving gain of 25.56% in the range of 19.89 ~ 32.02% with *marginal* loss in UL UE satisfied rate.

Table 96 Source specific data: eCDRX, FR1, UL-only, DU, AR UL 1 & 2 stream

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 164 | R1-2111046 | Note 1 | 16 | 6 | 4 | AR UL 1 stream | L | 5 | 9 | 95.56% | 32.02% |
| vivo | 169 | R1-2111046 | Note 1 | 16 | 6 | 4 | AR UL 1 stream | H | 9 | 9 | 91.60% | 28.99% |
| vivo | 213 | R1-2111046 | Note 1 | 16 | 6 | 4 | AR UL 2 streams | L | 4 | 7 | 100.00% | 21.35% |
| vivo | 218 | R1-2111046 | Note 1 | 16 | 6 | 4 | AR UL 2 streams | H | 7 | 7 | 90.48% | 19.89% |
| Note 1. e-CDRX adapting to quasi (ideal)-period position | | | | | | | | | | | | |

InH

Note results available for FR1, UL-only, InH, VR/CG Pose only.

**Observations**

* In FR1, UL only evaluation, DU, AR UL 1 & 2 streams, it was identified from Source vivo that the enhanced CDRX scheme provides the mean power saving gain of 28.67% in the range of 23.66 ~ 35.24% with *marginal* loss in UL UE satisfied rate.

Table 97 Source specific data: eCDRX, FR1, UL-only, InH, AR UL 1 & 2 streams

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT  (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all UEs (%) |
| vivo | 151 | R1-2111046 | Note 1 | 16 | 6 | 4 | AR UL 1 stream | L | 7 | 13 | 100% | 35.24% |
| vivo | 156 | R1-2111046 | Note 1 | 16 | 6 | 4 | AR UL 1 stream | H | 13 | 13 | 92.38% | 33.64% |
| vivo | 203 | R1-2111046 | Note 1 | 16 | 6 | 4 | AR UL 2 stream | L | 6 | 12 | 100% | 23.66% |
| vivo | 208 | R1-2111046 | Note 1 | 16 | 6 | 4 | AR UL 2 stream | H | 12 | 12 | 91.90% | 22.17% |
| Note 1. e-CDRX adapting to quasi (ideal)-period position | | | | | | | | | | | | |

UMa

No results available for UMa

##### FR2

###### DL-only evaluation

Table 98 Summary of FR2, DL-only power evaluation results for eCDRX

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | PS Gain (%), Note 1 | | source |
| Mean (%) | Range (%) |
| DU | VR | 30 | eCDRX | 31.97% | 31.30 ~ 32.63% | vivo |
| 45 | eCDRX | 27.87% | 27.16 ~ 28.57% | vivo |
| InH | VR | 30 | eCDRX | 16.42% | 0.3 ~ 34.89% | Vivo, QC |
| 45 | eCDRX | 28.81% | 28.37 ~ 29.25% | vivo |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered eCDRX configurations in this table are listed in the following tables. Note 3: For comparison with R15/16 CDRX results, see section 9.3.1 including baseline performance evaluation results. | | | | | | |

DU

**Observations**

* In FR2, DL only evaluation, DU, VR30, it was identified from Source vivo that the enhanced CDRX scheme provides the mean power saving gain of 31.97% in the range of 31.30 ~ 32.63% with *marginal* loss in DL UE satisfied rate.

Table 99 Source specific data: eCDRX, FR2, DL-only, DU, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT  (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all UEs (%) |
| vivo | 124 | R1-2111046 | e-CDRX adapting to quasi (ideal)-period position | 16 | 8 | 4 |  | L | 7 | 13 | 99.09% | 32.63% |
| vivo | 130 | R1-2111046 | e-CDRX adapting to quasi (ideal)-period position | 16 | 8 | 4 |  | H | 13 | 13 | 91.97% | 31.30% |

**Observations**

* In FR2, DL only evaluation, DU, VR45, it was identified from Source vivo that the enhanced CDRX scheme provides the mean power saving gain of 27.87% in the range of 27.16 ~ 28.57% with *marginal* loss in DL UE satisfied rate.

Table 100 Source specific data: eCDRX, FR2, DL-only, DU, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT  (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all UEs (%) |
| vivo | 136 | R1-2111046 | e-CDRX adapting to quasi (ideal)-period position | 16 | 8 | 4 |  | L | 4 | 8 | 100.00% | 28.57% |
| vivo | 142 | R1-2111046 | e-CDRX adapting to quasi (ideal)-period position | 16 | 8 | 4 |  | H | 8 | 8 | 91.47% | 27.16% |

InH

**Observations**

* In FR2, DL only evaluation, InH, VR30, it was identified from Source vivo, QC that the enhanced CDRX scheme provides the mean power saving gain of 16.42% in the range of 0.3 ~ 34.89% with *marginal* loss in DL UE satisfied rate.

Table 101 Source specific data: eCDRX, FR2, DL-only, InH, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 100 | R1-2111046 | e-CDRX adapting to  quasi (ideal)- period position | 16 | 8 | 4 | 0 | L | 4 | 8 | 98.61% | 34.89% |
| vivo | 106 | R1-2111046 | e-CDRX adapting  to quasi (ideal)- period position | 16 | 8 | 4 | 0 | H | 8 | 8 | 90.97% | 33.68% |
| QC | 77 | R1-2112244 | eCDRX | 16/16/15 | 4 | 4 | 0 | H | 7 | 7 | 90.00% | 18.93% |
| QC | 78 | R1-2112244 | eCDRX | 16/16/15 | 8 | 8 | 0 | H | 7 | 7 | 90.00% | 7.71% |
| QC | 79 | R1-2112244 | eCDRX | 16/16/15 | 8 | 16 | 0 | H | 7 | 7 | 90.00% | 0.30% |
| QC | 81 | R1-2112244 | eCDRX | 16/16/15 | 4 | 4 | 0 | H | 7 | 7 | 27.00% | 25.10% |
| QC | 82 | R1-2112244 | eCDRX | 16/16/15 | 8 | 8 | 0 | H | 7 | 7 | 84.00% | 8.28% |
| QC | 83 | R1-2112244 | eCDRX | 16/16/15 | 8 | 16 | 0 | H | 7 | 7 | 88.00% | 2.43% |

**Observations**

* In FR2, DL only evaluation, InH, VR45, it was identified from Source vivo that the enhanced CDRX scheme provides the mean power saving gain of 28.81% in the range of 28.37 ~ 29.25% with *marginal* loss in DL UE satisfied rate.

Table 102 Source specific data: eCDRX, FR2, DL-only, InH, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT  (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all UEs (%) |
| vivo | 112 | R1-2112244 | e-CDRX adapting to quasi (ideal)- period position | 16 | 8 | 4 |  | L | 2 | 4 | 100.00% | 29.25% |
| vivo | 118 | R1-2112244 | e-CDRX adapting to quasi (ideal)- period position | 16 | 8 | 4 |  | H | 4 | 4 | 91.67% | 28.37% |

###### UL-only evaluation

Table 103 Summary of FR2, UL-only power evaluation results for eCDRX

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme, Note 2 | PS Gain (%), Note 1 | | source |
| Mean (%) | Range (%) |
| DU | AR UL 1 stream | 10 | eCDRX | 32.35 | 31.72 ~ 32.97 | vivo |
| InH | AR UL 1 stream | 10 | eCDRX | 37.57% | 36.79 ~ 38.35 | vivo |
| Note 1 : PSG was computed for the cases only with marginal loss in % of UL satisfied UE. Note 2: The CDRX configurations considered in each case could be different. The details of considered eCDRX configurations in this table are listed in the following tables. Note 3: For comparison with R15/16 CDRX results, see section 9.3.1 including baseline performance evaluation results. | | | | | | |

DU

**Observations**

* In FR2, UL only evaluation, DU, AR UL 1 stream, it was identified from Source vivo that the enhanced CDRX scheme provides the mean power saving gain of 32.35% in the range of 31.72 ~ 32.97% with *marginal* loss in UL UE satisfied rate.

Table 104 Source specific data: eCDRX, FR2, UL-only, DU, AR UL 1 stream

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT  (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all UEs (%) |
| vivo | 193 | R1-2111046 | e-CDRX adapting to quasi (ideal)- period position | 16 | 8 | 4 |  | L | 4 | 8 | 99.60% | 32.97% |
| vivo | 198 | R1-2111046 | e-CDRX adapting to quasi (ideal)- period position | 16 | 8 | 4 |  | H | 8 | 8 | 90.67% | 31.72% |

InH

**Observations**

* In FR2, UL only evaluation, InH, AR UL 1 stream, it was identified from Source vivo that the enhanced CDRX scheme provides the mean power saving gain of 37.57% in the range of 36.79 ~ 38.35% with *marginal* loss in UL UE satisfied rate.

Table 105 Source specific data: eCDRX, FR2, UL-only, InH, AR UL 1 stream

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 180 | R1-2111046 | e-CDRX adapting  to quasi (ideal)- period position | 16 | 8 | 4 | 0 | L | 4 | 8 | 100.00% | 38.35% |
| vivo | 185 | R1-2111046 | e-CDRX adapting  to quasi (ideal)- period position | 16 | 8 | 4 | 0 | H | 8 | 8 | 92.36% | 36.79% |

#### Jitter Handling

This section provides the performance impact of potential jitter handling mechanisms.

XR DL traffic arrival has jitter which makes exact frame arrival timing random due to random delay contributed from frame encoders in Edge server, network transfer time in core network, etc. If traffic arrives too early, then packets should be delayed until UE wakes up from CDRX off state, which increases the latency for the packet transmission. This can potentially negatively affect the capacity given the tight PDB in DL. DL burst arrives later than the expected time of arrival (where DRX On duration start offset is configured), the UE should wait for DL burst arrival while performing unnecessary PDCCH monitoring. The unnecessary PDCCH monitoring increases UE power consumption. Thus, jitter could decrease capacity and increase UE power consumption. Jitter handling mechanisms address these issues.

##### DL+UL Evaluation

Table 106 Summary of PS schemes for jitter handlings, DL+UL evaluation

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | PS scheme | PS Gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| DU | VR | 30 | eCDRX with jitter handling | 30.50 | 28.12 ~ 32.88 | vivo |
| Enhanced PDCCH monitoring adaptation with jitter handling | 40.64 | 37.65 ~ 43.63 | vivo |
| AR | 30 | eCDRX with jitter handling | 23.36 | 20.65 ~ 27.46 | vivo |
| Enhanced PDCCH monitoring adaptation with jitter handling | 34.11 | 30.63 ~ 40.21 | vivo |
| InH | VR | 30 | eCDRX with jitter handling | 32.14 | 29.92 ~ 34.36 | vivo |
| Enhanced PDCCH monitoring adaptation with jitter handling | 40.74 | 39.86 ~ 41.62 | vivo |
| enhanced CDRX with additional active time | 20.50 | 20.50 | ZTE |
| 45 | eCDRX with additional active time | 25.05 | 25.0 ~ 25.10 | ZTE |
| AR | 30 | eCDRX with jitter handling | 24.30 | 21.43 ~ 30.41 | vivo |
| Enhanced PDCCH monitoring adaptation with jitter handling | 34.04 | 30.45 ~ 39.29 | vivo |
| CG | 30 | eCDRX with additional active time | 21.35 | 21.3 ~ 21.4% | ZTE |

**Observations**

* In FR1, DL+UL evaluation, DU, VR30, it was identified from Source vivo that the eCDRX with jitter handling scheme provides the mean power saving gain of 30.50% in the range of 28.12 ~ 32.88% with *marginal* loss in DL+UL UE satisfied rate.
* In FR1, DL+UL evaluation, DU, VR30, it was identified from Source vivo that the enhanced PDCCH monitoring adaptation with jitter handling scheme provides the mean power saving gain of 40.64% in the range of 37.65 ~ 43.63% with *marginal* loss in DL+UL UE satisfied rate.

Table 107 Source specific data: FR1, DL+UL, DU, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 241 | R1-2111046 | eCDRX with jitter handling | 16 | 3 | 3 | 0 | L | 7 | 13 |  |  | 100.00% | 32.88% |
| vivo | 243 | R1-2111046 | enhanced PDCCH monitoring adaptation with jitter handling | 0 | 0 | 0 | 0 | L | 7 | 13 |  |  | 100.00% | 43.63% |
| vivo | 249 | R1-2111046 | eCDRX with jitter handling | 16 | 3 | 3 | 0 | H | 13 | 13 |  |  | 91.82% | 28.12% |
| vivo | 251 | R1-2111046 | enhanced PDCCH monitoring adaptation with jitter handling | 0 | 0 | 0 | 0 | H | 13 | 13 |  |  | 91.94% | 37.65% |

**Observations**

* In FR1, DL+UL evaluation, DU, AR30, it was identified from Source vivo that the eCDRX with jitter handling scheme provides the mean power saving gain of 23.36% in the range of 20.65 ~ 27.46% with *marginal* loss in DL+UL UE satisfied rate.
* In FR1, DL+UL evaluation, DU, AR30, it was identified from Source vivo that the enhanced PDCCH monitoring with jitter handling scheme provides the mean power saving gain of 34.11% in the range of 30.63 ~ 40.21% with *marginal* loss in DL+UL UE satisfied rate.

Table 108 Source specific data: FR1, DL+UL, DU, AR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 273 | R1-2111046 | Note 3 | 16 | 3 | 3 | Note 1 | L | 5 | 9 |  |  | 95.87% | 27.46% |
| vivo | 275 | R1-2111046 | Note 4 | 0 | 0 | 0 | Note 1 | L | 5 | 9 |  |  | 95.87% | 40.21% |
| vivo | 281 | R1-2111046 | Note 3 | 16 | 3 | 3 | Note 1 | H | 9 | 9 |  |  | 91.71% | 20.65% |
| vivo | 283 | R1-2111046 | Note 4 | 0 | 0 | 0 | Note 1 | H | 9 | 9 |  |  | 91.89% | 33.36% |
| vivo | 305 | R1-2111046 | Note 3 | 16 | 3 | 3 | Note 2 | L | 4 | 7 |  |  | 100.00% | 24.18% |
| vivo | 307 | R1-2111046 | Note 4 | 0 | 0 | 0 | Note 2 | L | 4 | 7 |  |  | 100.00% | 32.25% |
| vivo | 313 | R1-2111046 | Note 3 | 16 | 3 | 3 | Note 2 | H | 7 | 7 |  |  | 91.16% | 21.14% |
| vivo | 315 | R1-2111046 | Note 4 | 0 | 0 | 0 | Note 2 | H | 7 | 7 |  |  | 91.38% | 30.63% |
| Note 1 AR with single UL stream.  Note 2 AR with two UL streams.  Note 3. eCDRX with jitter handling  Note 4. enhanced PDCCH monitoring adaptation with jitter handling | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, InH, VR30, it was identified from Source vivo that the eCDRX with jitter handling scheme provides the mean power saving gain of 32.14% in the range of 29.92 ~ 34.36% with *marginal* loss in DL+UL UE satisfied rate.
* In FR1, DL+UL evaluation, InH, VR30, it was identified from Source vivo that the enhanced PDCCH monitoring adaptation with jitter handling scheme provides the mean power saving gain of 40.64% in the range of 37.65 ~ 43.63% with *marginal* loss in DL+UL UE satisfied rate.
* In FR1, DL+UL evaluation, InH, VR30, it was identified from Source ZTE that the enhanced CDRX with additional active time scheme provides the mean power saving gain of 20.50% with *marginal* loss in DL+UL UE satisfied rate.

Table 109 Source specific data: FR1, DL+UL, InH, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 225 | R1-2111046 | Note 1 | 16 | 3 | 3 |  | L | 5 | 10 |  |  | 100.00% | 34.36% |
| vivo | 227 | R1-2111046 | Note 2 | 0 | 0 | 0 |  | L | 5 | 10 |  |  | 100.00% | 41.62% |
| vivo | 233 | R1-2111046 | Note 1 | 16 | 3 | 3 |  | H | 10 | 10 |  |  | 91.27% | 29.92% |
| vivo | 235 | R1-2111046 | Note 2 | 0 | 0 | 0 |  | H | 10 | 10 |  |  | 91.11% | 39.86% |
| ZTE, Sanechips | 9 | R1-2111351 | Note 3 | 16 | 6 | 4 |  | H | 11 | 11 | 91.67% | 100.00% | 91.67% | 20.50% |
| ZTE, Sanechips | 10 | R1-2111351 | Note 3 | 16 | 6 | 4 |  | H | 11 | 11 | 91.67% | 100.00% | 91.67% | 20.50% |
| Note 1. eCDRX with jitter handling  Note 2. enhanced PDCCH monitoring adaptation with jitter handling  Note 3. eCDRX(change drx-startoffset per 100ms and additional active time) | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, InH, VR45, it was identified from Source ZTE that the enhanced CDRX with additional active time scheme provides the mean power saving gain of 25.05% in the range of 25.0 ~ 25.10% with *marginal* loss in DL+UL UE satisfied rate.

Table 110 Source specific data: FR1, DL+UL, InH, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving  scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| ZTE,  Sanechips | 17 | R1-2111351 | Note 1 | 16 | 6 | 4 | 0 | H | 7 | 7 | 86.30% | 100.00% | 86.30% | 25.10% |
| ZTE,  Sanechips | 18 | R1-2111351 | Note 1 | 16 | 6 | 4 | 0 | H | 7 | 7 | 86.30% | 100.00% | 86.30% | 25.00% |
| Note 1. eCDRX(change drx-startoffset per 100ms and additional active time) | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, InH, AR30, it was identified from Source vivo that the eCDRX with jitter handling scheme provides the mean power saving gain of 24.30% in the range of 21.43 ~ 30.41% with *marginal* loss in DL+UL UE satisfied rate.
* In FR1, DL+UL evaluation, InH, AR30, it was identified from Source vivo that the enhanced PDCCH monitoring adaptation with jitter handling scheme provides the mean power saving gain of 34.04% in the range of 30.45 ~ 39.29% with *marginal* loss in DL+UL UE satisfied rate.

Table 111 Source specific data: FR1, DL+UL, InH, AR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 257 | R1-2111046 | Note 3 | 16 | 3 | 3 | Note 1 | L | 5 | 10 |  |  | 100.00% | 30.41% |
| vivo | 259 | R1-2111046 | Note 4 | 0 | 0 | 0 | Note 1 | L | 5 | 10 |  |  | 100.00% | 39.29% |
| vivo | 265 | R1-2111046 | Note 3 | 16 | 3 | 3 | Note 1 | H | 10 | 10 |  |  | 90.95% | 21.88% |
| vivo | 267 | R1-2111046 | Note 4 | 0 | 0 | 0 | Note 1 | H | 10 | 10 |  |  | 91.67% | 34.46% |
| vivo | 289 | R1-2111046 | Note 3 | 16 | 3 | 3 | Note 2 | L | 5 | 10 |  |  | 100.00% | 23.46% |
| vivo | 291 | R1-2111046 | Note 4 | 0 | 0 | 0 | Note 2 | L | 5 | 10 |  |  | 100.00% | 31.97% |
| vivo | 297 | R1-2111046 | Note 3 | 16 | 3 | 3 | Note 2 | H | 10 | 10 |  |  | 90.79% | 21.43% |
| vivo | 299 | R1-2111046 | Note 4 | 0 | 0 | 0 | Note 2 | H | 10 | 10 |  |  | 91.11% | 30.45% |
| Note 1. AR with single UL stream.  Note 2. AR with two UL streams.  Note 3. eCDRX with jitter handling  Note 4. enhanced PDCCH monitoring adaptation with jitter handling | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, InH, CG30, it was identified from Source ZTE that the enhanced CDRX with additional active time scheme provides the mean power saving gain of 21.35% in the range of 21.3 ~ 21.4% with *marginal* loss in DL+UL UE satisfied rate.

Table 112 Source specific data: FR1, DL+UL, InH, CG30

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| ZTE, Sanechips | 25 | R1-2111351 | Note 1 | 16 | 6 | 4 | 0 | H | 12 | 12 | 88.19% | 100.00% | 88.19% | 21.40% |
| ZTE, Sanechips | 26 | R1-2111351 | Note 1 | 16 | 6 | 4 | 0 | H | 12 | 12 | 88.19% | 100.00% | 88.19% | 21.30% |
| Note 1. eCDRX(change drx-startoffset per 100ms and additional active time) | | | | | | | | | | | | | | |

##### DL-only Evaluation

###### FR1

Table 113 Summary of PS schemes for jitter handlings, FR1, DL-only

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| FR | Scen-arios | App | DL Bit rate (Mbps) | PS scheme | PS Gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| FR1 | DU | VR | 30 | fast/dense WUS for jitter handling with eCDRX | 31 |  | QC |
| eCDRX with jitter handling | 29.60 | 25.11~34.08 | vivo |
| Enhanced PDCCH monitoring adaptation with jitter handling | 42.61 | 37.83~47.38 | vivo |
| 45 | eCDRX with jitter handling | 32.27 | 29.30~35.23 | vivo |
| Enhanced PDCCH monitoring adaptation with jitter handling | 41.23 | 37.26~45.19 | vivo |
| Enhanced CDRX with additional active time | 29.9 | 29.9 | ZTE |
| InH | VR | 30 | enhanced CDRX with additional active time | 29.8 | 29.8 | ZTE |
| eCDRX with jitter handling | 32.21 | 29.06~35.35 | vivo |
| Enhanced PDCCH monitoring adaptation with jitter handling | 44.96 | 41.03~48.88 | vivo |
| 45 | eCDRX with jitter handling | 32.11 | 29.12 ~ 35.09 | vivo |
| Enhanced PDCCH monitoring adaptation with jitter handling | 42.04 | 38.76 ~ 45.32 | vivo |
| enhanced CDRX with additional active time | 29.7 | 29.7 | ZTE |
| CG | 30 | eCDRX with additional active time | 32.4 | 32.4 | ZTE |
| UMa | VR | 30 | eCDRX with jitter handling | 32.40 | 29.29~35.51 | vivo |
| Enhanced PDCCH monitoring adaptation with jitter handling | 43.86 | 40.59~47.13 | vivo |
| 45 | eCDRX with jitter handling | 30.97 | 29.51~32.43 | vivo |
| Enhanced PDCCH monitoring adaptation with jitter handling | 40.22 | 37.18~43.26 | vivo |

DU

**Observations**

* In FR1, DL evaluation, DU, VR30, it was identified from Source QC that the fast/dense WUS for jitter handling + eCDRX scheme provides the mean power saving gain of 31.00% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL evaluation, DU, VR30, it was identified from Source vivo that the eCDRX for jitter handling scheme provides the mean power saving gain of 29.60% in the range of 25.11~34.08% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL evaluation, DU, VR30, it was identified from Source vivo that the enhanced PDCCH for jitter handling scheme provides the mean power saving gain of 42.61% in the range of 37.83~47.38% with *marginal* loss in DL UE satisfied rate.

Table 114 Source specific data:FR1, DL, DU, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| QC | 59 | R1-2110402 | Fast / dense WUS  for jitter handling + eCDRX | 16/17/17 | 6 | 6 | 0 | H | 11 | 11 | 99.30% | 31.00% |
| vivo | 38 | R1-2111046 | eCDRX with jitter handling | 16 | 3 | 3 | 0 | L | 7 | 13 | 100.00% | 34.08% |
| vivo | 40 | R1-2111046 | enhanced PDCCH  monitoring adaptation  with jitter handling | 0 | 0 | 0 | 0 | L | 7 | 13 | 100.00% | 47.38% |
| vivo | 46 | R1-2111046 | eCDRX with jitter handling | 16 | 3 | 3 | 0 | H | 13 | 13 | 91.70% | 25.11% |
| vivo | 48 | R1-2111046 | enhanced PDCCH  monitoring adaptation  with jitter handling | 0 | 0 | 0 | 0 | H | 13 | 13 | 92.43% | 37.83% |

**Observations**

* In FR1, DL evaluation, DU, VR45, it was identified from Source vivo that the eCDRX for jitter handling scheme provides the mean power saving gain of 32.27% in the range of 29.30~35.23% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL evaluation, DU, VR45, it was identified from Source vivo that the enhanced PDCCH for jitter handling scheme provides the mean power saving gain of 41.23% in the range of 37.26~45.19% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL evaluation, DU, VR45, it was identified from Source ZTE that the enhanced CDRX with additional active time scheme provides the mean power saving gain of 29.9% with *marginal* loss in DL UE satisfied rate.

Table 115 Source specific data:FR1, DL, DU, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 54 | R1-2111046 | Note 1 | 16 | 3 | 3 | - | L | 3 | 6 | 97.88% | 35.23% |
| vivo | 56 | R1-2111046 | Note 2 | - | - | - | - | L | 3 | 6 | 100.00% | 45.19% |
| vivo | 62 | R1-2111046 | Note 1 | 16 | 3 | 3 | - | H | 6 | 6 | 95.24% | 29.30% |
| vivo | 64 | R1-2111046 | Note 2 | - | - | - | - | H | 6 | 6 | 95.63% | 37.26% |
| ZTE, Sanechips | 41 | R1-2111351 | Note 3 | 16 | 6 | 4 | - | H | 7 | 7 | 90% | 29.9% |
| Note 1. eCDRX with jitter handling  Note 2. enhanced PDCCH monitoring adaptation with jitter handling  Note 3. enhanced eCDRX(change drx startoffset per 100ms and additional active time) | | | | | | | | | | | | |

InH

**Observations**

* In FR1, DL evaluation, InH, VR30, it was identified from Source vivo that the eCDRX for jitter handling scheme provides the mean power saving gain of 32.21% in the range of 29.06~35.35% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL evaluation, InH, VR30, it was identified from Source vivo that the enhanced PDCCH for jitter handling scheme provides the mean power saving gain of 44.96% in the range of 41.03~48.88% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL evaluation, InH, VR30, it was identified from Source ZTE that the enhanced CDRX with additional active time scheme provides the mean power saving gain of 29.8% with *marginal* loss in DL UE satisfied rate.

Table 116 Source specific data:FR1, DL, InH, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 6 | R1-2111046 | Note 1 | 16 | 3 | 3 | - | L | 5 | 10 | 100.00% | 35.35% |
| vivo | 8 | R1-2111046 | Note 2 | - | - | - | - | L | 5 | 10 | 100.00% | 48.88% |
| vivo | 14 | R1-2111046 | Note 1 | 16 | 3 | 3 | - | H | 10 | 10 | 91.67% | 29.06% |
| vivo | 16 | R1-2111046 | Note 2 | - | - | - | - | H | 10 | 10 | 92.50% | 41.03% |
| ZTE, Sanchips | 31 | R1-2111351 | Note 3 | 16 | 6 | 4 | - | H | 11 | 11 | 91.67% | 29.8% |
| Note 1. eCDRX with jitter handling  Note 2. enhanced PDCCH monitoring adaptation with jitter handling  Note 3. enhanced eCDRX(change drx startoffset per 100ms and additional active time) | | | | | | | | | | | | |

**Observations**

* In FR1, DL only evaluation, InH, VR45, it was identified from Source vivo that the eCDRX for jitter handling provides the mean power saving gain of 32.11% in the range of 29.12 ~ 35.09% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, InH, VR45, it was identified from Source vivo that the enhanced PDCCH monitoring adaptation with jitter handling provides the mean power saving gain of 42.04% in the range of 38.76 ~ 45.32% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL only evaluation, InH, VR45, it was identified from Source ZTE that the enhanced CDRX with additional active time scheme provides the mean power saving gain of 29.7% with *marginal* loss in DL UE satisfied rate.

Table 117 Source specific data: FR1, DL-only, InH, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 22 | R1-2111046 | Note 1 | 16 | 3 | 3 | 0 | L | 3 | 5 | 100.00% | 35.09% |
| vivo | 24 | R1-2111046 | Note 2 | 0 | 0 | 0 | 0 | L | 3 | 5 | 100.00% | 45.32% |
| vivo | 30 | R1-2111046 | Note 1 | 16 | 3 | 3 | 0 | H | 5 | 5 | 94.44% | 29.12% |
| vivo | 32 | R1-2111046 | Note 2 | 0 | 0 | 0 | 0 | H | 5 | 5 | 96.67% | 38.76% |
| ZTE, Sanechips | 35 | R1-2111351 | Note 3 | 16 | 6 | 4 | 0 | H | 7 | 7 | 86.3% | 29.7% |
| Note 1. eCDRX with jitter handling  Note 2. enhanced PDCCH monitoring adaptation with jitter handling  Note 3. enhanced eCDRX(change drx startoffset per 100ms and additional active time) | | | | | | | | | | | | |

**Observations**

* In FR1, DL only evaluation, InH, CG30, it was identified from Source ZTE that the enhanced CDRX with additional active time scheme provides the mean power saving gain of 32.4% with *marginal* loss in DL UE satisfied rate.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| ZTE,  Sanechips | 39 | R1-2111351 | enhanced eCDRX(change drx startoffset per 100ms and additional active time) | 16 | 6 | 4 |  | H | 12 | 12 | 88.19% | 32.4% |

UMa

**Observations**

* In FR1, DL evaluation, UMa, VR30, it was identified from Source vivo that the eCDRX for jitter handling scheme provides the mean power saving gain of 32.40% in the range of 29.29~35.51% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL evaluation, UMa, VR30, it was identified from Source vivo that the enhanced PDCCH for jitter handling scheme provides the mean power saving gain of 43.86% in the range of 40.59~47.13% with *marginal* loss in DL UE satisfied rate.

Table 118 Source specific data:FR1, DL, Uma, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 70 | R1-2111046 | eCDRX with jitter handling | 16 | 3 | 3 | - | L | 4 | 8 | 98.02% | 35.51% |
| vivo | 72 | R1-2111046 | enhanced PDCCH  monitoring adaptation  with jitter handling | - | - | - | - | L | 4 | 8 | 98.81% | 47.13% |
| vivo | 78 | R1-2111046 | eCDRX with jitter handling | 16 | 3 | 3 | - | H | 8 | 8 | 93.25% | 29.29% |
| vivo | 80 | R1-2111046 | enhanced PDCCH  monitoring adaptation  with jitter handling | - | - | - | - | H | 8 | 8 | 93.75% | 40.59% |

**Observations**

* In FR1, DL evaluation, UMa, VR45, it was identified from Source vivo that the eCDRX for jitter handling scheme provides the mean power saving gain of 30.97% in the range of 29.51~32.43% with *marginal* loss in DL UE satisfied rate.
* In FR1, DL evaluation, UMa, VR45, it was identified from Source vivo that the enhanced PDCCH for jitter handling scheme provides the mean power saving gain of 40.22% in the range of 37.18~43.26% with *marginal* loss in DL UE satisfied rate.

Table 119 Source specific data:FR1, DL, UMa, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 86 | R1-2111046 | Note 1 | 16 | 3 | 3 | - | L | 2 | 4 | 96.83% | 32.43% |
| vivo | 88 | R1-2111046 | Note 2 | - | - | - | - | L | 2 | 4 | 96.83% | 43.26% |
| vivo | 94 | R1-2111046 | Note 1 | 16 | 3 | 3 | - | H | 4 | 4 | 92.46% | 29.51% |
| vivo | 96 | R1-2111046 | Note 2 | - | - | - | - | H | 4 | 4 | 94.05% | 37.18% |
| Note 1. eCDRX with jitter handling  Note 2. enhanced PDCCH monitoring adaptation with jitter handling | | | | | | | | | | | | |

###### FR2

DU

Table 120 Summary of PS schemes for jitter handlings, FR2, DL-only

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| FR | Scen-arios | App | DL Bit rate (Mbps) | PS scheme | PS Gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| FR2 | DU | VR | 30 | Enhanced PDCCH monitoring adaptation with jitter handling | 57.58 | 55.51~59.65 | vivo |
| 45 | Enhanced PDCCH monitoring adaptation with jitter handling | 52.03 | 50.46~53.59 | vivo |
| InH | VR | 30 | Enhanced PDCCH monitoring adaptation with jitter handling | 59.69 | 57.53~61.85 | vivo |
| 45 | Enhanced PDCCH monitoring adaptation with jitter handling | 53.32 | 52.14~54.50 | vivo |

**Observations**

* In FR2, DL evaluation, DU, VR30, it was identified from Source vivo that the enhanced PDCCH for jitter handling scheme provides the mean power saving gain of 57.58% in the range of 55.51~59.65% with *marginal* loss in DL UE satisfied rate.

Table 121 Source specific data:FR2, DL, DU, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 126 | R1-2111046 | enhanced PDCCH  monitoring adaptation  with jitter handling | - | - | - | - | L | 7 | 13 | 99.55% | 59.65% |
| vivo | 132 | R1-2111046 | eCDRX with jitter handling | 16 | 3 | 3 | - | H | 13 | 13 | 95.24% | 55.51% |

**Observations**

* In FR2, DL evaluation, DU, VR45, it was identified from Source vivo that the enhanced PDCCH for jitter handling scheme provides the mean power saving gain of 52.03% in the range of 50.46~53.59% with *marginal* loss in DL UE satisfied rate.

Table 122 Source specific data:FR2, DL, DU, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 138 | R1-2111046 | enhanced PDCCH  monitoring adaptation  with jitter handling | - | - | - | - | L | 4 | 8 | 100.00% | 53.59% |
| vivo | 144 | R1-2111046 | eCDRX with jitter handling | 16 | 3 | 3 | - | H | 8 | 8 | 93.25% | 50.46% |

InH

**Observations**

* In FR2, DL evaluation, InH, VR30, it was identified from Source vivo that the enhanced PDCCH for jitter handling scheme provides the mean power saving gain of 59.69% in the range of 57.53~61.85% with *marginal* loss in DL UE satisfied rate.

Table 123 Source specific data:FR2, DL, InH, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 102 | R1-2111046 | enhanced PDCCH  monitoring adaptation  with jitter handling | - | - | - | - | L | 4 | 8 | 100.00% | 61.85% |
| vivo | 108 | R1-2111046 | eCDRX with jitter handling | 16 | 3 | 3 | - | H | 8 | 8 | 92.01% | 57.53% |

**Observations**

* In FR2, DL evaluation, InH, VR45, it was identified from Source vivo that the enhanced PDCCH for jitter handling scheme provides the mean power saving gain of 53.32% in the range of 52.14~54.50% with *marginal* loss in DL UE satisfied rate.

Table 124 Source specific data:FR2, DL, InH, VR45

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| vivo | 114 | R1-2111046 | enhanced PDCCH  monitoring adaptation  with jitter handling | - | - | - | - | L | 2 | 4 | 100.00% | 54.50% |
| vivo | 120 | R1-2111046 | eCDRX with jitter handling | 16 | 3 | 3 | - | H | 4 | 4 | 94.44% | 52.14% |

#### XR dedicated PDCCH Monitoring Window

In this section, we capture the evaluation results for dynamic scheduling of XR specific dedicated PDCCH monitoring window scheme with PDCCH skipping and go-to-sleep. In this scheme, XR dedicated PDCCH monitoring window/cycle is defined, which is disassociated with the DRX configuration, but aligned with XR traffic pattern. Dynamic scheduling with XR specific dedicated PDCCH monitoring window scheme would have UE monitor PDCCH in the given window in both within Active time and outside Active Time when DRX is configured.

Table 125 Summary of source specific data for XR dedicated PDCCH Monitoring Window, FR1, InH, VR

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | Direction | Assumptions | PS Gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| InH | VR | 30 | DL | PDCCH monitoring window with PDCCH skipping and go-to-sleep | 26.73 | 24.01~29.44 | CATT |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL satisfied UE. | | | | | | | |

**Observations**

* In FR1, DL evaluation, DU, VR30, it was identified from Source CATT that the XR dedicated PDCCH monitoring window scheme provides the mean power saving gain of 26.73% in the range of 24.01~29.44% with *marginal* loss in DL UE satisfied rate.

Table 126 Source specific data: FR1, DL, InH, VR30, XR dedicated PDCCH monitoring window

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional  Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| CATT | 4 | R1-2111234 | XR-dedicated PDCCH  monitoring window  with go-to-sleep | 0 | 0 | 0 | Monitoring cycle  =16.67ms;  Monitoring window=16.67ms; | H | 12 | 12 | 90.00% | 24.01% |
| CATT | 5 | R1-2111234 | XR-dedicated PDCCH  monitoring window  with PDCCH skipping  and go-to-sleep | 0 | 0 | 0 | Monitoring cycle =16.67ms;  Monitoring window=16.67ms; | H | 12 | 12 | 89.16% | 29.44% |

#### Network Coding

This section captures the evaluation results of network/outer coding for XR applications. Network/outer coding adds coded redundancy to combat packet errors. The added redundancy allows a video frame to be decoded with a high probability without HARQ retransmissions and ACK/NACK feedback. In this evaluation, the power saving gain is computed with respect to AlwaysOn with HARQ enabled.

**Observations**

* In FR1, DL evaluation, DU, VR30, it was identified from Source QC that network coding and eCDRX together provides the mean power saving gain of 5.86% in the range of -0.2~11% with *marginal* loss in DL UE satisfied rate.

Table 127 Source specific data: DL, VR30, Network coding + eCDRX

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving  scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | FR | Data rate | Initial BLER | CC | Additional assumption | N1 | Mean PSG of all Ues (%) |
| QC | 84 | R1-2110402 | Note 4 | 0 | Note 3 | 2 | FR1 | 8 | 0.1 | 1 | Note 1,2 | 1 | 6.00% |
| QC | 85 | R1-2110402 | Note 4 | 0 | Note 3 | 2 | FR1 | 30 | 0.1 | 1 | Note 1,2 | 1 | 10.00% |
| QC | 86 | R1-2110402 | Note 4 | 0 | Note 3 | 2 | FR1 | 50 | 0.1 | 1 | Note 1,2 | 1 | 7.00% |
| QC | 87 | R1-2110402 | Note 4 | 0 | Note 3 | 2 | FR2 | 8 | 0.05 | 1 | Note 1,2 | 1 | -0.20% |
| QC | 88 | R1-2110402 | Note 4 | 0 | Note 3 | 2 | FR2 | 30 | 0.05 | 1 | Note 1,2 | 1 | 11.00% |
| QC | 89 | R1-2110402 | Note 4 | 0 | Note 3 | 2 | FR2 | 50 | 0.05 | 1 | Note 1,2 | 1 | 7.00% |
| QC | 114 | R1-2112244 | Note 4 | 0 | Note 3 | 2 | FR2 | 8 | 0.05 | 4 | Note 1,2 | 1 | 2.15% |
| QC | 115 | R1-2112244 | Note 4 | 0 | Note 3 | 2 | FR2 | 30 | 0.05 | 4 | Note 1,2 | 1 | 3.80% |
| QC | 116 | R1-2112244 | Note 4 | 0 | Note 3 | 2 | FR2 | 50 | 0.05 | 4 | Note 1,2 | 1 | 1.63% |
| QC | 117 | R1-2112244 | Note 4 | 0 | Note 3 | 0 | FR2 | 8 | 0.05 | 4 | Note 1,2 | 1 | 4.68% |
| QC | 118 | R1-2112244 | Note 4 | 0 | Note 3 | 0 | FR2 | 30 | 0.05 | 4 | Note 1,2 | 1 | 9.63% |
| QC | 119 | R1-2112244 | Note 4 | 0 | Note 3 | 0 | FR2 | 50 | 0.05 | 4 | Note 1,2 | 1 | 7.58% |
| Note 1. The captured network/outer coding simulations do not follow 3GPP RAN1 evaluation methodology. MAC and above is modelled with fixed TB size + HARQ BLER probability.  Note 2. HARQ assumption: Use of field data to obtain correlation between successive TB transmissions; Markov model  Note 3. The ON timer is not modelled. The ON time is matched to the UE's active time, i.e., when receiving PDSCH and monitoring PDCCH.  Note 4. Network/outer coding + eCDRX | | | | | | | | | | | | | |

#### Additional Packet Delay Budget with Playout Buffer

This section captures the evaluation results of the impact of additional PDB (APDB) on UE power consumption. If the size of playout buffer is known at gNB, then, additional PDB could be used for packet scheduling which could potentially increase capacity and reduce power consumption.

**Observations**

* In FR1, DL evaluation, DU, VR30, it was identified from Source CATT that additional packet delay budget with play out buffer provides the mean power saving gain of 30.42% in the range of 26.43~34.56% with *marginal* loss in DL UE satisfied rate.

Table 128 Source specific data for additional packet delay budget with play out buffer: FR1, DU, DL, VR30

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| CATT | 6 | R1-2111234 | CDRX(16,8,4)  with go-to-sleep  with UE playout buffer | 0 | 0 | 0 | 0 | H | 12 | 12 | 94.17% | 26.43% |
| CATT | 7 | R1-2111234 | C-DRX(16,8,4)  with PDCCH skipping  and go-to-sleep  with UE playout buffer | 0 | 0 | 0 | 0 | H | 12 | 12 | 93.30% | 34.56% |
| CATT | 8 | R1-2111234 | PDCCH skipping  with UE playout buffer | 0 | 0 | 0 | 0 | H | 12 | 12 | 91.67% | 30.26% |

#### Traffic Arrival Offset Staggering

This section captures the evaluation results of the impact of different traffic arrival offsets across different UEs. The XR DL traffic arrival offsets potentially determines the time UE wakes up and how long the UE need to be awake. When the frame arrivals are aligned with each other, the XR traffic of the UEs contend for resources, decreasing the capacity and increasing power consumption due to the increased UE awake time. If the frame arrivals of UEs are staggered relative to each other, the cell can serve UEs minimizing the overlap of scheduling durations of each UE, which consequently reduce UEs’ awake time and make UEs stay longer in sleep state.

Table 129 Summary of source specific data for traffic arrival offset staggering, FR1, DU, VR, DL+UL

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Scen-arios | App | DL Bit rate (Mbps) | Fps | Traffic arrival offset | PS Gain (%), Note 1 | | Source |
| Mean (%) | Range (%) |
| DU | VR | 30 | 60 | Random | 1.57 | 1.57 | QC |
| Evenly spaced | 4.07 | 2~6.14 | QC |
| 30 | Random | 1.79 | 0.15~3.44 | QC |
| Evenly spaced | 8.55 | 3.69~13.4 | QC |
| 45 | 60 | Random | 2.01 | 1.82~2.21 | QC |
| Evenly spaced | 4.16 | 2.13~6.19 | QC |
| 30 | Random | -1.33 | -4.53~1.86 | QC |
| Evenly spaced | 4.3 | 2.06~6.54 | QC |
| Note 1 : PSG was computed for the cases only with marginal loss in % of DL satisfied UE. | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, DU, VR30Mbps-60Fps, it was identified from Source QC that making random traffic arrival offset provide the mean power saving gain of 1.57% with respect to all synced traffic arrival offset with *marginal* loss in DL+UL UE satisfied rate.
* In FR1, DL+UL evaluation, DU, VR30Mbps-60Fps, it was identified from Source QC that making evenly spaced traffic arrival offset provide the mean power saving gain of 4.07% in the range of 2~6.14% with respect to all synced traffic arrival offset with *marginal* loss in DL+UL UE satisfied rate.

Table 130 Source specific data: FR1, DU, DL+UL, VR30Mbps-60Fps, ULPose60Fps

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Traffic arrival offset | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| QC | 93 | R1-2112244 | Always ON | 0 | 0 | 0 | All Sync | H | 7 | 7 | 90.00% | 99.10% | 90.00% | 0.00% |
| QC | 94 | R1-2112244 | Always ON | 0 | 0 | 0 | Random | H | 7 | 8 | 100.00% | 99.50% | 100.00% | 1.57% |
| QC | 95 | R1-2112244 | Always ON | 0 | 0 | 0 | Evenly Spaced | L | 7 | 9 | 100.00% | 99.30% | 99.00% | 2.00% |
| QC | 105 | R1-2112244 | Note 1 | 0 | 0 | 0 | All Sync | H | 7 | 7 | 90.00% | 99.10% | 90.00% | 0.00% |
| QC | 106 | R1-2112244 | Note 1 | 0 | 0 | 0 | Random | H | 7 | 8 | 100.00% | 99.50% | 100.00% | 1.57% |
| QC | 107 | R1-2112244 | Note 1 | 0 | 0 | 0 | Evenly Spaced | L | 7 | 9 | 100.00% | 99.30% | 99.00% | 6.14% |
| Note 1. Genie (CDRX with ideal PDCCH Skipping) | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, DU, VR30Mbps-30Fps, it was identified from Source QC that making evenly spaced traffic arrival offset provide the mean power saving gain of 1.79% in the range of 0.15~3.44% with respect to all synced traffic arrival offset with *marginal* loss in DL+UL UE satisfied rate.
* In FR1, DL+UL evaluation, DU, VR30Mbps-30Fps, it was identified from Source QC that making evenly spaced traffic arrival offset provide the mean power saving gain of 8.55% in the range of 3.69~13.4% with respect to all synced traffic arrival offset with *marginal* loss in DL+UL UE satisfied rate.

Table 131 Source specific data: FR1, DU, DL+UL, VR30Mbps-30Fps, ULPose30Fps

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Traffic arrival offset | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| QC | 99 | R1-2112244 | Always ON | 0 | 0 | 0 | All Sync | H | 3 | 3 | 92.00% | 99.70% | 92.00% | 0.00% |
| QC | 100 | R1-2112244 | Always ON | 0 | 0 | 0 | Random | L | 3 | 6 | 98.00% | 100.00% | 98.00% | 3.44% |
| QC | 101 | R1-2112244 | Always ON | 0 | 0 | 0 | Evenly Spaced | L | 3 | 8 | 98.00% | 100.00% | 98.00% | 3.69% |
| QC | 111 | R1-2112244 | Note 1 | 0 | 0 | 0 | All Sync | H | 3 | 3 | 92.00% | 99.70% | 92.00% | 0.00% |
| QC | 112 | R1-2112244 | Note 1 | 0 | 0 | 0 | Random | L | 3 | 6 | 98.00% | 100.00% | 98.00% | 0.15% |
| QC | 113 | R1-2112244 | Note 1 | 0 | 0 | 0 | Evenly Spaced | L | 3 | 8 | 98.00% | 100.00% | 98.00% | 13.40% |
| Note 1. Genie (CDRX with ideal PDCCH Skipping) | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, DU, VR30Mbps-30Fps, it was identified from Source QC that making evenly spaced traffic arrival offset provide the mean power saving gain of 2.01% in the range of 1.82~2.21% with respect to all synced traffic arrival offset with *marginal* loss in DL+UL UE satisfied rate.
* In FR1, DL+UL evaluation, DU, VR30Mbps-30Fps, it was identified from Source QC that making evenly spaced traffic arrival offset provide the mean power saving gain of 4.16% in the range of 2.13~6.19% with respect to all synced traffic arrival offset with *marginal* loss in DL+UL UE satisfied rate.

Table 132 Source specific data: FR1, DL+UL, VR45Mbps-60Fps, ULPose60Fps

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| QC | 90 | R1-2112244 | Always ON | 0 | 0 | 0 | 0 | H | 4 | 4 | 98.00% | 99.40% | 98.00% | 0.00% |
| QC | 91 | R1-2112244 | Always ON | 0 | 0 | 0 | 0 | H | 4 | 5 | 99.00% | 99.40% | 99.00% | 1.82% |
| QC | 92 | R1-2112244 | Always ON | 0 | 0 | 0 | 0 | L | 4 | 6 | 100.00% | 99.40% | 99.00% | 2.13% |
| QC | 102 | R1-2112244 | Note 1 | 0 | 0 | 0 | 0 | H | 4 | 4 | 98.00% | 99.40% | 98.00% | 0.00% |
| QC | 103 | R1-2112244 | Note 1 | 0 | 0 | 0 | 0 | H | 4 | 5 | 99.00% | 99.40% | 99.00% | 2.21% |
| QC | 104 | R1-2112244 | Note 1 | 0 | 0 | 0 | 0 | L | 4 | 6 | 100.00% | 99.40% | 99.00% | 6.19% |
| Note 1. Genie (CDRX with ideal PDCCH Skipping) | | | | | | | | | | | | | | |

**Observations**

* In FR1, DL+UL evaluation, DU, VR30Mbps-30Fps, it was identified from Source QC that making evenly spaced traffic arrival offset provide the mean power saving gain of -1.33% in the range of -4.53~1.86% with respect to all synced traffic arrival offset with *marginal* loss in DL+UL UE satisfied rate.
* In FR1, DL+UL evaluation, DU, VR30Mbps-30Fps, it was identified from Source QC that making evenly spaced traffic arrival offset provide the mean power saving gain of 4.3% in the range of 2.06~6.54% with respect to all synced traffic arrival offset with *marginal* loss in DL+UL UE satisfied rate.

Table 133 Source specific data: FR1, DU, DL+UL, VR45Mbps-30Fps, ULPose30Fps

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | CDRX cycle (ms) | ODT (ms) | IAT (ms) | Additional Assumptions | Load H/L | N1 | C1 | % of DL satisfied UE | % of UL satisfied UE | % of DL + UL satisfied UE | Mean PSG of all Ues (%) |
| QC | 96 | R1-2112244 | Always ON | 0 | 0 | 0 | 0 | H | 1 | 1 | 97.00% | 100.00% | 97.00% | 0.00% |
| QC | 97 | R1-2112244 | Always ON | 0 | 0 | 0 | 0 | L | 1 | 3 | 98.00% | 100.00% | 98.00% | 1.86% |
| QC | 98 | R1-2112244 | Always ON | 0 | 0 | 0 | 0 | L | 1 | 5 | 99.00% | 100.00% | 99.00% | 2.06% |
| QC | 108 | R1-2112244 | Note 1 | 0 | 0 | 0 | 0 | H | 1 | 1 | 97.00% | 100.00% | 97.00% | 0.00% |
| QC | 109 | R1-2112244 | Note 1 | 0 | 0 | 0 | 0 | L | 1 | 3 | 98.00% | 100.00% | 98.00% | -4.53% |
| QC | 110 | R1-2112244 | Note 1 | 0 | 0 | 0 | 0 | L | 1 | 5 | 99.00% | 100.00% | 99.00% | 6.54% |
| Note 1. Genie (CDRX with ideal PDCCH Skipping) | | | | | | | | | | | | | | |

#### SR group switching

This section captures the evaluation results of the SR group switching and baseline. The XR UL traffic arrives frequently, especially for pose/control. For dynamic scheduling, UE transmits a SR if UE has data to be transmitted. UE will monitor PDCCH for potential UL grant after the transmission of SR. Frequent SR transmission will increase both UL and DL power consumption. Switching between a dense SR periodicity and a sparse SR periodicity can achieve a tradeoff between latency of UL data transmission and UE power consumption.

**Observation**

* In FR1, UL evaluation, InH, ULPose with 250FPS, it was identified from Source ZTE that SR group switching provide the mean power saving gain of 12.1% with respect to UL\_baseline (UE can perform UL transmission at every UL slot/symbol if needed) with *marginal* loss in UL UE satisfied rate.

Table 134 Source specific data: FR1, InH, UL, UL Pose 250FPS

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | SR switch cycle (ms) | SR group #1 periodicity (slots) | SR group #1 duration(ms) | SR group #2 periodicity (slot) | SR group #2 duration(ms) | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| ZTE,Sanechips | 42 | R1-2111351 | UL\_baseline, Note 1 |  |  |  |  |  | L | 11 | >40 | 100% | 0% |
| ZTE,Sanechips | 43 | R1-2111351 | SR group switching, Note 1 | 16 | 1 | 6 | 15 | 10 | L | 11 | >40 | 100% | 12.1% |
| Note 1: If UE transmits SR, UE will monitor PDCCH for the subsequent 2.5ms, otherwise, UE does not monitor PDCCH. | | | | | | | | | | | | | |

**Observation**

* In FR1, UL evaluation, DU, UL Pose 250FPS it was identified from Source ZTE that SR group switching provide the mean power saving gain of 11.37% with respect to UL baseline(UE can perform UL transmission at every UL slot/symbol if needed) with *marginal* loss in UL UE satisfied rate.

Table 135 Source specific data: FR1, DU, UL, UL Pose 250FPS

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | SR switch cycle (ms) | SR group #1 periodicity (slots) | SR group #1 duration(ms) | SR group #2 periodicity (slot) | SR group #2 duration(ms) | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| ZTE,Sanechips | 44 | R1-2111351 | UL\_baseline, Note 1 |  |  |  |  |  | L | 11 | >40 | 100% | 0% |
| ZTE,Sanechips | 45 | R1-2111351 | SR group switching, Note 1 | 16 | 1 | 6 | 15 | 10 | L | 11 | >40 | 100% | 11.37% |
| Note 1: If UE transmits SR, UE will monitor PDCCH for the subsequent 2.5ms, otherwise, UE does not monitor PDCCH. | | | | | | | | | | | | | |

#### UL active time

This section captures the evaluation results of the UL active time and baseline. Various signals/data needs to be transmitted in UL. The independent transmission occasion of each signals/data shall reduce the sleep chance at the UE. If the transmission of UL signals/data can be confined within an UL active time, UE is more likely to go to a deeper sleep UE only transmits UL signals/data within the UL active time and cannot transmit UL signals outside the UL active time.

**Observation**

* In FR1, UL evaluation, InH, UL Pose 250FPS, it was identified from Source ZTE that UL active time provide the mean power saving gain of 16.335% in the range of 13.67 ~19% with respect to UL\_baseline(UE can perform UL transmission at every UL slot/symbol if needed) with *marginal* loss in UL UE satisfied rate.

Table 136 Source specific data: FR1, InH, UL, UL Pose250FPS

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | UL active time cycle (ms) | UL active time duration (slots) | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| ZTE,Sanechips | 46 | R1-2111351 | UL\_baseline, Note 1 |  |  | L | 11 |  | 100% | 0% |
| ZTE,Sanechips | 47 | R1-2111351 | UL active time, Note 1 | 8 | 4 | L | 11 |  | 100% | 13.67% |
| ZTE,Sanechips | 50 | R1-2111351 | UL\_baseline, Note 1 |  |  | L | 3 |  | 100% | 0% |
| ZTE,Sanechips | 51 | R1-2111351 | UL active time, Note 1 | 8 | 3 | L | 3 |  | 100% | 19% |
| Note 1: configured grant(periodicity = 2.5ms), UE does not need to monitor PDCCH. | | | | | | | | | | |

**Observation**

* In FR1, UL evaluation, DU, UL Pose 250FPS, it was identified from Source ZTE that UL active time provide the mean power saving gain of 14% with respect to UL baseline(UE can perform UL transmission at every UL slot/symbol if needed) with *marginal* loss in UL UE satisfied rate.

Table 137 Source specific data: FR1, DU, UL, UL Pose250FPS

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | data row index | Tdoc source | Power saving scheme | UL active time cycle (ms) | UL active time duration (slots) | Load H/L | N1 | C1 | % of UL satisfied UE | Mean PSG of all Ues (%) |
| ZTE,Sanechips | 48 | R1-2111351 | UL\_baseline, Note 1 |  |  | L | 11 |  | 100% | 0% |
| ZTE,Sanechips | 49 | R1-2111351 | UL active time, Note 1 | 8 | 4 | L | 11 |  | 100% | 14% |
| Note 1: configured grant (periodicity = 2.5ms), UE does not need to monitor PDCCH. | | | | | | | | | | |

#### Enhanced PDCCH monitoring

This section captures the evaluation results of enhanced PDCCH monitoring, where it configures a MonitoringSlotPeriodicity pattern with different MonitoringSlotPeriodicity values instead of a single MonitoringSlotPeriodicity value. For example, MonitoringSlotPeriodicity pattern is set as {17, 17, 16}ms.

**Observation**

* In FR1, for DL VR/AR@30Mbps and DL CG 30Mbps in DU, it was identified from Source Huawei that enhanced PDCCH monitoring provides the power saving gain in the range of 5%~22%

Table 138 Source specific data: FR1, Dense Urban, DL, VR/AR30

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | Tdoc source | Power saving scheme | MonitoringSlotPeriodicity pattern | Duration (ms) | MonitoringSlotOffset (ms) | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 8 | -2 | L | 3 | 5 | 75.24% | 22.05% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 10 | -4 | L | 3 | 5 | 74.92% | 15.38% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 12 | -4 | L | 3 | 5 | 94.76% | 9.09% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 14 | -4 | L | 3 | 5 | 97.94% | 5.18% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 8 | -2 | H | 5 | 5 | 59.05% | 21.84% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 10 | -4 | H | 5 | 5 | 59.90% | 15.25% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 12 | -4 | H | 5 | 5 | 84.57% | 8.96% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 14 | -4 | H | 5 | 5 | 90.67% | 5.08% |

Table 139 Source specific data: FR1, Dense Urban, DL, CG30

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| source | Tdoc source | Power saving scheme | MonitoringSlotPeriodicity pattern | Duration (ms) | MonitoringSlotOffset (ms) | Load H/L | N1 | C1 | % of DL satisfied UE | Mean PSG of all Ues (%) |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 8 | -2 | L | 3 | 7 | 92.22% | 21.91% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 10 | -4 | L | 3 | 7 | 97.62% | 15.22% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 12 | -4 | L | 3 | 7 | 99.37% | 9.05% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 14 | -4 | L | 3 | 7 | 99.84% | 5.16% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 8 | -2 | H | 7 | 7 | 60.88% | 21.38% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 10 | -4 | H | 7 | 7 | 71.84% | 14.58% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 12 | -4 | H | 7 | 7 | 83.67% | 8.73% |
| Huawei, HiSilicon | R1-2110811 | e-PDCCH monitoring | 17/17/16 ms | 14 | -4 | H | 7 | 7 | 88.44% | 4.95% |

1. The loss in UE satisfied rate is said *marginal* if the DL+UL UE satisfied rate is larger than equal to 80% for a considered power saving scheme when the number of UEs per cell is equal to capacity. This definition applies all other cases and sections. [↑](#footnote-ref-1)
2. The loss in UE satisfied rate is said *marginal* if the DL UE satisfied rate is larger than equal to 80% for a considered power saving scheme when the number of UEs per cell is equal to capacity. This definition applies all other sections. [↑](#footnote-ref-2)
3. The loss in UE satisfied rate is said *marginal* if the UL UE satisfied rate is larger than equal to 80% for a considered power saving scheme when the number of UEs per cell is equal to capacity. This definition applies all other sections. [↑](#footnote-ref-3)
4. The loss in UE satisfied rate is said *marginal* if the DL UE satisfied rate is larger than equal to 80% for a considered power saving scheme when the number of UEs per cell is equal to capacity. This definition applies all other sections. [↑](#footnote-ref-4)
5. The loss in UE satisfied rate is said *marginal* if the UL UE satisfied rate is larger than equal to 80% for a considered power saving scheme when the number of UEs per cell is equal to capacity. This definition applies all other sections [↑](#footnote-ref-5)