**3GPP TSG RAN WG1 Meeting #106-e R1-21xxxxx**

**E-meeting, August 16th – 27th, 2021**

**Source: Moderator (vivo)**

**Title: Discussion summary #2 of [106-e-NR-52-71GHz-05]**

**Agenda item: 8.2.5**

**Document for: Discussion and decision**

# Introduction

In this contribution, we summarize issues regarding PDSCH/PUSCH enhancements for new SCSs on supporting NR from 52.6 GHz to 71 GHz for the following email discussion in RAN1 #106-e.

[106-e-NR-52-71GHz-05] Email discussion/approval on defining maximum bandwidth for new SCSs, timeline related aspects adapted to each of the new numerologies 480kHz and 960kHz and reference signals with checkpoints for agreements on August 19, 24 and 27 – Huaming (vivo)

Note that the scope of agenda 8.2.5 including defining maximum bandwidth for new SCSs, time line related aspects adapted to each of the new numerologies 480kHz and 960kHz, reference signals, scheduling particularly w.r.t. multi-PDSCH/PUSCH with a single DCI, HARQ, etc. In this summary, only issues related to bandwidth for new SCSs, time line related aspects adapted to each of the new numerologies 480kHz and 960kHz and reference signals are summarized. Issues related to scheduling particularly w.r.t. multi-PDSCH/PUSCH with a single DCI, HARQ are not in the scope of this summary.

# PDSCH/PUSCH enhancements for new SCSs

In this section, we provide a summary of issues, observations and proposals related to PDSCH/PUSCH enhancements for new SCSs discussed in the submitted contributions.

As in WID, the related objectives for this summary of agenda 8.2.5 are the following.

* Physical layer aspects including [RAN1]:
  + In addition to 120kHz SCS, specify new SCS, 480kHz and 960kHz, and define maximum bandwidth(s), for operation in this frequency range for data and control channels and reference signals, only NCP supported.

Note: Except for timing line related aspects, a common design framework shall be adopted for 480kHz to 960kHz

* + Time line related aspects adapted to 480kHz and 960kHz, e.g., BWP and beam switching timing, HARQ timing, UE processing, preparation and computation timelines for PDSCH, PUSCH/SRS and CSI, respectively.
  + Evaluate, and if needed, specify the PTRS enhancement for 120kHz SCS, 480kHz SCS and/or 960kHz SCS, as well as DMRS enhancement for 480kHz SCS and/or 960kHz SCS.

## 2.1. Channel bandwidth(s) related

### Individual observations/proposals

The following are individual observations/proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [22, Apple] | Conclusion 1: On the issue of maximum and minimum channel bandwidths, based on RAN4 feedback, the following can be concluded:   * Minimum Channel BW for 120 kHz: 100 MHz * Minimum Channel BW for 480 kHz: 400 MHz * Minimum Channel BW for 960 kHz: 400 MHz * Maximum Channel BW for 120 kHz: 400 MHz * Maximum Channel BW for 480 kHz: 1600 MHz   + BWs are applicable to both licensed and unlicensed channels subject to further review of licences spectrum block sizes.   The following issues are still pending:   * Maximum Channel BW for 960 kHz * Questions on channelization and # of RBS for each BW |

### Summary on bandwidth(s) related

In RAN1#104-e meeting, the following were agreed.

* From RAN1 perspective, for NR operation in 52.6 GHz to 71 GHz,
  + The maximum channel bandwidth for 120 kHz SCS is 400 MHz
  + The maximum channel bandwidth for 480 kHz SCS is 1600 MHz
  + The maximum channel bandwidth for 960 kHz SCS is one of the following options
    - 2000 MHz
    - 2160 MHz
* Send LS to RAN4 to inform about RAN1’s agreement of maximum channel bandwidth and ask RAN4 to decide and feedback the exact value of maximum channel bandwidth for 960 kHz SCS, the corresponding numbers of RBs for the maximum channel bandwidth of SCS(s) supported in 52.6 GHz to 71 GHz.
* From RAN1 perspective, for NR operation in 52.6 GHz to 71 GHz, at least the following options on minimum channel bandwidth are identified.
  + for 120 kHz SCS
    - Option 1-1: 100 MHz
    - Option 1-2: 200 MHz
    - Option 1-3: 400 MHz
  + for 480 kHz SCS
    - Option 2-1: 200 MHz
    - Option 2-2: 400 MHz
  + for 960 kHz SCS
    - Option 3-1: 400 MHz
    - Option 3-2: 800 MHz
    - Option 3-3: same value as the maximum channel bandwidth for 960 kHz SCS
* Further study in RAN1 the above options’ implications on RAN1 design and specification
* Send LS to RAN4 to inform about RAN1’s identified options of minimum channel bandwidth and ask RAN4 to decide and feedback the minimum channel bandwidth

Only one contribution [22, Apple] submitted to this meeting discussed issues related to channel bandwidth where [22, Apple] concluded several bandwidth aspects based on RAN4’s reply LS and identified the remaining issues related to channel bandwidth(s).

Moderator’s comment:

It is moderator’s understanding that the remaining issues (the maximum channel bandwidth for 960 kHz and channelization etc.) are under the responsibility of RAN4 and no further discussion/agreement is needed in RAN1 before RAN4’s feedback.

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Yes, we agree with the moderator’s comment |
| Huawei, HiSilicon | We agree that this discussion is now in the hands of RAN4 |
| LG Electronics | Agree with the moderator’s comment |
| Intel | Agree with moderator, issue is assumed to be handled in RAN4.  On a side note, RAN4 has agreed to [2000] GHz for max CBW for 960kHz in last meeting (R4#99e). |
| Futurewei | Agree that RAN1 wait for RAN4 decision on the maximum channel bandwidth for 960kHz and channelization etc. |

## 2.2. Timeline

### Individual observations/proposals

The following are individual observations and proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [1, Huawei] | Proposal 1: The absolute time of 120 kHz SCS timelines should be adopted by default unless the reduced value for specific timeline(s) can be verified by implementation.  Proposal 2: For single slot scheduling with 480 kHz and 960 kHz SCS, N1, N2 and N3 values providing same absolute processing time as that of 120 kHz SCS in FR2 is preferred. The values should be further studied for the case of multi slot scheduling after the detailed schemes are clear, which includes the position of DMRS, the number of PUCCHs for HARQ feedback, PTRS pattern.  Proposal 3: The value range of k0 and k2 should be extended to 0~128 and 0~256 for 480 kHz and 960 kHz SCS respectively.  Proposal 4: The value range of k1 should be defined for DCI format 1\_0, 1\_1 and 1\_2 separately:  For DCI format 1\_0: define a new set with scaled values for 480 kHz and 960 kHz respectively;   * {4, 8, 12, 16, 20, 24, 28, 32} for 480 kHz * {8, 16, 24, 32, 40, 48, 56, 64} for 960 kHz   For DCI format 1\_1: define -1~63 and -1~127 as the value range of k1 for 480 kHz and 960 kHz;  For DCI format 1\_2: define 0~63 and 0~127 as the value range of k1 for 480 kHz and 960 kHz.  Proposal 5: For 480 kHz and 960 kHz SCS, Z1, Z2 and Z3 values providing same absolute processing time as that of 120 kHz SCS in FR2 is preferred. |
| [3, vivo] | Proposal 7: To design the timeline, we may need to investigate more on the target performance for a given UE and UE capability limitation.  Proposal 8: The default set for PDSCH-to-HARQ\_feedback timing indicator should be adapted to the SCS of PDSCH. |
| [7, Lenovo] | Proposal 12: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, following enhancements should be supported to efficiently utilize UE’s limited processing capability to reduce latency and efficiently handle processing/preparation of CSI reports associated with multiple numerologies in parallel:   * Same reference symbols duration (possibly the shortest duration corresponding to maximum supported SCS value) could be used for checking CPU availability corresponding to different CSI reports associated with different SCS values |
| [8, Samsung] | Proposal 1: At least for PDSCH processing time (N1), PUSCH preparation time (N2) and HARQ-ACK multiplexing timeline (N3), RAN1 strives to define a single value for each timeline per SCS with the consideration of worst case.  Proposal 2: Support SCS-specific K1/K2 by reusing existing default/configured K1/K2 plus a SCS specific offset. |
| [9, CATT] | Proposal 1: Compared with the processing time of 120 KHz SCS, considering the maximum system bandwidth and maximum PRB number can be scheduled, N1/N2 is proposed as follows   * For SCS=480 KHz, the N1/N2 can be 1.5 times as 120 KHz N1/N2 value. * For SCS=960 KHz, the N1/N2 can be 1.25 times as 480 KHz N1/N2 value.   Proposal 2: The range of k1 value specified for PDSCH HARQ process operation for 480 KHz/960 KHz SCS should take the N1 processing time into account with the starting slot from the value.  Proposal 3: The range of k2 value specified for PUSCH process for 480 KHz/960 KHz SCS should take the N2 processing time into account with the starting slot from the value. |
| [10, ZTE] | Proposal 7: For above 52.6GHz, a new UE capability for timeline related aspects should be defined based on slot (or symbol)-group granularity.  Proposal 8: Consider the phase noise estimation and compensation time on timeline design when PTRS is configured.  Proposal 9: The following methods can be considered to interpret k0, k1 and k2, and we prefer Method 1.   * Method 1: slot-group level unit can be defined for the value of k0, k1 and k2, that is the value indicated in the DCI is not the slot offset but the slot group offset. One slot group can include M slots. * Method 2: some new candidate values of k0, k1 and k2 should be defined considering the UE processing capability. * Method 3: the value range of k0, k1 and k2 is not changed and the unit is still the slot, but the actually used k0, k1 and k2 is an offset of the indicated value in the DCI, and the offset value is different for different SCS. |
| [13, Ericsson] | Observation 19 UE PDSCH/PUSCH processing timelines for SCS > 120 kHz need to be tightened compared to those for 120 kHz SCS to enable high performance NR operation in 52.6 to 71 GHz.  Proposal 27 RAN1 should strive to narrow down the range of UE processing latencies as soon as possible, particularly those related PDSCH/PUSCH processing (N1, N2, N3), to enable multi-PDSCH/PUSCH design to proceed. A reasonable starting point for discussion is an exponential function a∙2^(b∙μ) fitted to the Rel-15 values that provides extrapolated values of N1, N2, and N3 for 480 and 960 kHz (µ = 5 and 6, respectively). The actual values to be specified can be discussed on a case-by-case basis. |
| [14, Futurewei] | Proposal 17. The absolute time duration for 120 kHz SCS, which now serves as the upper bound, can be directly used for 480kHz/960kHz SCSs without reductions, at least for the single-PDSCH/PUSCH cases.  Proposal 18. The slot configuration period is reused for 480kHz/960kHz SCS and the number of configuration slots is scaled accordingly. |
| [15, Nokia] | Proposal 13: Increase the maximum number of DL and UL HARQ processes from 16 to 32, for 480 kHz and 960 kHz SCSs.  Table 3. Proposed processing times for PDSCH and PUSCH    Proposal 14: Consider proposing times shown in Table 3 for PDSCH and PUSCH.  Observation 2: CSI computation delay has relation with PDCCH decoding complexity including BD/CCE limit.  Proposal 15: Consider CSI computation delay parameters for new SCSs only after determination of BD/CCE limit for new SCSs.  Observation 3: Rel-15/16 schemes for CPU can be reused for 480kHz and/or 960kHz SCS.  Proposal 16: Deprioritize the discussion on the additional processing timelines below.   * UE PDSCH reception preparation time with cross carrier scheduling with different subcarrier spacings for PDCCH and PDSCH * SRS, PUCCH, PUSCH, PRACH cancellation with dynamic SFI * ZP CSI Resource set activation/deactivation * Application delay of the minimum scheduling offset restriction * timing aspects related to cross carrier operation |
| [18, Qualcomm] | Proposal 12: Revisit K1 values for SCS 480kHz and 960kHz after the discussions on the PDSCH processing timeline.  Proposal 24: The timeline calculations need to take into account the different cases for PDCCH monitoring, i.e., per-slot or multi-slot. This will require either one of the following   * Timeline is calculated based on the worst case * gNB and UE applies different processing timeline depending on PDCCH monitoring periodicity   Proposal 26: RAN1 design for 480kHz and 960kHz SCS, should assume a timeline similar to the absolute timeline of 120kHz. |
| [19, LG] | Proposal #20: Consider additional UE PDSCH processing procedure time (i.e., N1 symbols) when UE is required to perform both of CPE and ICI compensation, e.g., for 120 kHz SCS and 64 QAM.  Proposal #21: Indicated (or configured) value(s) for k0/k1/k2 can be interpreted as multiplied by M where M denotes the number of slots in a slot-group (if configured).  Proposal #22: The configured and default value of k1 (or PDSCH-to-HARQ\_feedback), should be adjusted to practical value considering the increased N1, e.g., ceil(N1/14) or floor(N1/14).  Proposal #23: The configured and default value of k2 should be adjusted to practical value considering the increased N2, e.g., ceil(N2/14) or floor(N2/14).  Proposal #24: The configured value of k0 should be adjusted to practical value considering the UE PDSCH reception preparation time with cross carrier scheduling with different numerologies for PDCCH and PDSCH.  Proposal #25: Consider the dependence of each other when determining the value range of k0 and k1.  Proposal #26: Consider CSI processing timeline enhancements for better availability for CPUs for multiple CSI reports associated with different numerologies. |
| [20, MediaTek] | Proposal 11: Support the absolute processing time duration for 120 kHz SCS as the basic UE capability on the processing timelines for 480 kHz and 960 kHz SCS for NR operation in 52.6 to 71 GHz.   * FFS: the necessity of advanced timelines and the methodology for evaluation if advanced timelines are needed |
| [22, Apple] | Proposal 1: the absolute time duration of 120 kHz is adopted as the timeline for all UE processing timelines under consideration.   * The values of N1, N2, N3, Z1, Z1’, Z2, Z2’, Z3, and Z3’ should be set to the same absolute time as the same timeline for the 120 kHz SCS * Any tighter timelines that are proposed should be based on an additional UE capability.   Proposal 2: there should be a single set of timelines with no need to differentiate between single and multiple PDSCH scheduling.  Proposal 3: discuss and decide the values of k0/k1/k2 after N1/N2/N3 and multi-slot PDCCH monitoring details have been decided. |

### Summary on timeline

#### N1, N2 and N3

[1, Huawei] proposed that for single slot scheduling with 480 kHz and 960 kHz SCS, N1, N2 and N3 values providing same absolute processing time as that of 120 kHz SCS in FR2 is preferred. The values should be further studied for the case of multi slot scheduling after the detailed schemes are clear. Similarly, [14, Futurewei], [18, Qualcomm], [20, MediaTek] and [22, Apple] all proposed to take the same absolute time duration of 120 kHz as the timeline for 480 and 960 kHz.

On the other hand, [13, Ericsson] observed that UE PDSCH/PUSCH processing timelines for SCS > 120 kHz need to be tightened compared to those for 120 kHz SCS to enable high performance NR operation in 52.6 to 71 GHz. Furthermore, [13, Ericsson] took an exponential function a∙2^(b∙μ) fitted to the Rel-15 values that provides extrapolated values of N1, N2, and N3 for 480 and 960 kHz (µ = 5 and 6, respectively) as starting point for discussion.

[15, Nokia] analysed the relationship between UE processing timeline and the number of HARQ process and provided some example values of N1 and N2. [9, CATT] provided their values of N1 and N2 based on an analysis on the impact of channel bandwidth, the number of PRB and LDPC coding to UE processing timeline, where for SCS=480 KHz, the N1/N2 can be 1.5 times as 120 KHz N1/N2 value and for SCS=960 KHz, the N1/N2 can be 1.25 times as 480 KHz N1/N2 value.

Regarding whether the same timeline for single slot scheduling can be applied to multi-PDSCH/PUSCH scheduling, [8, Samsung] proposed that at least for PDSCH processing time (N1), PUSCH preparation time (N2) and HARQ-ACK multiplexing timeline (N3), RAN1 strives to define a single value for each timeline per SCS with the consideration of worst case. Similarly, [22, Apple] proposed there should be a single set of timelines with no need to differentiate between single and multiple PDSCH scheduling. [18, Qualcomm] proposed the timeline calculations need to take into account the different cases for PDCCH monitoring, i.e., per-slot or multi-slot and it proposed two options: timeline is calculated based on the worst case or gNB and UE applies different processing timeline depending on PDCCH monitoring periodicity. On the same topic, [10, ZTE] proposed for above 52.6GHz, a new UE capability for timeline related aspects should be defined based on slot (or symbol)-group granularity.

The proposed values of N1, N2 and N3 from companies are summarized in the following tables.

Table 1 PDSCH processing time arrange for PDSCH processing capability 1

|  |  |  |
| --- | --- | --- |
|  | PDSCH decoding time *N1* [symbols] | |
| *dmrs-AdditionalPosition* = pos0 in  *DMRS-DownlinkConfig* in both of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB* | *dmrs-AdditionalPosition* ≠ pos0 in  *DMRS-DownlinkConfig* in either of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB*  *or if the higher layer parameter is not configured* |
| 3 (120 kHz) | 20 | 24 |
| 5 (480 kHz) | 80 ([1, Huawei], [14, Futurewei], [18, Qualcomm], [20, MediaTek], [22, Apple])  30 ([9, CATT])  37 ([13, Ericsson])  40 ([15, Nokia]) | 96 ([1, Huawei], [14, Futurewei], [18, Qualcomm], [20, MediaTek], [22, Apple])  36 ([9, CATT]) |
| 6 (960 kHz) | 160 ([1, Huawei], [14, Futurewei], [18, Qualcomm], [20, MediaTek], [22, Apple])  42 ([9, CATT])  50 ([13, Ericsson])  80 ([15, Nokia]) | 192 ([1, Huawei], [14, Futurewei], [18, Qualcomm], [20, MediaTek], [22, Apple])  50 ([9, CATT]) |

Table 2 PUSCH preparation time for PUSCH timing capability 1

|  |  |
| --- | --- |
|  | PUSCH preparation time *N2* [symbols] |
| 3 (120 kHz) | 36 |
| 5 (480 kHz) | 144 ([1, Huawei], [14, Futurewei], [18, Qualcomm], [20, MediaTek], [22, Apple])  60 ([9, CATT])  91 ([13, Ericsson])  52 ([15, Nokia]) |
| 6 (960 kHz) | 288 ([1, Huawei], [14, Futurewei], [18, Qualcomm], [20, MediaTek], [22, Apple])  72 ([9, CATT])  144 ([13, Ericsson])  108 ([15, Nokia]) |

Table 3 Minimum gap between the second detected DCI and the beginning of the first PUCCH resources

|  |  |
| --- | --- |
|  | HARQ-ACK multiplexing timeline *N3* [symbols] |
| 3 (120 kHz) | 20 |
| 5 (480 kHz) | 80 ([1, Huawei], [14, Futurewei], [18, Qualcomm], [20, MediaTek], [22, Apple])  37 ([13, Ericsson]) |
| 6 (960 kHz) | 160 ([1, Huawei], [14, Futurewei], [18, Qualcomm], [20, MediaTek], [22, Apple])  50 ([13, Ericsson]) |

Moderator’s comment:

During RAN1#104b-e, there’s a proposal “At least for PDSCH processing time (N1), PUSCH preparation time (N2) and HARQ-ACK multiplexing timeline (N3), RAN1 strives to define a single value for each timeline per SCS. This single value of each timeline per SCS applies to both single PDSCH/PUSCH and multi-PDSCH/PUSCH scheduling for NR operation in 52.6 GHz to 71 GHz.”. No agreement was achieved as some companies don’t agree to such principle without knowing the details of multi-PDSCH/PUSCH scheduling.

During that discussion, one comment questioned the meaning of “single value for each timeline per SCS” and mentioned that there is another set of N1(N2) values for UE capability 2 captured in TS 38.214 Table 5.3-2(6.4-2). It is moderator’s understanding that only UE capability 1 is applicable to FR2 and hence for 480/960 kHz SCS (FR2-2), only PDSCH processing time (N1) for PDSCH processing capability 1 and PUSCH preparation time (N2) for PUSCH timing capability 1 should be defined. To clarify the scope and to align understanding among companies, the following proposal is formulated.

##### Proposal 2-1-1 (closed):

For NR operation in FR2-2 with 480 kHz and/or 960 kHz SCS, value(s) for PDSCH processing time (N1) for PDSCH processing capability 1 and PUSCH preparation time (N2) for PUSCH timing capability 1 are to defined.

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Support the proposal 2-1-1 |
| Qualcomm | We are fine with the proposal |
| Huawei, HiSilicon | The proposal is fine but we already know that we need to define these values, so there is little point in agreeing to the proposal itself, unless we agree with the values at the same time. |
| LG Electronics | We are fine with the proposal |
| Intel | Agree with proposal.  As for the values themselves. We are generally supportive of lower values (compared to what is available for 120kHz). At the same time, we understand this may have hardware implications. Therefore, open for discussions. In case identical time units as 120kHz case needs to be supported, we believe a secondary set of values for more advanced UEs should be then also supported. |
| Futurewei | Support that for PxSCH processing capacity 1, N1 and N2 are to be defined. |
| Moderator | Discussion closed. Please refer to Chair’s note for the relevant agreement. |

Moderator’s comment:

On the values of N1, N2 and N3, majority of companies proposed to take the same absolute time duration of 120 kHz SCS for 480 and 960 kHz without any further reduction. Note that the absolute time duration of 120 kHz SCS has been agreed as the upper bound previously. Formulate the following proposal to have the timeline values at least for single PDSCH/PUSCH scheduling while keep the option open for any additional tightened timeline.

##### Proposal 2-1-2:

For NR operation in FR2-2, adopt the values of N1, N2 and N3 as in the following tables at least for single PDSCH/PUSCH scheduling.

* FFS whether applicable to multi-PDSCH/PUSCH scheduling
* FFS whether to introduce additional UE capability with smaller values considering at least the following factors
  + PDCCH monitoring capability
  + Mix numerology scheduling
  + Multi-PDSCH/PUSCH scheduling
  + Cross-carrier scheduling

Table 2-2.1 PDSCH processing time arrange for PDSCH processing capability 1

|  |  |  |
| --- | --- | --- |
|  | PDSCH decoding time *N1* [symbols] | |
| *dmrs-AdditionalPosition* = pos0 in  *DMRS-DownlinkConfig* in both of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB* | *dmrs-AdditionalPosition* ≠ pos0 in  *DMRS-DownlinkConfig* in either of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB*  *or if the higher layer parameter is not configured* |
| 3 (120 kHz) | 20 | 24 |
| 5 (480 kHz) | 80 | 96 |
| 6 (960 kHz) | 160 | 192 |

Table 2-2.2 PUSCH preparation time for PUSCH timing capability 1

|  |  |
| --- | --- |
|  | PUSCH preparation time *N2* [symbols] |
| 3 (120 kHz) | 36 |
| 5 (480 kHz) | 144 |
| 6 (960 kHz) | 288 |

Table 2-2.3 Minimum gap between the second detected DCI and the beginning of the first PUCCH resources

|  |  |
| --- | --- |
|  | HARQ-ACK multiplexing timeline *N3* [symbols] |
| 3 (120 kHz) | 20 |
| 5 (480 kHz) | 80 |
| 6 (960 kHz) | 160 |

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Support the proposal 2-1-2 |
| Qualcomm | We support the proposal |
| MediaTek | We are supportive to moderator’s proposal in general. In our view, we have following comments and suggestion for modification.   1. For the first FFS, in our understanding, it comes from Huawei, HilSilicon’s Tdoc R1-2106446, where the aspect of the gap between the DMRS location and the ending of the scheduled PDSCH varies with SCSs when multi-PDSCH scheduling is considered as shown in the figure below. Basically, such gap becomes shorter when SCS becomes larger due to the reduced symbol length. In our view, this observation should apply to single scheduled PDSCH as well. Furthermore, R1-2106446 also proposes the processing time should further increase if UE performs joint DMRS detection. In our view, both observation are potentially valid (even though DMRS enhancements are under discussion) and we think those aspects will contribute to longer processing time. 2. For the second FFS, we understand some companies want to reduce the processing timeline further and we are open to discussion. However, the factors listed in the sub-bullets seem to contradict the purpose from a UE vendor’s point of view. In particular, mix-numerology and cross-carrier scheduling should increase the processing complexity instead of reducing it. In fact, in Rel-15/16, both mix-numerology and cross-carrier scheduling have been addressed in the processing time formula specified in clause 5.3 TS 38.214. Furthermore, companies [R1-2107331 Qualcomm] [R1-2107727 Apple] also mention the potential need of studying cross-carrier scheduling, which we also support.   Based on the above comments, we suggest the following modification to the moderator’s proposal: Proposal 2-1-2: For NR operation in FR2-2, adopt the values of N1, N2 and N3 as in the following tables ~~at least~~ for single PDSCH/PUSCH scheduling and multi-PDSCH/PUSCH scheduling.   * ~~FFS whether applicable to multi-PDSCH/PUSCH scheduling~~ * FFS whether to introduce extra processing time in addition to N1, N2 and N3 considering at least the following factors for single and multi-PDSCH/PUSCH scheduling   + Gap between the last DMRS symbol and the ending symbol of PDSCH   + Mix numerology scheduling   + Cross-carrier scheduling   + Joint DMRS detection for multi-PDSCH scheduling * FFS whether to introduce additional UE capability with smaller values considering at least the following factors   + PDCCH monitoring capability   + ~~Mix numerology scheduling~~   + ~~Multi-PDSCH/PUSCH scheduling~~   + ~~Cross-carrier scheduling~~ |
| Huawei, HiSilicon | We support the proposal. |
| LG Electronics | We are generally fine with the proposal and would like to add an FFS.  FFS: Considering UE additional burden for ICI compensation at least at high MCS |
| Intel | While we are not objecting to Proposal 2-1.2, we think the removal of FFS on additional capability is critical issue for agreeing to the proposal. We believe it is technically feasible for certain UEs to support faster processing for 480 and 960kHz (with current state of art implementation), and to only support these cases that are same as 120kHz seem to be limiting technology that can be deployed in 60GHz.  We think the FFS should be removed and agree to supporting additional capability on top of Proposal 2-1.2. |
| Futurewei | Support to adopt values N1, N2, N3 in Table 2-2.1.  Fine with continue study whether additional UE capability is needed considering the aspects listed in the FFS. |
| Moderator | Based on the comments received during GTW session, formulate the following proposal 2-1-2a. |

##### Proposal 2-1-2a (high priority):

For NR operation with 480 and 960 kHz SCS, adopt at least the values of N1, N2 and N3 as in the following tables for single and multi-PDSCH/PUSCH scheduling.

* RAN1 strives to study and introduce additional smaller values for UE capability 1 considering at least the following factors
  + PDCCH monitoring capability
  + Mix numerology scheduling
  + Multi-PDSCH/PUSCH scheduling
  + Cross-carrier scheduling

Table 2-2.1 PDSCH processing time arrange for PDSCH processing capability 1

|  |  |  |
| --- | --- | --- |
|  | PDSCH decoding time *N1* [symbols] | |
| *dmrs-AdditionalPosition* = pos0 in  *DMRS-DownlinkConfig* in both of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB* | *dmrs-AdditionalPosition* ≠ pos0 in  *DMRS-DownlinkConfig* in either of  *dmrs-DownlinkForPDSCH-MappingTypeA*, *dmrs-DownlinkForPDSCH-MappingTypeB*  *or if the higher layer parameter is not configured* |
| 3 (120 kHz) | 20 | 24 |
| 5 (480 kHz) | 80 | 96 |
| 6 (960 kHz) | 160 | 192 |

Table 2-2.2 PUSCH preparation time for PUSCH timing capability 1

|  |  |
| --- | --- |
|  | PUSCH preparation time *N2* [symbols] |
| 3 (120 kHz) | 36 |
| 5 (480 kHz) | 144 |
| 6 (960 kHz) | 288 |

Table 2-2.3 Minimum gap between the second detected DCI and the beginning of the first PUCCH resources

|  |  |
| --- | --- |
|  | HARQ-ACK multiplexing timeline *N3* [symbols] |
| 3 (120 kHz) | 20 |
| 5 (480 kHz) | 80 |
| 6 (960 kHz) | 160 |

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Intel | Ok with proposal 2-1-2a.  On the issue on whether the new values should be considered as capability 2. From our understanding the main difference between capability 1 and 2 is not only the faster timing but also how TBS is handled. For capability 2, gNB configured a specific cell to enable this for the UE, and how peak throughput is handled is quite different (see TS38.214 Section 5.1.3 and 6.1.4). The handling of TBS and per-celll enablement configuration is one of the key differences for capability 2.  Because of this, we think we should still work with capability 1 framework, as capability 2 is not supported for FR2 but only supported in FR1.  So what we are discussing is potentially additional set of values for capability 1. |
|  |  |
|  |  |

#### k0, k1 and k2

[3, vivo] proposed the default set of PDSCH-to-HARQ\_feedback timing (k1) indicator should be adapted to the SCS of PDSCH. Similarly, [19, LG] proposed that the configuration and default value of k1 and k2, should be adjusted to practical value considering the increased N1 and N2 respectively, examples are given as ceil(N1/14) or floor(N1/14) for k1 and ceil(N2/14) or floor(N2/14) for k2. [9, CATT] proposed the range of k1 (k2) value specified for PDSCH (PUSCH) HARQ process operation for 480 kHz/960 kHz SCS should take the N1 (N2) processing time into account with the starting slot/offset from the value ⌊N1/14⌋ (⌊N2/14⌋). [8, Samsung] also proposed to support SCS-specific K1/K2 by reusing existing default/configured K1/K2 plus a SCS specific offset.

[10, ZTE] proposed multiple methods to interpret k0, k1 and k2 where their preferred method is to define slot-group level unit for the value of k0, k1 and k2, that is the value indicated in the DCI is not the slot offset but the slot group offset where one slot group can include M slots. [19, LG] proposed that the indicated (or configured) value(s) for k0/k1/k2 can be interpreted as multiplied by M where M denotes the number of slots in a slot-group (if configured).

[1, Huawei] proposed value range of k0 and k2 considering scaled TDD configuration and non-continuous resource mapping in time domain. [1, Huawei] also proposed values of k1 for DCI format 1\_0, 1\_1 and 1\_2 separately. [9, CATT] thought the range of K0 value should not be changed for 480 kHz and 960 kHz SCS. While [19, LG] proposed the configuration and default value of k0 should be adjusted to practical value considering the UE PDSCH reception preparation time with cross carrier scheduling with different numerologies for PDCCH and PDSCH.

[18, Qualcomm] proposed to visit K1 values for SCS 480kHz and 960kHz after the discussions on the PDSCH processing timeline while [22, Apple] proposed to discuss and decide the values of k0/k1/k2 after N1/N2/N3 and multi-slot PDCCH monitoring details have been decided.

Proposed values of k0, k1 and k2 are summarized in the following table.

Table 4 k0, k1 and k2 values

|  |  |  |
| --- | --- | --- |
| **Notation** | **Range** | **Default value** |
| k0 | * Option 1: 0 ~ 128 for 480 kHz, 0 ~ 256 for 960 kHz ([1, Huawei]) * Option 2: 0 ~ 32 ([9, CATT]) |  |
| k1 | * Option 1 ([1, Huawei]):   for DCI format 1\_0: {4, 8, 12, 16, 20, 24, 28, 32} for 480 kHz and {8, 16, 24, 32, 40, 48, 56, 64} for 960 kHz  for DCI format 1\_1: -1~63 for 480 kHz and -1~127 for 960 kHz  for DCI format 1\_2: 0~63 for 480 kHz and 0~127 for 960 kHz   * Option 2 ([3, vivo], [8, Samsung], [9, CATT], [19, LG]): existing range + offset where offset is ceil(N1/14) or floor(N1/14) |  |
| k2 | * Option 1 ([1, Huawei]): 0 ~ 128 for 480 kHz, 0 ~ 256 for 960 kHz * Option 2 ([8, Samsung], [9, CATT], [19, LG]): existing range + offset where offset is ceil(N2/14) or floor(N2/14) | * ([8, Samsung], [9, CATT], [19, LG]):   ceil(N2/14) or floor(N2/14) |

Moderator’s comment:

There’s proposal to defer the discussion due to relationship between some of the values of k0/k1/k2 to UE processing time (N1/N2/N3). Although it may be difficult to agree upon value ranges of k0/k1/k2, it may be useful to see whether we can keep the definition/interpretation of k0/k1/k2. Formulate the following proposal on the definition of k0/k1/k2.

##### Proposal 2-2:

Keep the existing definition of k0, k1 and k2 for FR2-2. That is

* the value of k0 indicates the slot offset between DCI and its scheduled PDSCH in number of slots
* the value of k1 indicates the slot offset between PDSCH and corresponding HARQ-ACK in number of slots
* the value of k2 indicates the slot offset between DCI and its scheduled PUSCH in number of slots

Companies are encouraged to provide comments to above proposal 2-2 and/or potential agreeable proposals on the value ranges and/or default values for k0, k1 and k2.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Support the proposal 2-2 |
| Qualcomm | We are okay with proposal, we would like to add  FFS: extending the range of values of k0/k1/k2 for SCS 480kHz/960kHz |
| Huawei, HiSilicon | We support the proposal and would prefer to have another discussion on the range of values of k0/k1/k2 rather than having an FFS, or otherwise add a note (if this was Qualcomm’s intent):  *Note: the range of values of k0/k1/k2 for SCS 480kHz/960kHz is to be further discussed, and it should be discussed separately for DCI format 1\_0 and DCI format 1\_1* |
| LG Electronics | We agree with the proposal. Qualcomm’s FFS is also fine. |
| Intel | Ok with Proposal 2-2. |
| Futurewei | The definitions in Proposal 2-2 needs to be clearer, since there can be seperate k0’s, k1’s, and k2’s for multiple PxSCH. Consider specify that these ki’s indicate slot offset(s) between DCI and its scheduled PDSCH(s) in a multi-slot. |
| Moderator | Wording update based on comments received during GTW session into proposal 2-2a. |

##### Proposal 2-2a (high priority):

* For single PDSCH/PUSCH scheduling, keep the existing definition of k0, k1 and k2 for NR operation with 480 and 960 kHz SCS. That is
  + the value of k0 indicates the slot offset between DCI and its scheduled PDSCH in number of slots
  + the value of k1 indicates the slot offset between PDSCH and corresponding HARQ-ACK in number of slots
  + the value of k2 indicates the slot offset between DCI and its scheduled PUSCH in number of slots
* FFS the definitions for multi-PDSCH/PUSCH scheduling

Companies are encouraged to provide comments to above proposal and/or potential agreeable proposals on the value ranges and/or default values for k0, k1 and k2.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Intel | Ok with Proposal 2-2a |
|  |  |
|  |  |

#### Z1, Z2 and Z3

[1, Huawei] proposed that for 480 kHz and 960 kHz SCS, Z1, Z2 and Z3 values providing same absolute processing time as that of 120 kHz SCS in FR2 is preferred. [18, Qualcomm] proposed that RAN1 design for 480kHz and 960kHz SCS, should assume a timeline similar to the absolute timeline of 120kHz.

[15, Nokia] thought CSI computation delay has relation with PDCCH decoding complexity including BD/CCE limit and proposed to consider CSI computation delay parameters for new SCSs only after determination of BD/CCE limit for new SCSs.

Moderator’s comment:

Similar to the case of N1 and N2, current specification defines two CSI computation delay requirement captured in TS 38.214 Table 5.4-1 and 5.4-2, where the CSI computation delay requirement 1 in NR is defined for a very restricted/simplistic scenario in which only wideband CQI corresponding to up to 4 CSI-RS port in a single CSI resource without CRI report is requested and only single-panel codebook is configured.

It is moderator’s understanding that CSI computation delay requirement 2 is applicable to FR2-2. To clarify the scope and to align understanding among companies, the following proposal is formulated.

##### Proposal 2-3-1 (closed):

For NR operation in FR2-2 with 480 kHz and/or 960 kHz SCS, value(s) for CSI computation delay requirement 2 are to be defined.

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Support the proposal 2-3-1 |
| Qualcomm | We are okay with the proposal |
| Huawei, HiSilicon | The proposal is fine but we already know that we need to define these values, so there is little point in agreeing to the proposal itself, unless we agree with the values at the same time. |
| LG Electronics | We are fine with the proposal. |
| Intel | We would be ok to accept the proposal 2-3-1. |
| Futurewei | Agree that the CSI computation delay requirement 2 is applicable to FR2-2. |
| Moderator | Discussion closed. Please refer to Chair’s note for the relevant agreement. |

Moderator’s comment:

On the values of Z1, Z2 and Z3, with very limited input on these values, it is not easy to derive any agreeable values. Two approaches can be considered:

1. Choose the values of Z1/Z2/Z3 for 480 and 960 kHz SCS to maintain the same absolute time duration as that of 120 kHz SCS in FR2. The logic is similar to the case of N1/N2/N3 and also considering the relevant agreement of UE reported capability *beamReportTiming* and *beamSwitchTiming* (both are related to CSI computation time as captured in TS 38.214 Table 5.4-2) for 480 and 960 kHz are scaled from that of 120 kHz SCS.
2. Defer the discussion/decision of Z1/Z2/Z3 values until the details of other aspects (e.g., PDCCH monitoring capability, multi-PDSCH/PUSCH scheduling) are clear.

##### Discussion point 2-3-2:

Companies are encouraged to provide comments and/or proposals.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We have preference for the 1st approach where the absolute time duration is same as that of 120kHz SCS in FR2 |
| Qualcomm | We prefer the 1st approach |
| MediaTek | We prefer the 1st approach |
| Huawei, HiSilicon | We also prefer the first approach |
| LG Electronics | We prefer the 1st approach |
| Intel | We are ok with approach 2. As for approach 1, if we are going to take similar case as N1/N2/N3 then we should consider additional UE capability for this as well. |
| Futurewei | Ok with deferring the issue. |
| Moderator | Based on the above provided majority view in comments, formulate the following. |

##### Proposal 2-3-2:

For NR operation with 480 and 960 kHz SCS, adopt at least the values of Z1, Z2 and Z3 as in the following table for single and multi-PDSCH/PUSCH scheduling to maintain the same absolute time duration as that of 120 kHz SCS in FR2.

* Note: is UE reported capability *beamReportTiming*; KB3 and KB4 is UE reported capability *beamSwitchTiming* for 480 and 960 kHz SCS respectively.
* RAN1 strives to study and introduce additional smaller values for CSI computation delay requirement

Table 2-4. CSI computation delay requirement 2

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | *Z1* [symbols] | | *Z2* [symbols] | | *Z3* [symbols] | |
| *Z1* | *Z'1* | *Z2* | *Z'2* | *Z3* | *Z'3* |
| 3 | 97 | 85 | 152 | 140 | min(97, *X*3+ KB2) | *X*3 |
| 5 | 388 | 340 | 608 | 560 | [min(388, *X*5+ KB3)] | [*X*5] |
| 6 | 776 | 680 | 1216 | 1120 | [min(776, *X*6+ KB4)] | [*X*6] |

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Moderator | “[]” are put for Z3 and Z’3 values for now pending the decision of any additional *beamReportTiming* and/or *beamSwitchTiming* other than those scaled values from that of 120 kHz SCS. |
|  |  |
|  |  |

#### Other issue(s)

Several contributions mentioned some other issues related to timelines.

[7, Lenovo] raised an issue and thought it is critical to handle CPU availability check for UEs when it is required to process multiple CSI reports associated with different SCS values ranging from 15kHz to 960kHz in a parallel manner. It proposed same reference symbols duration (possibly the shortest duration corresponding to maximum supported SCS value) could be used for checking CPU availability corresponding to different CSI reports associated with different SCS values. Regarding CSI processing unit (CPU), [15, Nokia] argued that CPU is the UE capability for simultaneous CSI calculations which is indicated as and is related to channel variation or UE mobility rather than scheduling/subcarrier spacings. Therefore, there is no reason to increase the frequency of CSI reporting or rule for calculation of CSI occupancy. Given is independent from numerology, [15, Nokia] proposed that the existing specification can be reused for 480kHz and 960kHz SCS.

[14, Futurewei] proposed the slot configuration period in UL/DL configuration is reused for 480kHz/960kHz SCS and the number of configuration slots is scaled accordingly.

Moderator’s comment:

With limited input on these issues, suggest companies to study further and provide input to discuss.

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Indication of number of CPUs is UE capability, however the intervals at which CPU availability is checked is related to symbol duration. Now, with the introduction of higher SCS up to 960kHz, the CPU availability check with 960kHz and 480kHz can be much more frequent in comparison to lower SCS. Therefore, the absolute opportunities could vary quite significantly. Therefore, the proposal to have same intervals/granularity for CPU availability check regardless of SCS should be supported.  Also, this is quite a simple enhancement and doesn’t impact how the actual processing timeline, but just fairer in terms of CPU availability check for all SCS values. |
| Futurewei | Ok with further study. |
|  |  |

## 2.3. PTRS

### Individual observations/proposals

The following are individual observations/proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [1, Huawei] | Observation 8: Block PTRS with the designed circular sequence has better BLER and spectrum efficiency than distributed PTRS when power boosting is applied.  Proposal 14: Support block PTRS as one type of PTRS pattern for 120 kHz, 480 kHz and 960 kHz SCS of CP-OFDM. The use of block PTRS can be indicated by MCS, scheduled bandwidth, and power boosting scheme. The PTRS sequence is composed of ZC sequence and circular part based on ZC sequence for block PTRS.  Observation 9: With more PTRS groups and less PTRS samples per PTRS group denoted as (, ) = (16, 2), the BLER performance of all the SCSs are improved significantly.  Proposal 15: A new PTRS pattern with more PTRS groups and less PTRS samples per PTRS group denoted as (, ) = (16, 2) within one DFT-s-OFDM symbol should be supported for large scheduling bandwidth and high scheduled MCS.  Observation 10: Due to Rx timing shift, (at least part of) a PTRS group placed at the tail of the transmitter’s DFT-s-OFDM symbol, may wrap-around to the head of the symbol from the receiver’s perspective, thus spoiling the original intention of the design and unnecessarily increasing Rx complexity, as well as deteriorating PN compensation performance, especially for the high MCS.  Observation 11: New PTRS location which is in the middle of each interval can solve the influence on BLER performance caused by Rx advance timing shift.  Proposal 16: For PTRS with , the mapping of last PTRS group should consider potential Rx timing shift and avoid the last X pre-DFT symbol(s). |
| [2, Mitsubishi] | [Observation 1: In bands above 52.6GHz, the ICI component of the phase noise becomes predominant on CPE.](#_Toc77780148)  [Observation 2: Distributed PT-RS pattern shows poor performance results with CPE phase noise estimation, regardless of the PT-RS pattern density.](#_Toc77780149)  [Observation 3: For a distributed PT-RS pattern, at small carrier allocations, the performance is poor even with de-ICI filtering, due to an insufficient number of PT-RS samples. Increasing the distributed pattern density partially improves the situation, but cyclic block patterns still yield better results.](#_Toc77780150)  [Observation 4: For a distributed PT-RS pattern, de-ICI Wiener filtering outperforms CPE in all cases, but high MCS still not reach FER=0.1.](#_Toc77780151)  [Observation 5: Distributed PT-RS patterns are not robust enough to ensure system performance in bands above 52.6GHz, especially with high MCS and/or at 70GHz.](#_Toc77780152)  [Observation 6: For a similar overhead, block PT-RS (with any ordinary non-cyclic sequence) is outperformed by distributed PT-RS pattern when a same de-ICI Wiener filter is used at the receiver side. There is no interest in supporting block non-cyclic sequences.](#_Toc77780153)  [Observation 7: PT-RS blocks with a ZP pattern outperforms the distributed PT-RS pattern, even with dense distributed patterns.](#_Toc77780154)  [Observation 8: Block PT-RS with cyclic sequence significantly outperforms the distributed PT-RS pattern with ICI compensation. The gain increases with the carrier frequency.](#_Toc77780155)  [Observation 9: Block PT-RS with cyclic sequence outperforms block PT-RS with ZP pattern.](#_Toc77780156)  [Observation 10: Block PT-RS with cyclic sequence requires lower complexity phase noise compensation filtering than the de-ICI filter needed for the distributed PT-RS pattern.](#_Toc77780157)  Proposal 1: Support block PT-RS with cyclic sequence for OFDM waveform. FFS exact sequence.  Proposal 2: A PT-RS sequence for OFDM waveform composed of KP samples includes a cyclic prefix of floor(KP/2) samples.  Proposal 3: Support density extension of current Rel.15 PT-RS for DFTsOFDM waveform. |
| [3, vivo] | Observation 1:   * The performance of de-ICI (3-tap filter) with K\_PTRS = 2 is worse than K\_PTRS = 1 or K\_PTRS = 0.5 when PDSCH RB number <= 16; * When PDSCH RB number <= 16, CPE only with K\_PTRS = 2 has much better performance than de-ICI with K\_PTRS = 1 or K\_PTRS = 0.5. * For all evaluated cases, the preferred method for PN compensation (with the best performance) is shown in Table 4. The best performance is obtained with legacy PTRS density in frequency, i.e. K\_PTRS = 2. There’s no motivation to justify higher PTRS density in frequency domain for small RB allocation.   Table 4 Preferred PN compensation method when number of RB <=32   |  |  |  |  |  | | --- | --- | --- | --- | --- | | SCS (kHz)/MCS | 7 | 16 | 22 | 26 | | 120 | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | no method to achieve 10% BLER. | | 480 | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | If PDSCH RB num <= 16, use CPE only (K\_PTRS=2); else, use de-ICI (K\_PTRS=2). | | 960 | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | CPE only (K\_PTRS=2) | If PDSCH RB num <= 16, use CPE only (K\_PTRS=2); else, use de-ICI (K\_PTRS=2). |   Proposal 1: There is no need to introduce higher PTRS frequency density as K\_PTRS = 1 or K\_PTRS = 0.5 for NR operation in 52.6 to 71 GHz in Rel-17.  Observation 2: With current simulation parameters, the performance of de-ICI with Rel-15 PTRS pattern outperforms the performance of block-based PTRS pattern with cyclic ZC sequence.  Proposal 2: Do not support block-based PTRS pattern with cyclic ZC sequence for NR operation in 52.6 to 71 GHz in Rel-17.  Observation 3: For block-based PTRS pattern with zero-power RE, the performance of ‘6dB power boosting’ is around 2.5 dB worse than that of ‘full power boosting’ for SNR achieving 10% BLER.  Proposal 3: Do not support block-based PTRS pattern with zero-power RE for NR operation in 52.6 to 71 GHz in Rel-17.  Observation 4: For MCS-7, MCS-16 and MCS-22, the performance gap is less than 0.8 dB between (CN, CS) = (8, 4) and the configuration with the best performance.  Observation 5: For MCS-26 and PUSCH RB number as 256, configuration (CN, CS) = (16, 4) achieves best performance.  Proposal 4: The necessity to introduce more PTRS chunk number needs further discussion as there is no significant performance benefit. If a new configuration with more PTRS chunk number needs to be added, the SCS and MCS should be within the condition of applying this configuration. |
| [5, InterDigital] | Proposal 18: Rel-17 NR operation in 52.6-71 GHz follow Rel-15/Rel-16 PT-RS design, at least when allocated RBs > 32.  Proposal 19: The need of PT-RS enhancement for small RB allocation (< 32 RBs) should be carefully evaluated. |
| [8, Samsung] | Observation 1: At 60GHz, two block PTRS patterns with ICI approximation filter show some performance gain comparing to Rel-15 PT-RS with de-ICI algorithm. The gains are widened at 70GHz.  Observation 2: Block PTRS patterns 2 (cyclic PTRS sequence with 3dB power boost) provides better performance than block PTRS pattern 1 (patterns with ZP tones in both side) at 10% target BLER. The performance order reverses at 1% target BLER.  Proposal 3: Support block PTRS patterns can be considered for further performance improvement and UE complexity reduction comparing to legacy PTRS.  Observation 3: For small RB allocations (32RB/16RB/8RB) and legacy PTRS frequency density (K=2 and K=4), CPE compensation outperforms the one with ICI compensation.  Observation 4: For 16 RBs and 8RBs allocations, K=1 configuration provides better performance compared with legacy PTRS frequency density.  Proposal 4: For 16RB and 8RB allocations, support K=1 for performance improvement. |
| [9, CATT] | Proposal 19: For NR operation in 52.6 to 71 GHz with OFDM, PTRS enhancement is not supported. |
| [10, ZTE] | Observation 1: When PRB number is not larger than 32, CPE compensation with lower PTRS density can achieve similar or better performance than ICI compensation with higher PTRS density.  Proposal 10: Do not increase PTRS frequency density for small RB allocations for CP-OFDM.  Observation 2: Block PTRS with cyclic sequence cannot provide performance gain compared with legacy PTRS.  Observation 3: Block PTRS with power boosting cannot achieve better performance than legacy PTRS.  Proposal 11: Reuse the Rel-15 legacy PTRS pattern for 52.6GHz~71GHz.  Observation 4: Increasing PTRS groups for DFT-s-OFDM waveform can bring benefit to performance of 120kHz SCS and MCS 22.  Proposal 12: Support to increase the number of PTRS groups for DFT-s-OFDM. |
| [13, Ericsson] | **Observation 20 Even for small RB allocation, enhanced PTRS structure with K = 1 or K=0.5 does not provide additional performance gain over the existing Rel-15 PTRS structure (K = 2 and K=4).**  **Observation 21 For every tested scenario, Rel-15 PTRS + direct de-ICI receiver with multiple settings for the PTRS density can be used to outperform the best settings for square and orthogonal circulant PTRS with square and orthogonal circulant ICI filter approximation without significant phase noise compensation complexity increase or even decreased phase noise compensation complexity.**  **Observation 22 For every tested scenario, best setting for orthogonal circulant PTRS with 3 dB power boosting does not provide additional gain over the best setting for existing Rel-15 PTRS structure + direct de-ICI receiver.**  **Observation 23 The performance of square and orthogonal ICI filter approximation is worse than Rel-15 PTRS structure with direct de-ICI filtering because of the various fundamental design issues identified in Annex A:**  **1. ICI filter approximation with block PTRS does not fully utilize all received PTRS symbols.**  **2. Phase noise compensation with ICI filter approximation approach relies on an auto-deconvolution assumption that is not valid in practice.**  **3. The construction of a circulant matrix with cyclic block PTRS sequence relies on an assumption that is invalid for frequency selective channels.**  **4. The approximate filter estimation with circulant PTRS matrix involves anti-match-filter combining, which amplifies noises from clusters and subcarriers with weak received SNR.**  **Observation 24 The ICI filter approximation receiver with single-tone PTRS (see Annex A.5) requires excessive power boosting which can result in both substantial link performance losses and severe out-of-band intermodulation leakages.**  Proposal 28 Retain the same Rel-15 distributed PTRS design for OFDM for all RB allocations. Additional PTRS structure(s) are not needed.  Observation 25 Complexity of ICI mitigation is dominated by frequency domain de-ICI filtering. Matrix inversion constitutes no more than 2% of the total complexity for realistic filter lengths and PXSCH allocations. |
| [14, Futurewei] | Observation 1. For PDSCH with 120kHz SCS, de-ICI does not necessarily work better than de-CPE method for cases when the number of RBs is small, e.g., 8 or 16.  Observation 2. For PDSCH with 120kHz SCS, increasing the density of PTRS to (K=0.5, L=1) does not provide performance gain, while increasing the density of PTRS to (K=1, L=1) can provide performance gain over the current maximum allowed density (K=2, L=1) for cases when the number of RBs is small, e.g., 8, 16, or 32.  Proposal 1. For PDSCH with 120kHz SCS and a small number of RBs, consider increasing the density of PTRS to (K=1, L=1).  Observation 3. For PDSCH with 480kHz/960kHz SCS, de-CPE mostly works better than de-ICI counterparts for BLER performance.  Proposal 2. For PDSCH with 480kHz/960kHz SCS and a small number of RBs, consider reuse the legacy PTRS density of (K=2, L=1) (de-CPE is enough compared to de-ICI).  Observation 4. For each SCS with 64QAM, the PTRS density (Ng = 16, Ns = 4, L = 1) offers better performance than the legacy density, although the gain is more notable for the smaller SCS. For each SCS with 16QAM, the PTRS density (Ng = 16, Ns = 4, L = 1) has only comparable performance with legacy density (Ng = 8, Ns = 4, L = 1). For QPSK, it is possible that the legacy density provides the best performance, e.g., for the 960kHz SCS case.  Proposal 3. Increasing PTRS density to (Ng = 16, Ns = 4, L = 1) can be considered for PUSCH in B52/FR2-2 if 64QAM is used; for lower order modulations such as 16QAM and QPSK, the legacy density (Ng = 8, Ns = 4, L = 1) offers fine performance, thus can be reused. |
| [15, Nokia] | Observation 4. Existing PTRS configurations provide good allocation flexibility to achieve good performance for any bandwidth, SCS, or MCS.  Observation 5. Considerable benefit from increasing PTRS density to K=1 is observed only in a single case when high-order modulation is used and PRBs=16 and ICI compensation is used.  Observation 6. No gain is achieved using K=0.5.  Observation 7. Using small PRB allocations with high MCSs is a corner case and should not be considered to motivate new PTRS configurations  Proposal 17. Do not consider increasing frequency density for small PRB allocations (<32).  Proposal 18: Consider introducing a PTRS mapping unit in terms of fraction or multiple of DFTsOFDM symbols, to flexibly control PTRS overhead and allocation.  Observation 8. PUSCH performance of DFT-s-OFDM may be improved by increasing the maximum number of PTRS groups with well affordable PTRS overhead.  Observation 9. New PTRS configurations can give performance gains for high order modulations.  Observation 10. Performance can be significantly improved by combinations of existing PTRS patterns.  Proposal 19. Consider increasing number of PTRS groups for DFT-s-OFDM to make high order modulations robust to phase noise when a large number of PRBs is used.  Proposal 20. If 48 PTRS REs are being considered enough for maximum PTRS overhead, consider supporting the new PTRS configurations as combinations of existing PTRS configurations to a single configuration. |
| [18, Qualcomm] | Observation 1: Comparing the different PTRS patterns   * The best performance is obtained with block PTRS pattern with zero-power tones. * The legacy pattern performance is very close to block PTRS pattern with zero-power tones.   Observation 2: The block PTRS pattern with ZP tones and the legacy pattern outperform the cyclic patterns based on ZC sequences.  Observation 3: With 7 clusters each with 9 tones, 8 ZP PTRS tones and a single NZP tone in the centre, the two algorithms with the clustered pattern have almost the same performance, and they slightly outperform the legacy pattern.  Observation 4: With 7 clusters each with 9 tones, 8 ZP PTRS tones and a single NZP tone in the centre, power boosting the NZP tone by 6 dB can matches the performance in of the legacy PTRS pattern.  Observation 5: For clustered PTRS pattern with ZP tones, power boosting NZP tones will not increase CM or PAPR.  Observation 6: For small RB allocation, e.g., 16 or 8 RBs, sending the PTRS over every RB, i.e., K=1, enhances the performance as it helps in having more accurate ICI filter calculations or CPE estimates. In addition, the performance is degraded when the density is increased with K=0.5 due to the large overhead and increase coding rate.  Observation 7: For MCS 22, there is no significant enhancement for increasing the total number of PTRS samples to 64, while small gains can be observed with MCS 24. In addition, increasing the number of PTRS samples beyond 64 is not helping the performance.  Observation 8: With total of 16 samples, the pattern with 8 chunks outperforms the one with 4 chunks, i.e., distributing samples over time domain enhances the performance, but still the legacy pattern with 32 samples is outperforming.  Proposal 1: For SCS 120kHz, the complexity of phase noise ICI compensation and its effects on the UE processing timeline need to be considered.  Proposal 2: Support introducing a new PTRS pattern, clustered based with ZP tones, to reduce the ICI compensation complexity.  Proposal 3: As PTRS enhancement for assisting ICI compensation, increasing the frequency domain density, of Rel. 15 PTRS, for small RB allocation can be considered. |
| [19, LG] | Proposal #16: Retain the existing distributed PT-RS structure for all SCS in FR2-2. It seems that further improvement either by advanced estimation algorithms or by new PT-RS pattern cannot achieve a noticeable improvements.  Observation #2: Based on the performed evaluation research, PTRS frequency density K=0.5 or 1 does not provide enough performance gain, or provide marginal gain by 0.1 dB in very specific situations.  Proposal #17: Do not support K=0.5 and K=1  Observation #3: Complexity analysis of the de-ICI filtering approaches has shown that the main contribution to the overall number of operations comes from the application of the filter and not from the taps estimation procedure. Thus, for the advanced Nulling (or zero-padded) PTRSs scheme, the computation gain with respect to the baseline Rel-15 is typically less than 3%. |
| [21, Intel] | Proposal 11: RAN1 to introduce UE capability of supporting high MCS/rank combinations in FR2-2. Details of the capability signal is FFS.  Observation 1: De-ICI filtering performance can be improved by using conjugate anti-symmetric filter.  Observation 2: De-ICI filtering performance can be improved by using CP-based linear phase ramp pre-compensation.  Observation 3: De-ICI performance can be improved by applying the unit-magnitude de-ICI compensation in time domain.  Observation 4: all the MCSs can be supported with rank 1 without any enhancements in the specification with advanced PN compensation technique.  Observation 5: MCSs up to MCS22 for CP-OFDM can be supported with rank 2 and SCS120kHz using frequency domain de-ICI filtering.  Observation 6: MCSs up to MCS25 for CP-OFDM can be supported with rank 2 and SCS120kHz using the combination of CP-based pre-compensation, conjugate antisymmetric de-ICI filter property and the unit-magnitude de-ICI compensation in time domain.  Observation 7: MCS26 for CP-OFDM and above cannot be supported with rank 2 and SCS120kHz by any means of a realistic UE implementation.  Observation 8: MCSs up to MCS24 for CP-OFDM can be supported with rank 2 and SCS960kHz using frequency domain de-ICI filtering.  Observation 9: MCSs up to MCS26 for CP-OFDM can be supported with rank 2 and SCS960kHz using the combination of CP-based pre-compensation, conjugate antisymmetric de-ICI filter property and the unit-magnitude de-ICI compensation in time domain.  Observation 10: MCS27 and above cannot be supported with rank 2 and SCS960kHz by any means of a realistic UE implementation for CP-OFDM.  Proposal 12: Adopt block PT-RS pattern for use in FR2-2.  Observation 11: 6dB PT-RS power boosting improves the MCS22 PN compensation performance from 0 to 0.7 dB depending on PT-RS block size.  Proposal 13: RAN1 to continue studying PT-RS power boosting aspects.  Observation 12: Unequal distribution of PN estimation error among DFT-s-ODFM samples may lead to systematic unbalance between code blocks’ BLERs.  Observation 13: PUSCH PTRS patterns with only 4 and 8 PTRS groups provide acceptable performance with 120kHz SCS.  Observation 14: Code blocks interlacing within a DFT-s-OFDM symbol provides performance gain from 0.5dB to 1.7dB at MCS22.  Proposal 14: RAN1 to consider code blocks interlacing for PUSCH with transform precoding. |
| [22, Apple] | Observation 1: At lower SNRs, there is a trade-off between the overhead of the PTRS selected and the throughput. Achieving the best throughput performance requires a lower value of K (K =1 ) than is currently available in the Rel-15 specification.  Proposal 7: RAN1 should support K = 1 for smaller frequency allocation sizes for PTRS in CP-OFDM. |

### Summary on PTRS

#### For CP-OFDM

In RAN1#104-e meeting, the following was agreed.

* At least existing PTRS design for CP-OFDM is supported for NR operation in 52.6 to 71 GHz.
* Companies are encouraged to study the need of potential PTRS enhancement for CP-OFDM with respect to phase noise compensation performance considering at least the following aspects:
  + PTRS density/pattern (e.g. distributed, block-based) and sequence (e.g. cyclic sequence)
  + Frequency domain power boosting and its impact to PDSCH performance and PDSCH to DMRS EPRE
  + Receiver complexity, including possible aspects related to supporting both existing PTRS design and potential PTRS enhancement
  + Possible specification impact of supporting potential PTRS enhancement in addition to existing PTRS design
  + Note: PTRS overhead should be accounted for in the evaluations, e.g. by showing spectral efficiency results and/or reporting effective coding rate

The following sources submitted to this meeting evaluated and compared different PN compensation performance using the existing Rel-15 NR distributed PTRS structure against new PTRS patterns and/or new sequence.

[1, Huawei] compared BLER performance of Rel-15 PTRS with K=4 and a block PTRS with cyclic sequence when ICI PN compensation is used. When a 3dB power boosting was applied in the simulation for both PTRS patterns, it observed a performance gain for block PTRS with cyclic sequence compared to Rel-15 PTRS with K=4.

Moderator’s observations from the reported numerical results: the performance gain (for 10% BLER target) is shown to be 0.2~0.4 dB for large RB allocation (256 RB for 120 and 480, 160 RB for 960 kHz) with MCS 22. The gain increased to 1.5~3 dB as the number of RB allocation decreased to 64 for MCS 22. When a 3dB power boosting was applied in the simulation for block PTRS pattern but not for Rel-15 PTRS, it reported at least 0.7dB gain of block PTRS with cyclic sequence when scheduled bandwidth is 128RB.

[2, Mitsubishi] compared phase noise compensation performance for the following cases with 120 kHz SCS: CPE-based for Rel-15 PTRS, de-ICI for Rel-15 PTRS, de-ICI for block PTRS, de-ICI for ZP block PTRS and ICI filtering for block PTRS with cyclic sequence. It is observed that for a similar overhead, block PTRS (with any ordinary non-cyclic sequence) is outperformed by distributed Rel-15 PTRS pattern when a same de-ICI filter is used at the receiver side. It also observed that with de-ICI, PTRS blocks with a ZP pattern outperforms the distributed Rel-15 PTRS pattern. Furthermore, it observed that ICI filtering for block PTRS with cyclic sequence outperforms de-ICI for block PTRS with ZP pattern.

It is stated in [2, Mitsubishi] that “for medium MCS we observe gains in order of 1-2dB for FER target 10-1” and “for high MCS, in some scenarios only block PT-RS with cyclic sequence reaches target FER of 10-1”.

[3, vivo] compared CP-OFDM performance for CPE with Rel-15 PTRS, de-ICI (5-tap) filter with Rel-15 PTRS, de-ICI (5-tap) with a block PTRS with cyclic ZC sequence for 120 kHz SCS. When 3 dB power boosting is applied to PTRS for all three schemes, it observed that the performance of de-ICI with Rel-15 PTRS pattern outperforms (~1 dB at 10% BLER target for different DS observed based on the reported results in table 6 in [3]) the performance of block-based PTRS pattern with cyclic ZC sequence. [3, vivo] also evaluated performance for a block PTRS with ZP. It observed that a significant performance loss for block PTRS of 7 clusters with 9 tones (8 ZP and 1 NZP) when power boosting is 6 dB for that 1 NZP RE compared to full power boosting.

[8, Samsung] compared the performance of three schemes: Rel-15 PTRS pattern with K=4 and no power boosting for PTRS, block PTRS with zeros tones and , with 9.54dB power boosted for NZP-PTRS, and block PTRS with cyclic sequence and , with 3dB power boosted for PTRS. For the case evaluated (120 kHz SCS with 256 RB, TDL-A 5 ns, MCS22, 60 GHz), it observed performance gain about 0.5~0.6 dB for both block PTRS patterns for 10% BLER target.

[10, ZTE] evaluated PDSCH with CP-OFDM performance with the legacy PTRS and block PTRS with cyclic ZC sequence for 120 and 480 kHz SCS with MCS 22. The evaluation was performed with different ICI estimation filter tap number, block number and sequence length for each block. It is observed that the performance of ICI compensation based on legacy PTRS is always better than block PTRS with cyclic sequence. It also compared the performance of block PTRS with 3dB power boosting with that of legacy PTRS without power boosting and showed that the performance of legacy PTRS without power boosting is still better than block PTRS with 3 dB power boosting.

[13, Ericsson] provided evaluation results on clustered-PTRS with cyclic sequence and investigated power boosting aspects for 120 KHz SCS with MCS 22. Comparing the performance of Rel-15 PTRS and a block-PTRS with cyclic sequence, it is observed that for every tested scenario, Rel-15 PTRS + direct de-ICI receiver with multiple settings for the PTRS density can be used to outperform (about 0.5 ~ 1 dB gain observed based on the reported results in table 10 to 13 in [13]) the best settings for square and orthogonal circulant PTRS with square and orthogonal circulant ICI filter approximation without significant phase noise compensation complexity increase or even decreased phase noise compensation complexity. Regarding power boosting, it observed that for every tested scenario, best setting for orthogonal circulant PTRS with 3 dB power boosting does not provide additional gain over the best setting for existing Rel-15 PTRS structure + direct de-ICI receiver. Finally, with respect to block PTRS with ZP, it is observed that the ICI filter approximation receiver with single-tone PTRS requires excessive power boosting which can result in both substantial link performance losses and severe out-of-band intermodulation leakages.

[13, Ericsson] observed that complexity of ICI mitigation is dominated by frequency domain de-ICI filtering. Matrix inversion constitutes no more than 2% of the total complexity for realistic filter lengths and PXSCH allocations.

[13, Ericsson] also observed that the performance of square and orthogonal ICI filter approximation is worse than Rel-15 PTRS structure with direct de-ICI filtering due to various identified issues: ICI filter approximation with block PTRS does not fully utilize all received PTRS symbols; phase noise compensation with ICI filter approximation approach relies on an auto-deconvolution assumption that is not valid in practice; the construction of a circulant matrix with cyclic block PTRS sequence relies on an assumption that is invalid for frequency selective channels; ICI filter approximation with circulant PTRS matrix involves anti-match-filter combining, which amplifies noise from clusters and subcarriers with weak received SNR. On the issues identified above, [2, Mitsubishi] provided counter arguments to issue 3 (channel equalization) and issue 4 (average over PTRS blocks) and claimed issue 3 and 4 are solved.

[18, Qualcomm] evaluated ICI compensation performance for 120 kHz SCS at MCS 22/24/26 with multiple PTRS patterns: clustered PTRS with different number of ZP tones, block PTRS with cyclic sequence and Rel-15 PTRS with K=4. It observed that the best performance is obtained with block PTRS pattern with zero-power tones and the legacy pattern performance is very close to block PTRS pattern with zero-power tones (about 0~0.3 dB gap for 10% BLER target observed based on the reported results in table 2 and 3 in [18]). It also observed that block PTRS pattern with zero-power tones and the legacy pattern outperforms (about 0.1 ~ 0.2 dB for 10% BLER target with MCS 22 and about 0.3 ~ 0.4 dB for MCS 24/26 based on the reported results in table 2 and 3 in [18]) the cyclic patterns based on ZC sequences.

It observed that with 7 clusters each with 9 tones, 8 ZP PTRS tones and a single NZP tone in the center, power boosting the NZP tone by 6 dB can matches the performance of the legacy PTRS pattern. Furthermore, it observed that for clustered PTRS pattern with ZP tones, power boosting NZP tones will not increase CM or PAPR. It then proposed to introduce a new PTRS pattern, clustered based with ZP tones, to reduce the ICI compensation complexity.

[19, LG] compared the performance difference between ideal cases (no PN or ideal filter estimation) and de-ICI and CPE-only compensation based on Rel-15 PTRS for all SCSs with MCS 22 and showed that the potential performance gain by advanced estimation algorithms or by new PT-RS pattern is well bounded (< 1 dB). [19, LG] also looked at the computational complexity aspect and observed that for de-ICI filtering approaches, the main contribution to the overall number of operations comes from the application of the filter and not from the taps estimation procedure. Thus, for the advanced Nulling (or zero-padded) PTRSs scheme, the computation gain with respect to the baseline Rel-15 is typically less than 3%.

[21, Intel] compared two PN compensation methods: PN spectrum-based and direct de-ICI filter coefficients estimation with different PTRS block sizes for 120 kHz with MCS 22 and 24. It observed that the performance of PN-spectrum based estimation algorithm drastically varies among the PTRS block sizes. It showed that PN-spectrum based approach is inferior to the direct one at the small PT-RS block sizes, while it outperforms the competing algorithm at large PTRS blocks. However, for large PT-RS block size, it is observed that PN-spectrum based approach is not the overall winner in a fading channel (TDL-A). It also observed that in almost flat LoS channel (TDL-E, optional channel for evaluation), the PN-spectrum based algorithm can significantly (~1.5dB at MCS22) outperform the direct coefficients estimation.

[21, Intel] argued that given grouping PT-RS tones into blocks is required for PN spectrum-based de-ICI filter estimation and LoS condition is common in mmWave communication, block PTRS should be supported in FR2-2. Note in their evaluation, the original Rel-15 PTRS Gold sequence was used. It also observed that 6 dB PTRS power boosting improves the MCS22 PN compensation performance from 0 to 0.7 dB depending on PTRS block size.

Summary of observations:

* Comparing block PTRS with cyclic sequence against Rel-15 PTRS
  + Under the same power condition (i.e., no or the same value of power boosting) for PTRS
    - 2 sources ([1, Huawei], [2, Mitsubishi]) showed notable (> 0.5 dB for 10% BLER target) performance gain
    - 4 sources ([3, vivo], [10, ZTE], [13, Ericsson], [18, Qualcomm]) showed notable (> 0.5 dB for 10% BLER target) performance loss
  + When 3 dB power boosting is applied to block PTRS with cyclic sequence but not to Rel-15 PTRS
    - 2 sources ([1, Huawei], [8, Samsung]) showed notable (> 0.5 dB for 10% BLER target) performance gain
    - 2 sources ([10, ZTE], [13, Ericsson]) showed performance loss for block PTRS with cyclic sequence against Rel-15 PTRS. The performance gap is about 0.1 ~ 1 dB for 10% BLER target for different scenarios.
* Comparing block PTRS with ZP tones against Rel-15 PTRS under the condition of the same total power for PTRS
  + 2 sources ([2, Mitsubishi], [8, Samsung]) showed notable (> 0.5 dB for 10% BLER target) performance gain
  + 1 source ([18, Qualcomm]) showed minor (~0.3 dB for 10% BLER target) performance gain
  + 1 source ([3, vivo]) showed minor (0.2~0.4 dB for 10% BLER target) performance loss
* Regarding ICI computation complexity aspect
  + 4 sources ([1, Huawei], [2, Mitsubishi], [8, Samsung], [18, Qualcomm]) showed the benefit of cyclic sequence or ZP tones
  + 2 sources ([13, Ericsson], [19, LG]) counter argued and stated that the computation gain of cyclic sequence or ZP tones are < 3% of the total complexity of ICI mitigation
* Regarding power boosting for block PTRS with ZP tones
  + 1 source ([18, Qualcomm]) showed power boosting the NZP tone by 6 dB can matches the performance of the legacy PTRS pattern
  + 1 source ([3, vivo]) showed notable (> 0.5 dB for 10% BLER target) performance loss for block PTRS of 7 clusters with 9 tones (8 ZP and 1 NZP) when power boosting is 6 dB for that 1 NZP RE compared to full power boosting which is still worse than legacy PTRS
  + 1 source ([13, Ericsson]) argued that the ICI filter approximation receiver with single-tone PTRS requires excessive power boosting which can result in both substantial link performance losses and severe out-of-band intermodulation leakages.
  + 1 source ([18, Qualcomm]) showed power boosting NZP tones will not increase CM or PAPR for clustered PTRS pattern with ZP tones

Based on the contributions, companies’ view to support block PTRS with cyclic sequence are summarized below.

Yes: [1, Huawei] (ZC sequence and circular part based on ZC sequence), [2, Mitsubishi] (a sequence of KP samples includes a cyclic prefix of floor(KP/2) samples), [8, Samsung] (no preference indicated for sequence)

No: [3, vivo], [9, CATT], [10, ZTE], [13, Ericsson], [18, Qualcomm], [19, LG]

Based on the contributions, companies’ view to support block PTRS with ZP tones are summarized below.

Yes: [8, Samsung], [18, Qualcomm]

No: [3, vivo], [9, CATT], [10, ZTE], [13, Ericsson], [19, LG]

Based on the contributions, companies’ view to support block PTRS are summarized below.

Yes: [8, Samsung], [21, Intel]

No: [3, vivo], [9, CATT], [10, ZTE], [13, Ericsson], [19, LG]

Moderator’s comment:

Looking at the available evaluation results and views expressed from contributions, it’s clear that companies have split views on whether there’s performance gain of block PTRS, the sequence of PTRS and in general the benefit/necessity of PTRS enhancement for CP-OFDM.

Given that companies have had at least two meetings to consider, evaluate and debate the proposed PTRS enhancement, and that there has not been a shift in company positions to form a clear majority for any of the proposed schemes, moderator don’t see a chance for an agreement on any of the schemes yet. With that, moderator suggest companies continue discussion to see if any new aspects/arguments can be identified in this meeting. Otherwise, it’d be better to conclude and close the discussion point considering limited time of this WI.

##### Discussion point 3-1-1:

Companies are encouraged to provide comments and/or potential agreeable proposal if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Agree with the moderator’s comment that if no consensus can be reached by end of this meeting, then this discussion should be closed |
| Qualcomm | We support introducing the new block PTRS pattern with ZP tones to reduce the complexity of filter coefficient calculations  The ICI compensations consists of two steps   1. Filter coefficient estimation 2. Applying the filter coefficient on rx tones   The second step is common between different algorithms and patterns and there are multiple ways to implement such vector multiplication efficiently  The complexity of the first step differs based on the algorithm and the pattern; therefore it should have higher impact of the decision among the different patterns. |
| Huawei, HiSilicon | More discussion would be useful first to understand the discrepancy among the evaluation results provided by different companies. For example, we noticed that in Ericsson’s evaluations the performance of Rel-15 PTRS (red curves) is different in Figures 12 and 26, whereas the same evaluation assumptions are applied. In the same figures, the performance of “orthogonal circulant, K=2 eq., L=3” is also different (black curve in Fig 14 vs. blue curve in Fig 26). |
| LG Electronics | Agree with the moderator’s comment that if no consensus can be reached by end of this meeting, then this discussion should be closed.  Regarding the complexity, the filter tap estimation has relatively small portion of overall complexity and main computational load comes from applying the filter, so the computation gain of cyclic sequence or ZP tones is not significant. |
| Futurewei | Since comb-PTRS does not guarantee to lead to the best performance in all cases, it is restrictive to disallow block-PTRS. There is possibility that there exists new sequences that work better with block-PTRS. Therefore, we would like to keep block-PTRS a viable choice. |
| Intel | Disagree with Moderator’s comment about closing the discussion if no consensus is reached this meeting.  We think the source of discrepancy among the companies’ evaluation results and views is that many companies evaluate block PT-RS with non-optimal block size and with non-optimal de-ICI filter estimation algorithm. The results in our Tdoc shows that the different choice of the combination of these two can lead to the opposite conclusions. Also, we found that block PT-RS pattern has more advantage in the channel with low frequency selectivity, e.g., a LoS channel. In our view, having block PT-RS performance gain just in LoS is enough to justify its adoption, because LoS links are common in mmWave communication.  To overcome the split between companies’ views, we propose to agree on the set of assumptions focused specifically on block PT-RS evaluation:   1. Make a LoS channel model mandatory for block PTRS evaluations. 2. Compare Rel-15 PTRS with direct de-ICI filter estimation algorithm to block PTRS of the block size *NB* ~ 40 with PN-based coefficients estimation algorithm. 3. Use high MCS with rank 2 as a focus area of PT-RS enhancements evaluation.   We encourage companies to evaluate block PT-RS till the next meeting using these assumptions. If no substantial performance gain is observed by the companies with this setup, the discussion should be closed at the next meeting. |

##### Discussion point 3-1-2:

[21, Intel] observed that de-ICI filtering performance could be improved via several receiver implementation based PN compensation methods. It then evaluated performance of high MCS for rank 1 and rank 2 using existing PTRS with direct de-ICI filter estimation. The following are observed.

* All the MCSs can be supported with rank 1 without any enhancements in the specification with advanced PN compensation technique.
* MCSs up to MCS22 for CP-OFDM can be supported with rank 2 and SCS120kHz using frequency domain de-ICI filtering.
* MCSs up to MCS25 for CP-OFDM can be supported with rank 2 and SCS120kHz using the combination of CP-based pre-compensation, conjugate antisymmetric de-ICI filter property and the unit-magnitude de-ICI compensation in time domain.
* MCS26 for CP-OFDM and above cannot be supported with rank 2 and SCS120kHz by any means of a realistic UE implementation.
* MCSs up to MCS24 for CP-OFDM can be supported with rank 2 and SCS960kHz using frequency domain de-ICI filtering.
* MCSs up to MCS26 for CP-OFDM can be supported with rank 2 and SCS960kHz using the combination of CP-based pre-compensation, conjugate antisymmetric de-ICI filter property and the unit-magnitude de-ICI compensation in time domain.
* MCS27 and above cannot be supported with rank 2 and SCS960kHz by any means of a realistic UE implementation for CP-OFDM.

In summary, [21, Intel] observed that high MCSs may require a combination of several receiver implementation techniques to be supported with rank 2 Tx and some MCSs may not be supported in a practical implementation at all. Therefore, it proposed to introduce UE capability of supporting certain high MCS/rank combinations in FR2-2.

A similar point has been made in [18, Qualcomm] that “define a UE capability to support the high MCS that requires ICI compensation” as phase noise ICI compensation has some computation complexity which may affect timeline for 120 kHz SCS.

Moderator’s comment:

Although briefly touched upon during previous discussion in RAN1#104b-e, this issue has not been extensively discussed. Suggest other companies to provide input for discussion.

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We see the merit of limiting certain higher MCS/rank in FR2-2 (based on UE capability) and are open to further discuss this. |
| Huawei, HiSilicon | Rather than putting such restriction, we should ensure that the design provides the possibility for a UE receiver that can effectively handle phase noise and support all MCS supported by the specs. |
| Futurewei | As this is observed by one company and it seems reasonable to limit higher MCS or rank for FR2-2, we suggest to further study. |
| Intel | We agree with HW that RAN1 should enable UEs to support as high MCS as possible by providing the needed features in the spec. However, our evaluation results give us enough confidence that support of at least MCS26-28 with rank-2 & 120kHz is very unlikely (at least by the means of PT-RS enhancements we discuss today in the WI).  Figure 4.1-4 of our Tdoc R1-2107581 contains “ideal de-ICI” curves. They correspond to using the PN realizations passed through the ideal high-pass filter with the stopband width equal to de-ICI filter bandwidth *BA* = SCS ‧ (2*u*+1). It’s intended to model a de-ICI filter with perfectly estimated taps, fully suppressing low frequency PN components within *BA*. Even this kind of perfect 7-tap filter cannot achieve 10% BLER at an SNR below 40dB when MCS26 is used with rank 2 & 120kHz. This isn’t likely to change by any PT-RS enhancement that improves the filter estimation.  So, in our view there will be some set of high MCSs that is not likely to be supported with rank 2 anyway, therefore the need for the UE capability is already clear. Of course, the upper bound of the potentially achievable MCS depends on the agreed PT-RS enhancements and could be discussed further. |
|  |  |

#### For small RB allocation with CP-OFDM

In RAN1#104b-e meeting, the following was agreed.

* In Rel-17, for NR operation in 52.6 – 71 GHz, conclude that increased PTRS frequency density is not supported for CP-OFDM at least for Rel-15 PTRS pattern when the allocated number of RB > 32
* Companies are encouraged to study whether to increase PTRS frequency density for small RB allocations for CP-OFDM for NR operation in 52.6 to 71 GHz with respect to phase noise compensation performance
  + CPE and ICI PN compensation
    - Note: Results for CPE compensation-only are to be reported for reference
  + (K = 0.5, L = 1), (K = 1, L = 1), (K = 2, L = 1),
    - Note: PTRS per K number of PRBs, and PTRS every L number of OFDM symbols
  + Number of RBs: 8, 16, 32
  + Other values of K and number of RBs are not precluded
* Study on other aspects of potential PTRS enhancement (e.g., decreased PTRS frequency density) is not precluded

On this subject, the following sources submitted to this meeting evaluated and compared different frequency density of Rel-15 PTRS pattern with different PN compensation schemes for small RB allocation.

[3, vivo] evaluated and compared the performance of different PTRS density (K=0.5, 1 and 2) with de-ICI (3 taps) and CPE only PN compensation methods with different number of PDSCH RB allocation and different MCS for all SCSs. It observed that while increased PTRS density (K = 0.5 or 1) may help improve the performance of de-ICI compared to K =2 when PDSCH RB number <= 16, a better performance is obtained for CPE only with K = 2 in this case. Given de-ICI with increased density (K = 0.5 or 1) is not the PN compensation method providing the best performance in any of the evaluated cases, it proposed not to increase PTRS density.

[8, Samsung] compared the performance of different PTRS density (K=1, 2 and 4) with de-ICI (3 taps) and CPE only PN compensation for 120 kHz SCS with MCS 22. It observed that for small RB allocations (32RB/16RB/8RB) and legacy PTRS frequency density (K=2 and K=4), CPE compensation outperforms the one with ICI compensation. It also observed that for 16 RBs and 8RBs allocations, K=1 configuration provides better performance for CPE compensation (for 10% BLER target, 1.5 dB gain reported at 8 RB and 2.1 dB gain reported at 16 RB) compared with legacy PTRS frequency density (K =2 and 4).

[10, ZTE] compared the performance of different PTRS density (K=0.5, 1 and 2) with de-ICI and CPE only PN compensation methods for small RB allocations. It observed when PRB number is not larger than 32, CPE compensation with lower PTRS density can achieve similar or better performance than ICI compensation with higher PTRS density.

[13, Ericsson] provided evaluation results on increased PTRS density for small RB allocation. It is observed that even for small RB allocation, enhanced PTRS structure with K = 1 or K=0.5 does not provide additional performance gain over the existing Rel-15 PTRS structure (K = 2 and K=4).

[14, Futurewei] observed that for most cases of PDSCH with 120/480/960 kHz SCS, de-ICI does not necessarily work better than de-CPE method for cases when the number of RBs is small. It observed a performance gain of 1 dB for (K=1, L=1) over (K=2, L=1) with 32 RB for 120 kHz SCS with MCS 22 and 5-tap de-ICI. No gain is observed for (K=1, L=1) for 8 and 16 RB. It proposed to support (K=1, L=1) for 120 kHz SCS with small RB allocation.

[15, Nokia] evaluated different PTRS density for small RB allocation. It observed benefit from increasing PTRS density to K=1 only in a single case when high-order modulation is used and PRBs=16 and ICI compensation is used. It observed no gain is achieved using K=0.5. Further, it argued that using small PRB allocations with high MCSs is a corner case and should not be considered to motivate new PTRS configurations.

[18, Qualcomm] evaluated PN compensation performance for 120 kHz SCS at MCS 22 and MCS 24 with multiple PTRS densities. It observed that for small RB allocation, i.e., 16 or 8 RBs, K=1 enhances the performance while the performance degrades for K=0.5. The performance gain of K=1 for 10% BLER target was reported as 0.5 dB for 8 RB with MCS 22, 0.2 dB for 16 RB with MCS 24 and 0.4 dB for 16 RB with MCS 24. The performance gain of K=1 for 1% BLER target was reported as 4.5 dB for 8 RB with MCS 22, 2.9 dB for 8 RB with MCS 24, 0.6~0.7 dB for 16 RB with MCS 22 and MCS 24.

[19, LG] compared the performance for different PTRS densities for small RB allocation. It observed that PTRS frequency density K=0.5 or 1 does not provide enough performance gain, or provide marginal gain by 0.1 dB in very specific situations.

[22, Apple] compared the performance for different PTRS densities for 480 kHz SCS with MCS 22 and 16 RB. It is observed there is an improvement in BLER performance with increased PTRS density while K = 1 has the highest spectral efficiency compared with K = 0.5 and K = 2 at low SNR. The performance gain of K=1 is > 1dB (moderator’s reading from Figure 7 in [22]) for 10% BLER target and <0.5 dB (moderator’s reading from Figure 8 in [22]) for spectral efficiency.

Companies’ results showing significant performance gain of increased PTRS density (i.e., K=1) for small RB (<=32) allocation are summarized below.

Yes: [8, Samsung] (for 120 kHz with MCS 22), [14, Futurewei] (for 120 kHz with 32 RB and MCS 22), [18, Qualcomm] (for 120 kHz with MCS 22 and 24), [22, Apple] (for 480 kHz with 16 RB and MCS 22)

No: [3, vivo], [10, ZTE], [13, Ericsson], [15, Nokia], [19, LG]

Companies’ view to support increased PTRS density (K=1) for small (<= 32) RB allocation are summarized below.

Yes: [8, Samsung], [14, Futurewei] (for 120 kHz only), [18, Qualcomm], [22, Apple]

No: [3, vivo], [10, ZTE], [13, Ericsson], [15, Nokia], [19, LG]

Moderator’s comment:

Compared to RAN1#104b-e, more evaluation results are submitted. Looking at the available evaluation results from contributions, the performance gain of K=1 are shown for some cases (e.g., small RB (<=32) allocation with high order modulation) by some sources while other sources showed no performance gain at all for those cases. Companies still have split views on whether there’s performance gain of increased PTRS density (K=1) for small RB allocation and hence no consensus to support K=1. Note that, this has already been extensively evaluated for two meetings.

Moderator suggest companies continue discussion to see if any new aspects/arguments can be identified to shift company views in this meeting. Otherwise, it’d be better to conclude and close the discussion point by extending the conclusion agreed in RAN1#104b-e to cover small RB allocation. That is, in Rel-17, for NR operation in FR2-2, conclude that increased PTRS frequency density for Rel-15 PTRS pattern is not supported for CP-OFDM when the allocated number of RB <= 32.

##### Discussion point 3-2:

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Agree with the moderator’s comment that if no consensus can be reached by end of this meeting, then this discussion should be closed |
| Qualcomm | We observe a significant gain from increasing the density to K=1 for small RB allocation, therefore, we support introducing K=1 for small RB allocations |
| LG Electronics | Agree with the moderator’s comment |
| Futurewei | It is fine to reuse the legacy PTRS density for small RB allocation cases. While it is better to allow K=1 for these cases given that there are evaluation results that show the performance gains. |
| Intel | We support increasing PT-RS frequency density to K=1. |

#### For DFT-s-OFDM

In RAN1#104b-e meeting, the following was agreed.

Continue study at least the following aspects for potential PTRS enhancement for DFT-s-OFDM for NR operation in 52.6 to 71 GHz

* The need of potential PTRS enhancement
* PTRS pattern with more PTRS groups within one DFT-s-OFDM symbol when a large number of PRBs is scheduled
  + (Ng = 8, Ns = 4, L = 1), (Ng = 16, Ns = 2, L = 1), (Ng = 16, Ns = 4, L = 1),
  + Note: Ng number of PT-RS groups, Ns number of samples per PT-RS group, and PTRS every L number of DFT-s-OFDM symbols
  + Other patterns are not precluded
* Other aspects of PTRS enhancements are not precluded from further study

The following contributions submitted to this meeting evaluated and studied on the need of potential PTRS enhancement for DFT-s-OFDM.

[1, Huawei] evaluated a new PTRS pattern with more PTRS groups within one DFT-s-OFDM symbol. It is observed that BLER performance of high MCS (e.g, MCS 22 and MCS 26) with large scheduled bandwidth can be improved by using a new pattern with more PTRS groups within one DFT-s-OFDM symbol. The performance gain of (Ng = 16, Ns = 2, L = 1) compared to (Ng = 8, Ns = 4, L = 1) is about 2.8, 1.4 and 0.2 dB for 120, 480 and 960 kHz SCS respectively with large RB allocation (256 RB for 120 and 480, 160 RB for 960 kHz) with MCS 22.

[3, vivo] compared PUSCH performance of DFT-s-OFDM with different PTRS configurations for 120 kHz SCS. It is observed that for MCS-7, MCS-16 and MCS 22, the performance gain of increasing PTRS chunk number is small (<0.8 dB). The gain is more noticeable for MCS 26 and with large RB allocation (e.g 256). However, a question on the motivation of PTRS enhancement for DFT-s-OFDM is raised in [3, vivo] when it is observed that DFT-s-OFDM is mainly used for UL coverage, it is unlikely that very high MCS, such as MCS 26, is typically used with DFT-s-OFDM.

[10, ZTE] evaluated DFT-s-OFDM PUSCH performance of 120 kHz with 64QAM and showed a gain (~0.5 dB for 10% BLER target and ~2 dB for 1% BLER target) at MCS 22 with TDL-A 10 ns.

[14, Futurewei] observed that for each SCS with 64QAM, the PTRS density (Ng = 16, Ns = 4, L = 1) offers better performance than the legacy density, although the gain is more notable for the smaller SCS. It then proposed to consider increasing PTRS density to (Ng = 16, Ns = 4, L = 1) for PUSCH in B52/FR2-2 if 64QAM is used; for lower order modulations such as 16QAM and QPSK, the legacy density (Ng = 8, Ns = 4, L = 1) offers fine performance, thus can be reused.

[15, Nokia] evaluated PUSCH performance of DFT-s-OFDM with different PTRS configurations and showed performance improvement of 64QAM with 120 kHz SCS by two different approaches: introducing a PTRS mapping unit in terms of fraction or multiple of DFT-s-OFDM symbols; increasing number of PTRS groups for DFT-s-OFDM to make high order modulations robust to phase noise when a large number of PRBs is used.

[18, Qualcomm] compared PUSCH performance of DFT-s-OFDM with different number of PTRS samples for 120 kHz SCS and observed no significant gain for increasing the total number of PTRS samples to 64 for MCS 22, while small gains (~0.2 dB for 10% BLER) for MCS 24. In addition, increasing the number of PTRS samples beyond 64 is not helping the performance.

[21, Intel] evaluated PUSCH performance of DFT-s-OFDM with different PTRS configurations and showed that PUSCH PTRS patterns with only 4 and 8 PTRS groups provide acceptable performance with 120kHz SCS.

Companies’ results showing notable performance gain of new PTRS configuration with more PTRS groups within one DFT-s-OFDM symbol when a large number of PRBs is scheduled with high MCS are summarized below.

Yes: [1, Huawei], [3, vivo] (for MCS 22 and 26 only), [10, ZTE], [14, Futurewei], [15, Nokia]

No: [18, Qualcomm]

Companies’ view to support new PTRS configuration with more PTRS groups within one DFT-s-OFDM symbol when a large number of PRBs is scheduled are summarized below.

Yes: [1, Huawei], [2, Mitsubishi], [10, ZTE], [14, Futurewei] (for 64QAM only), [15, Nokia]

No: [3, vivo], [18, Qualcomm]

Moderator’s comment:

Compared to RAN1#104b-e, more evaluation results are submitted. Majority of evaluation results showed some performance gain of (Ng = 16, Ns = 2, L = 1) for large RB allocation and high order MCS. Although the motivation question still holds on this PTRS enhancement for DFT-s-OFDM, suggest the following to see if companies can agree to move forward.

##### Proposal 3-3-1:

* For NR operation in FR2-2 with DFT-s-OFDM, support (Ng = 16, Ns = 2, L = 1) for large RB allocation and high order MCS.
  + Note: Ng number of PT-RS groups, Ns number of samples per PT-RS group, and PTRS every L number of DFT-s-OFDM symbols
  + FFS applicable to which RB allocation(s)
  + FFS applicable to which high order MCS(s)

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We are okay to support the proposal |
| Qualcomm | The overall performance with the legacy pattern of (Ng = 32, Ns = 4, L = 1) is better than the proposed pattern (Ng = 16, Ns = 2, L = 1). Therefore, we do not see a need to introduce such pattern. |
| Huawei, HiSilicon | We support proposal 3-3-1 |
| LG Electronics | Although the evaluation results differ from company to company, the more PTRS groups in a symbol show slightly better performance under specific conditions (e.g., high MCS). However, the method of making a more PTRS group varies from company to company, choosing a specific method: (Ng = 16, Ns = 2, L = 1) may be a hasty decision. In addition, it seems that the necessity of using high MCS in DFT-s-OFDM transmission should be clearly explained first. |
| Futurewei | For the number of PTRS group, support to increase to the maximal to Ng = 16. For the number of PTRS samples, further evaluation is suggested to verify if a lower density Ns = 2 is always better than a higher density Ns = 4. |
| Intel | We agree with Futurewei that more detailed comparison of (16,2) and (16,4) patterns is needed. Since each pattern can perform better than another in different conditions, the main applicability conditions should be clarified for 16 group PT-RS pattern. |

##### Discussion point 3-3-2:

[1, Huawei] also brought up another issue of PTRS group placement for PTRS with It observed that due to Rx timing shift, (part of) a PTRS group placed at the tail of the transmitter’s DFT-s-OFDM symbol, may wrap-around to the head of the symbol from the receiver’s perspective, thus deteriorating PN compensation performance. It then proposed for PTRS with , the mapping of last PTRS group should consider potential Rx timing shift and avoid the last X pre-DFT symbol(s).

Moderator’s comment:

Currently, it is a single company proposal. Suggest other companies to study further on this and provide input for discussion.

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Intel | We have done the study of this aspect and provided the details in our revised Tdoc R1-2108334 (Sec. 4.2.3). We compare edge-aligned versions of (8,4) and (16,2) PT-RS patterns (1st and last groups are at the symbol edges) vs center-aligned versions of those patterns (uniform groups placement at the center of each MPUSCH / Ng sample range). The evaluation shows that center-aligned patterns can outperform the edge-aligned ones by ~4dB at MCS25 within the typical Rx timing shift range 0 < Δt < 20% CP.  We support the proposal to adopt the center-aligned version of (8,4) pattern. We also think that in case (16,2) pattern will be adopted, it should be its center-aligned version.  This issue more prominent for larger subcarrier spacing as we expect relatively higher variability between received signals (from timing advance quantization error, tx transmit timing error, etc) with larger subcarrier from UEs in uplink. |
|  |  |
|  |  |

##### Discussion point 3-3-3:

One contribution mentioned an issues related to PTRS for DFT-s-OFDM.

It is observed in [21, Intel] that due to code block concatenation, unequal distribution of PN estimation error among DFT-s-ODFM samples may lead to systematic unbalance between code blocks’ BLERs. It also showed performance gain from 0.5dB to 1.7dB for code block interlacing within a DFT-s-OFDM symbol at MCS22. It then proposed to consider code block interlacing for PUSCH with transform precoding.

Moderator’s comment:

Again, right now, it is a single company proposal. The proposal itself seems not proposing some PTRS enhancement but rather on bit/symbol mapping of code block. Suggest the proponent company to clarify and other companies to provide input for discussion.

Companies are encouraged to provide comments.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Qualcomm | This proposal requires a lot of changes and is mainly related to rate match and CB mapping as mentioned by the moderator. Given the limited progress we have made so far, such discussion should be avoided during this release. |
| Futurewei | Agree with the FL’s view that the issue is not directly related to PTRS enhancement. |
| Intel | Although the proposed method is indeed not a PT-RS enhancement, it has substantial effect on PT-RS pattens’ PN compensation performance. For example, the use of per-OFDM symbol CBs interlacing allows to support the full range of MCSs with 960kHz SCS using the existing (8,4) PT‑RS pattern. So, in our view its natural to discuss it together with PT-RS pattern enhancements, because it can affect the PT-RS pattern choice.  In our revised Tdoc R1-2108334 (Sec. 4.2.2) we provide the evaluation of per-OFDM symbol CBs interlacing across different PT-RS patterns, MCSs, SCSs and FDRAs. We can confirm that CBs interlacing provides performance gain in all the tested scenarios with zero increase of PT-RS overhead. The gain is pretty large in high data rate scenario (up to 10dB with (8,4) pattern, up to 3dB with (16,2) pattern at MCS27).  We encourage companies to cross-check our evaluations and provide their view on the details of the interlacing procedure (i.e., block interleaver depth, interlacing of CBs of unequal size etc.). |

## 2.4. DMRS

### Individual observations/proposals

The following are individual observations/proposals from the contributions.

|  |  |
| --- | --- |
| Sources | Observations/proposals |
| [1, Huawei] | Observation 7: For 480 kHz and 960 kHz, bundling DMRS in one slot per multi-slot outperforms the legacy DMRS pattern mapped per slot.  Proposal 13: Support DMRS mapped on symbol l0 to symbol l0+S\*L-1 within the first PDSCH slot for the multi-slot scheduling, when only front-loaded DMRS is configured, where L is the length and l0 the starting symbol of legacy front-loaded DMRS. |
| [3, vivo] | Observation 6:   * Comparing with legacy pattern (type-1 with FD-OCC), ‘type-1 no FD-OCC’ has obvious performance gain for DS >= 20ns; * ‘DMRS on every RE with FD-OCC’ has better performance than ‘Type-1 with FD-OCC’ and ‘Type-1 no FD-OCC’, and the performance between DMRS on every RE with/without FD-OCC is very close; * ‘Type-1 no FD-OCC’ and ‘DMRS on every RE with FD-OCC’ still support 2-port transmission, which can be used for MU-MIMO or 2-layer transmission for single UE; * ‘Type-1 no FD-OCC’ still supports data multiplexing in DMRS symbols, while ‘DMRS on every RE’ can’t support this. * ‘Type-2 no FD-OCC’ has better performance than ‘Type-2 with FD-OCC’, and the gain on SCS-960KHz is higher than the gain on SCS-480KHz; * The performance of ‘Type-2 no FD-OCC’ is a little worse than that of ‘Type-1 no FD-OCC’.   Proposal 5: Support ‘type-1 no FD-OCC’ for NR operation in 52.6 to 71 GHz with 480 kHz and 960 kHz SCS in Rel-17.  Proposal 6: Do no introduce new DMRS pattern with increased frequency domain density (in number of subcarriers) than the existing DMRS patterns for NR operation in 52.6 to 71 GHz with 480 kHz and/or 960 kHz SCS in Rel-17. |
| [5, InterDigital] | Observation 1: Type-2 DM-RS shows performance loss due to insufficient RS density in low SNR.  Observation 2: Type-1 DM-RS shows performance loss due to FD-CDM in nonconsecutive REs.  Observation 3: Dynamic switching between the existing pattern and DM-RS with enhanced density provides best performance.  Proposal 1: Support proposed DM-RS pattern with dynamic switching for PDSCH and PUSCH with larger SCSs.  Observation 4: Dynamic switching can be achieved by utilizing reserved values for antenna port(s) indication table in DCI.  Proposal 2: Support the updated antenna port(s) indication table for enhanced density DM-RS. |
| [7, Lenovo] | Observation 1: For higher SCS values such as 480kHz and 960kHz, BLER performance difference between the ideal channel estimation and real channel estimation varies for different SCS values, where, as the subcarrier spacing is increasing, the performance degradation with real channel estimation also increases which could be attributed to the performance of DM-RS configuration with different SCS values  Proposal 10: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, new DM-RS configurations should be supported with following criterion:   * High frequency density of the DM-RS for high SCS for better channel estimation when channel coherence bandwidth is less than the configured SCS * Reduced number of DM-RS ports as the performance gain of high rank MIMO channels is expected to be limited in this FR   Proposal 11: For supporting NR between 52.6 GHz and 71 GHz with high subcarrier spacing values including 480kHz and 960kHz, it should be agreed to not support FD-OCC for DMRS type 1 and type 2 configuration and maximum number of orthogonal DMRS ports are reduced   * DMRS type 1:   + 1-symbol: No FD-OCC, maximum # of DMRS ports is 2   + 2-symbol: No FD-OCC, maximum # of DMRS ports is 4 * DMRS type 2:   + 1-symbol: No FD-OCC, maximum # of DMRS ports is 3   + 2-symbol: No FD-OCC, maximum # of DMRS ports is 6 |
| [8, Samsung] | Proposal 5: Support FD-OCC disable applicable to certain DMRS indication value by RRC configuration.  Proposal 6: Support DMRS overhead reduction in time domain and DMRS bundling across multiple PDSCH/PUSCHs. |
| [9, CATT] | Proposal 16: Use existing DMRS patterns for NR operation in 52.6 to 71 GHz; new DMRS pattern with increased frequency domain density is not supported.  Proposal 17: Additional potential DMRS enhancement for multi-PDSCH/PUSCH scheduling is not supported.  Proposal 18: The reserved states in the "Antenna port(s)" field can be used to indicate the FD-OCC off state for rank -1. |
| [10, ZTE] | Observation 5: With the same total RS power, Rel-15 DMRS Type 1 pattern and the new DMRS pattern that fully occupied in frequency domain show comparable performance.  Proposal 13: Reuse the Rel-15 legacy DMRS pattern for 52.6GHz~71GHz.  Proposal 14: Support to use the reserved bit to indicate whether FD-OCC is applied. |
| [13, Ericsson] | Proposal 29 For DMRS-Type 1 for 480 and 960 kHz SCS, support a method for rank-1 transmission that enables the UE to assume that all the remaining orthogonal antenna ports within a CDM group are not associated with transmission of PDSCH to another UE. Further discuss whether or not an RRC parameter is needed to enable this. |
| [15, Nokia] | Observation 11: Existing RAN1 specification provides support for flexible configuration of different DMRS antenna ports belonging into same or different CDM groups for rank-1 and rank-2.  Observation 12: For rank-1, type-1 and new type (“comb-1”) w/o OCC-2 can achieve better BLER performance of PDSCH compared with the type-2 DMRS w/o OCC-2 with SCSs =480 and 960 kHz.  Observation 13: For rank-2, both type-1 and type-2 DMRS w/o OCC-2 outperfom other DMRS types in BLER performance with SCSs=480 and 960 kHz.  Observation 14: Type-1 w/o OCC-2 outperforms in BLER performance other DMRS types in the most of the considered cases.  Observation 15: It is reasonable to provide a specification support for DMRS of PDSCH/PUSCH to be optimized only up to rank-2 in Rel-17 for at higher carrier frequencies (>52.6 GHz).  Observation 16: New DMRS type (irrespective of rank 1 or rank 2) does not provide any possibility for multiplexing of it with any other type of signal/RS/channel into same OFDM symbol.  Observation 17: Due to additional RS overhead associated with the new DMRS type, the usage of new DMRS type leads to reduced achievable PUSCH/PDSCH throughput in comparison with type-1 DMRS w/o OCC.  Observation 18: New DMRS type approximately doubles the computational complexity of the channel estimation associated with PUSCH/PDSCH.  Observation 19: It is not feasible to introduce new DMRS type for PUSCH/PDSCH in Rel-17 for above 52.6 GHz.  Proposal 21: No additional DMRS pattern is supported in Rel-17 for above 52.6 GHz.  Proposal 22: Support one of following alternatives for enhancement of the rank 1 PDSCH DM-RS reception.   * Alt 1: UE assumes no MU-pairing is applied when scheduled with 1 DM-RS port * Alt 2: Introduce new antenna port mapping of rank 1 scheduling and no MU-pairing. |
| [18, Qualcomm] | Observation 9: For rank 1, with SCS 960kHz, for channels with larger DS, the main reason of performance degradation with the larger SCS is the loss of orthogonality, and the gain from increasing the frequency density of the DMRS tones is limited, i.e., the performances of Config.1 with no CDMing and the new configuration with no CDMing are very close to each other.  Observation 10: For rank 1, with SCS 480kHz, even for channels with larger DS, the different DMRS patterns have very comparable performances, and the best performance is obtained Config.1 with no CDMing.  Observation 11: For rank 2, with SCS 960kHz, with DS 20ns all DMRS patterns perform the same, while with DS 50ns, there is a significant performance loss when FD-OCC is ON, and the best performance is obtained with config type 1 with ports from different CDM groups.  Observation 12: For rank 2, with SCS 480kHz, all DMRS patterns perform the same.  Proposal 5: Do not introduce a new pattern with DMRS tones sent over every RE, for the higher band.  Proposal 6: For DMRS enhancement for high SCSs, while communicating over channels with large DS and using high MCS, for rank 1, a single port should be used from one CDM group and the remaining ports from the same group should not be assigned to other UEs.  Proposal 7: Consider the following options to signal the information of FD-OCC OFF/ON   * Option 1: RRC configuration tied to an MCS threshold * Option 2: DCI indication by introducing new entries to the DMRS antenna ports tables, e.g., reuse the reserved entries |
| [19, LG] | Proposal #18: DM-RS configuration without FD-OCC should be supported for high SCS.  Proposal #19: Further study on how to indicate implicitly that FD-OCC is not applied to DM-RS port is required. |
| [21, Intel] | Proposal 15:   * For DMRS enhancement in NR extension up to 71 GHz support either indication to UE that CDM groups, signaled in scheduling DCI, do not contain potential co-scheduled DMRS ports (aka DMRS without OCC de-spreading) or full-density DMRS (without any OCC de-spreading restrictions). |
| [22, Apple] | Proposal 4: Conclude that no new DMRS pattern with increased frequency domain density (in number of subcarriers) than the existing DMRS patterns for NR operation in 52.6 to 71 GHz with 480 kHz and/or 960 kHz SCS in Rel-17.  Proposal 5: To account for transmission with large SCSs in low coherence BW channels,   * turn on or off the FD-OCC based on the scenario the channel is in * configure the UE with a DMRS port pattern based on the new SCSs and the coherence bandwidth of the channel * This should be applicable to DMRS type-1 and DMRS type-2.   Proposal 6: Deprioritize the study of DMRS bundling and DMRS overhead reduction for Rel-17 NR above 52.6 GHz operation. |
| [24, NTT DOCOMO] | Proposal 1: Support DMRS configuration, in which FD-OCC is not applied for 480 kHz and 960 kHz SCS, for Type1 and/or Type 2 DMRS  Proposal 2: Support new DMRS pattern with increased frequency domain density than the existing DMRS patterns for 480 kHz and 960 kHz SCS. |

### Summary on DMRS

#### FD density

The following was agreed in RAN1#104-e meeting.

* Existing DMRS patterns are supported for NR operation in 52.6 to 71 GHz with 120 kHz SCS.
* At least existing DMRS patterns are supported for NR operation in 52.6 to 71 GHz with 480 kHz and/or 960 kHz SCS
* Further study on whether to introduce different DMRS pattern with increased frequency domain density (in number of subcarriers) than the existing DMRS patterns for NR operation in 52.6 to 71 GHz with 480 kHz and/or 960 kHz SCS
* Further study on whether and how to restrict DMRS port configuration (e.g., the number of DMRS ports) as in FR2 for NR operation in 52.6 to 71 GHz with 480 kHz and/or 960 kHz SCS

On the need of DMRS enhancement for 480 and 960 kHz SCS, the following contributions submitted to this meeting evaluated and compared BLER performance using the existing comb DMRS pattern against some new DMRS patterns.

[3, vivo] compared performance of Rel-15 Type-1 DMRS and DMRS on every RE for high MCS with different DS. It is observed that ‘DMRS on every RE with FD-OCC’ has better performance than ‘Type-1 with FD-OCC’. It also observed that ‘Type-1 no FD-OCC’ still supports data multiplexing in DMRS symbols, while ‘DMRS on every RE’ cannot support that.

[5, InterDigital] compared BLER and throughput performances of Rank 1 and Rank 2 for 480 and 960 kHz SCS. It observed performance gain of an enhanced DMRS pattern with increased density for low SNR UEs. It proposed to support new DMRS pattern and dynamic switching of existing and new patterns.

[7, Lenovo] evaluated BLER performance of DMRS mapped to each RE in frequency domain and showed about 1 dB gain for 960 kHz SCS compared to existing type-1 DMRS. It also proposed to reduce number of DM-RS ports as the performance gain of high rank MIMO channels is expected to be limited in this FR.

[10, ZTE] observed that with the same total RS power, Rel-15 DMRS Type 1 pattern and the new DMRS pattern that fully occupied in frequency domain show comparable performance.

[15, Nokia] compared BLER performance of rank-1 and rank-2 PDSCH for different DMRS configuration options w/ and w/o OCC-2 (i.e. Rel-15 type-1, Rel-15 type-2 and new type (“comb-1”) ) without any phase noise impairments for 480 and 960 kHz SCS. It is observed that new type DMRS (i.e. comb-1 or increased frequency density) does not outperform Type-1 w/o OCC-2.

[18, Qualcomm] compared PDSCH performance of a new DMRS pattern featured by high frequency density (i.e., every RE) and 2-FD-OCC across adjacent REs with existing type-1 and type-2 DMRS patterns with 480 and 960kHz SCS. It is observed that the gain from increasing the frequency density of the DMRS tones is limited (e.g., < 0.2 dB when CDM is off for MCS22).

[21, Intel] evaluated PDSCH performance with and without frequency domain OCC being enabled as well as full density DMRS. For higher order modulation such as 64QAM (MCS 22), it observed the performance gain for both without FD-OCC and full density DMRS. It then proposed to support either FD-OCC off or full density DMRS.

[22, Apple] compared the performance of new pattern (increased density) for the 960 kHz SCS with different channel delay spreads at 5 usec, 10 usecs, and 20 usec for MSCS 22. It observed a small improvement (0.5 dB at 10-1 for DS = 20) in BLER performance and proposed that new pattern should not be adopted.

[24, NTT DOCOMO] have evaluated PDSCH BLERs with 480 and 960 kHz SCS for different DMRS patterns with 2-port configuration, i.e., Rel-15 DMRS type 1 with comb and non-comb (i.e., FD-OCC) based 2-port configuration, Rel-15 DMRS type 2 with comb and non-comb (i.e., FD-OCC) based 2-port configuration, and 2-port DMRS with DMRS on every RE in the symbol containing DMRS. It observed performance gain of full-density DMRS.

In addition to BLER performance, other aspects of block DMRS including the possibility for multiplexing of it with any other type of signal/RS/channel into same OFDM symbol, extra overhead and computational complexity of channel estimation are discussed in [15, Nokia].

Companies’ results showing notable performance gain of increased DMRS frequency density are summarized below.

Yes: [3, vivo], [5, InterDigital], [7, Lenovo], [21, Intel], [24, NTT DOCOMO]

No: [10, ZTE], [15, Nokia], [18, Qualcomm], [22, Apple]

Companies’ view to support increased DMRS frequency density are summarized below.

Yes: [5, InterDigital], [7, Lenovo], [21, Intel], [24, NTT DOCOMO]

No: [3, vivo], [9, CATT], [10, ZTE], [15, Nokia], [18, Qualcomm], [22, Apple]

Moderator’s comment:

It has been three meetings for companies to consider, evaluate and debate on the increased DMRS frequency density. Although more evaluation results are submitted, there has not been a shift in company positions to form a clear majority to support it.

Unless the proponent companies can convince other companies in this meeting, moderator suggest conclude and close the discussion point considering limited time of this WI and in light of the potential support of FD-OCC off (as in section 2.4.2.2), which achieves similar performance improvement compared to legacy DMRS with increased density (full RE).

##### Discussion point 4-1:

Companies are encouraged to provide comments and/or potential agreeable proposal if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | In our view, increased DMRS frequency density and/or FD-OCC are essential for the channel estimation performance with higher SCS. Therefore, at least one of these enhancements should be supported. If we can agree to support FD-OCC off, then we are ok with this proposed conclusion. |
| Qualcomm | We do not support introducing new pattern with full RE density as it does not provide a significant performance gain compared with legacy pattern with FD-OCC OFF |
| LG Electronics | Agree with the moderator’s comment that if no consensus can be reached by end of this meeting, then this discussion should be closed.  We do not support the new pattern with full RE density because the new pattern shows only a marginal performance gain compared to the legacy pattern, and also prevents data multiplexing. |
| Futurewei | Since the DMRS frequency density issue has been studied for three meetings and no clear gain is shown by companies to increase the density, it is recommended to reuse the legacy DMRS frequency density and close the discussion. |
| Intel | We support the full density DMRS as it provides improvement of PDSCH performance via better channel estimation according to our evaluation results. |

#### FD OCC (high priority)

The following was agreed in RAN1#104-e meeting.

Further study on at least the following aspects of potential DMRS enhancement with respect to FD-OCC:

* whether to support a configuration of DMRS in which FD-OCC is not applied for 480 kHz and 960 kHz SCS
  + Applicability to Type-1 and/or Type-2 DMRS
  + Details on whether and how to indicate that FD-OCC is not applied to DMRS port
  + Impact to UE multiplexing capacity and inter-UE interference in MU-MIMO

The following contributions studied and evaluated performance with respect to FD-OCC.

[3, vivo] compared PDSCH BLER performance of type-1 DMRS with and without FD-OCC for 480KHz and 960 KHz SCS with 64QAM, while the phase noise is compensated with CPE only approach. It observed some gain of both type-1 and type-2 DMRS without OCC for high MCS especially at large delay spread (e.g., TDL-A DS >= 20 ns).

[7, Lenovo] argued that for NR operation beyond 52.6 GHz, the performance gain of high rank is limited. Therefore, it proposed to support FD-OCC off for this FR, at least with high SCS values of 480kHz and 960kHz and consequently reduce the number of orthogonal ports.

[13, Ericsson] proposed to support FD-OCC off for rank-1 UE and argued that such a method is most beneficial for Type-1 DMRS, since this DMRS type is well-suited for the 52.6 – 71 GHz band due to it's low PAPR/CM properties, and the fact that large DMRS port-multiplexing capacity is not needed.

[15, Nokia] compared BLER performance of rank-1 and rank-2 PDSCH for different DMRS configuration options w/ and w/o OCC-2 (i.e. Rel-15 type-1, Rel-15 type-2 and new type (“comb-1”) ) without any phase noise impairments. It is observed that Type-1 w/o OCC-2 outperforms other DMRS configurations. It proposed to support either UE assumes no MU-pairing is applied when scheduled with 1 DM-RS port or introduce new antenna port mapping of rank 1 scheduling and no MU-pairing.

[18, Qualcomm] compared PDSCH performance of a new DMRS pattern featured by high frequency density (i.e., every RE) and 2-FD-OCC across adjacent REs with existing type-1 and type-2 DMRS patterns with 480 and 960kHz SCS. It is observed that for channels with larger DS, the main reason of performance degradation with the larger SCS is the loss of orthogonality. It showed performance gain without CDM for MCS22/26.

[21, Intel] evaluated PDSCH performance with and without frequency domain OCC being enabled for DMRS. For higher order modulation such as 64QAM (MCS 22), it observed the performance drop when OCC is enabled.

[22, Apple] evaluated PDSCH performance of type-1 DMRS with and without FD-OCC for 960 kHz SCS. It observed that at high frequency selectivity (low coherence bandwidth for large delay spread) there is a benefit in turning off the FD-OCC. It also observed that the FD-OCC adaptation can be used by a UE with DMRS type-2 without any increase in signaling/complexity especially if explicit signaling is used and as such should be applicable for DMRS type-2.

[24, NTT DOCOMO] have evaluated PDSCH BLERs with 480 and 960 kHz SCS for different DMRS patterns with 2-port configuration, i.e., Rel-15 DMRS type 1 with comb and non-comb (i.e., FD-OCC) based 2-port configuration, Rel-15 DMRS type 2 with comb and non-comb (i.e., FD-OCC) based 2-port configuration, and 2-port DMRS with DMRS on every RE in the symbol containing DMRS. It observed performance gain when FD-OCC is off for both type 1 and type 2 DMRS.

Companies’ results showing notable performance gain of turn off FD-OCC are summarized below.

Yes: [3, vivo], [15, Nokia], [18, Qualcomm], [21, Intel], [22, Apple], [24, NTT DOCOMO]

Companies’ view to support FD-OCC off are summarized below.

Yes: [3, vivo], [7, Lenovo], [13, Ericsson], [15, Nokia], [18, Qualcomm], [19, LG], [21, Intel], [22, Apple], [24, NTT DOCOMO]

No:

Companies views on whether support FD-OCC off for type-1 and/or type-2 DMRS are summarized below.

Type-1 only: [8, Samsung], [13, Ericsson],

Type-1 and type-2: [3, vivo], [7, Lenovo], [22, Apple], [24, NTT DOCOMO]

Companies views on how to indicate FD-OCC off to UE are summarized below.

RRC: [8, Samsung]

DCI (e.g., use the reserved states in the "Antenna port(s)" field): [9, CATT]

FFS: [13, Ericsson], [15, Nokia], [18, Qualcomm], [19, LG]

Moderator’s comment:

Seems no company object to support a DMRS configuration where UE can assume FD-OCC is off. Note that based on the discussion in RAN1#104b-e, formulate the following alternative proposals and one of them should be chosen.

##### Proposal 4-2.Alt1:

* For NR operation in FR2-2 with 480 kHz and/or 960 kHz SCS, for rank 1 PDSCH at least with DMRS type-1, support a configuration of DMRS where the UE is able to assume that FD-OCC is not applied.
  + FFS whether applies to DMRS type-2
  + FFS details on whether and how to indicate that FD-OCC is not applied to DMRS port

##### Proposal 4-2.Alt2:

* For NR operation in FR2-2 with 480 kHz and/or 960 kHz SCS, for rank 1 PDSCH with DMRS type-1, support a RRC configuration which indicates FD-OCC is not applied to an DMRS port indicated by antenna port(s) field in DCI scheduling the rank 1 PDSCH.
  + FFS which or all DMRS port(s)

##### Proposal 4-2.Alt3:

* For NR operation in FR2-2 with 480 kHz and/or 960 kHz SCS, for rank 1 PDSCH with DMRS type-1, support a DMRS configuration where UE is able to assume that FD-OCC is not applied to the DMRS port(s) indicated by antenna port(s) field in DCI scheduling the rank 1 PDSCH.
  + FFS which reserved state(s) in antenna port(s) field

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | We support proposal 4-2 Alt 1.  In our view, FD-OCC should be applied to both DMRS type-1 and type-2 and it seems to be considered only with Alt 1. |
| Qualcomm | We do not see much progress with Alt 1 compared with the last agreement.  We support Alt 3, with the addition of considering DMRS type-2 as well for this enhancement  Alt 2 will limit the flexibility of scheduling by losing multiplexing opportunities specially with low MCS where FD-OCC does not cause a significant performance loss |
| LG Electronics | We support Alt 1 or Alt 3. For Alt 2, we share the view as Qualcomm. |
| Futurewei | Support Proposal 4-2.Alt1 that includes further study for type-2 DMRS FD-OCC. |
| Moderator | Wording update below to address comments to DMRS type-2. |

##### Proposal 4-2a.Alt1:

* For NR operation in FR2-2 with 480 kHz and/or 960 kHz SCS, for rank 1 PDSCH at least with DMRS type-1, support a configuration of DMRS where the UE is able to assume that FD-OCC is not applied.
  + FFS whether applies to DMRS type-2
  + FFS details on whether and how to indicate that FD-OCC is not applied to DMRS port

##### Proposal 4-2a.Alt2:

* For NR operation in FR2-2 with 480 kHz and/or 960 kHz SCS, for rank 1 PDSCH at least with DMRS type-1, support a RRC configuration which indicates FD-OCC is not applied to an DMRS port indicated by antenna port(s) field in DCI scheduling the rank 1 PDSCH.
  + FFS whether applies to DMRS type-2
  + FFS which or all DMRS port(s)

##### Proposal 4-2a.Alt3:

* For NR operation in FR2-2 with 480 kHz and/or 960 kHz SCS, for rank 1 PDSCH at least with DMRS type-1, support a DMRS configuration where UE is able to assume that FD-OCC is not applied to the DMRS port(s) indicated by antenna port(s) field in DCI scheduling the rank 1 PDSCH.
  + FFS whether applies to DMRS type-2
  + FFS which reserved state(s) in antenna port(s) field

Companies are encouraged to provide comments if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Intel | Among the alternatives 1/2/3, we support Proposal 4-2.Alt3. |
|  |  |
|  |  |
|  |  |

#### DMRS for multi-PDSCH/PUSCH scheduling

[1, Huawei] compared two DMRS patterns in time domain: Rel-15 DMRS pattern (with individual channel estimation per slot), and a bundling DMRS pattern (with joint channel estimation based on all the DMRS symbols across slots). It observed about 0.2dB~0.6dB gain of the bundling DMRS pattern. [1, Huawei] then proposed that DMRS mapped on symbol l0 to symbol l0+S\*L-1 within the first PDSCH slot for the multi-slot scheduling, when only front-loaded DMRS is configured, where L is the length and l0 the starting symbol of legacy front-loaded DMRS.

[9, CATT] argued that given the channel estimation filter at the UE is usually optimized with fixed filter length based on current DMRS pattern, DMRS bundling will increase the UE implementation complexity since the enhancement depends on the receiver algorithm in UE implementation. With that, it proposed not to support potential DMRS enhancement for multi-PDSCH/PUSCH scheduling.

[8, Samsung] proposed for multiple PDSCHs/PUSCHs with contiguous time domain resource, DMRS time domain density can be lower than one DMRS per PUSCH/PDSCH to reduce DMRS overhead and DMRS bundling of multiple PUSCHs/PDSCHs can be applied to improve channel estimation performance.

On the same topic, [15, Nokia] argued that the decoding of each slot in a period is up to implementation, and new (bundled DMRS) pattern increase the complexity and proposed to use the existing DMRS time-domain pattern for multi-slot scheduling unless any critical performance degradation is identified.

[22, Apple] also argued that given there is current work on joint channel estimation for PUSCH in the Rel-17 coverage enhancement Work Item, to avoid duplication of effort between work items, the discussion on these enhancements (especially DMRS bundling) should be de-prioritized.

Companies’ view to support DMRS enhancement for multi-PDSCH/PUSCH scheduling are summarized below.

Yes: [1, Huawei], [8, Samsung]

No: [9, CATT], [15, Nokia], [22, Apple] (deprioritize)

Moderator’s comment:

With limited input and diverse views on this topic, suggest companies to study further.

##### Discussion point 4-3:

Companies are encouraged to provide comments and/or suggestions on agreeable proposals if any.

|  |  |
| --- | --- |
| Company Name | Comments/Views |
| Lenovo, Motorola Mobility | Similar work is on-going in the CE WI and considering that this is a low-priority area for this WI, we propose to conclude that no further discussion on DMRS enhancements for multiple PDSC/PUSCH is done in this WI. |
| Qualcomm | For Multi-PUSCH grant, the DMRS bundling is considered in coverage enhancement WI and no need to duplicate the discussion.  We do not support DMRS bundling for multi-PDSCH as is will increase the UE complexity and may affect the UE processing timeline. |
| Huawei, HiSilicon | For clarity, we do not propose DMRS bundling across slots, as this is being discussed in the Coverage Enhancements WI and there is no need repeating the discussion here. The two comments above don’t apply to our proposal described below for better clarity.  Our proposal for above 52.6 GHz with multi-slot scheduling is to have DMRS only in the first scheduled slot, in order to avoid the delay incurred for PDSCH decoding in the last slot(s) of 480/960 kHz SCS, which would otherwise delay the HARQ feedback unevenly for different values of SCS. Additionally the DMRS that is only present in the first slot it may benefit from occupying more OFDM symbols for better channel estimation accuracy. Therefore our proposal:  DMRS mapped on symbol l0 to symbol l0+S\*L-1 within the first PDSCH slot for the multi-slot scheduling, when only front-loaded DMRS is configured, where L is the length and l0 the starting symbol of legacy front-loaded DMRS. |
| Futurewei | Given that the channel fluctuation across multiple slots is expected to be small for higher subcarrier spacing, we support new DMRS patterns for multiple PxSCH, for example, allocation more DMRS symbols to the earlier slots of a multi-slots, such that demodulation latency is reduced without affecting much of the performance. |

# Conclusion

TBD

# Reference

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3. [R1-2106583](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_106-e/Docs/R1-2106583.zip) Discussions on PDSCH/PUSCH enhancements for NR operation from 52.6GHz to 71GHz vivo
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10. [R1-2107004](https://www.3gpp.org/ftp/tsg_ran/WG1_RL1/TSGR1_106-e/Docs/R1-2107004.zip) Discussion on the data channel enhancements for 52.6 to 71GHz ZTE, Sanechips
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