**3GPP TSG RAN WG1 Meeting #106-e R1-2108207**

**e-Meeting, August 16 – 27, 2021**

**Source: Moderator (Intel Corporation)**

**Title: Summary #1 of email discussion on initial access aspect of NR extension up to 71 GHz**

**Agenda item: 8.2.1**

**Document for: Discussion**

# Introduction

In this contribution, we discuss aspects related to initial access for extending NR up to 71 GHz based on submitted contributions to RAN1 #106-e. The main issues discussed in the following section for initial access are detailed design for synchronization signal block (SSB), CORESET#0, PRACH related issues, and discovery reference signal (DRS) related operations.

During the last RAN Plenary, the WID has been updated to reflect the approved numerologies for initial access. The following is copy of the WID objectives relevant for initial access.

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| * Physical layer aspects including [RAN1]:   + Support of up to 64 SSB beams for licensed and unlicensed operation in this frequency range.   + Supports 120kHz SCS for SSB and 120kHz SCS for initial access related signals/channels in an initial BWP.     - Study and specify, if needed, additional SCS (480kHz, 960kHz) for SSB for cases other than initial access.     - Note: coverage enhancement for SSB is not pursued.   + In addition to 120kHz, support 480 kHz SSB for initial access with support of CORESET#0/Type0-PDCCH configuration in the MIB with following constraints:     - Limited sync raster entry numbers       * It is assumed that RAN4 supports a channelization design which results in the total number of synchronization raster entries considering both licensed and unlicensed operation in a 52.6 – 71 GHz band no larger than 665 (Note: the total number of synchronization raster entries in FR2 for band n259 + n257 is 599). If the assumption cannot be satisfied, it’s up to RAN4 to decide its applicability to bands in 52.6 – 71 GHz.     - only 480kHz CORESET#0/Type0-PDCCH SCS supported for 480 kHz SSB SCS.     - Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis.     - 960 kHz numerology for the SSB is not supported by the UE for initial access in Rel-17.     - Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible     - Note: 480 kHz is an optional SSB numerology for initial access for the UE. A UE supporting a band in 52.6-71 GHz must at least support 120 kHz SCS (for initial access and after initial access)     - Note: Dependency or lack thereof for a UE supporting 480kHz and/or 960kHz numerology for data and control to also support 480kHz SSB numerology for initial access is to be tackled as part of UE capability discussion.   + Support ANR and PCI confusion detection for 120, 480 and 960kHz SCS based SSB, support CORESET#0/Type0-PDCCH configuration in MIB of 120, 480 and 960kHz SSB     - FFS: additional method(s) to enable support to obtain neighbour cell SIB1 contents related to CGI reporting     - Only 1 CORESET#0/Type0-PDCCH SCS supported for each SSB SCS, i.e., (120, 120), (480, 480) and (960, 960).     - Prioritize support SSB-CORESET#0 multiplexing pattern 1. Other patterns discussed on a best effort basis.     - Note: Strive to minimize specification impact by reusing tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2 in Rel-15, as much as possible     - Note: From UE perspective, ANR detection for 480/960kHz SCS based SSB is not supported if the UE does not support 480/960 SCS for SSB.     - Note: for ANR, when reading the MIB, the cell containing the SSB is known to the UE, as defined in 38.133 specification.   + Specify support for PRACH sequence lengths (i.e. L=139, L=571 and L=1151) and study, if needed, specify support for RO configuration for non-consecutive RACH occasions (RO) in time domain for operation in shared spectrum |

# Summary of issues

## 2.1 SSB Aspects

### 2.1.1 DRS Related Aspects (and other MIB design other than CORESET#0/Type0-PDCCH)

* From [1] Huawei/HiSilicon:
  + For operation with shared spectrum and for 480 kHz and 960 kHz SSBs, indicate the 7th bit of the candidate SSB index by borrowing the 4th LSB of SFN in the PBCH payload. Indicate the 4th LSB of SFB in MIB payload.
  + Support discovery burst transmission window for all numerologies in shared spectrum in 52.6GHz to 71GHz.
  + If LBT on/off indication is deemed required to determine the size of DCI 1\_0 whose CRC scrambled with SI-RNTI, such an indication may be performed using one of the following methods:
    - Using one bit in MIB
    - Implicitly using the synch raster entry of the associated SSB used for initial access
  + Similar to Rel-16 NR-U, use the following method to implicitly indicate in SIB1 that DBTW is enabled/disabled:
    - If DBTW length is equal to or smaller than the time duration from the beginning of the half frame to the end of the slot containing the candidate SSB index N\_SSB^QCL-1, DBTW is disabled.
    - If DBTW length is larger than the time duration from the beginning of the half frame to the end of the slot containing the candidate SSB index N\_SSB^QCL -1, DBTW is enabled.
    - Note 1: DBTW is configured in SIB1 and N\_SSB^QCL is acquired from the MIB payload.
    - Note 2: Prior to reading SIB1, UE assumes that DBTW includes all candidate SSB positions in a half frame.
  + Values {8, 16, 32, 64} should be supported for N\_{SSB}^{QCL}\ in operation with shared spectrum above 52.6GHz.
  + Configure DBTW length in SIB1 for operation with shared spectrum in 52.6GHz to 71GHz with the following values:
    - 120 kHz SCS: {40, 32, 24, 16, 8, 4} slots = {5, 4, 3, 2, 1} ms
    - 480 kHz SCS: {72, 32, 24, 16, 8, 4} slots = {2.25, 1, 0.75, 0.5, 0.25, 0.125} ms
    - 960 kHz SCS: {64, 32, 24, 16, 8, 4} slots = {1, 0.5, 0.375, 0.25, 0.125, 0.0625} ms
  + In operation with shared spectrum in 60 GHz, for MSB k, k≥1, of inOneGroup and MSB m, m≥1, of groupPresense of ssb-PositionsInBurst:
    - if MSB k of inOneGroup and MSB m of groupPresense are set to 1, the UE assumes that SSB(s) within DBTW with candidate SSB index(es) corresponding to SSB index equal to k-1+(m-1)×8 may be transmitted;
    - if MSB k of inOneGroup or MSB m of groupPresense are set to 0, the UE assumes that the SSB(s) are not transmitted.
  + Regardless of the value of the MSB k of inOneGroup and MSB m of groupPresense in ssb-PositionsInBurst configured in SIB1, if , UE assumes that candidate SSB index(es) corresponding to SSB index equal to are not transmitted.
* From [2] vivo:
  + The following fields could be considered to indicate the value of Q in PBCH:
    - subCarrierSpacingCommon
    - LSB of ssb-SubcarrierOffset
    - Coreset#0 and Type#0 PDCCH indication
  + When DBTW is enabled with indicated value of Q, how to interpret the meaning of ssbPositionsInBurst should be studied.
  + More number of candidate SSBs should be specified for LBT case to alleviate LBT failure than non-LBT case.
  + Support DBTW in un-licensed band/LBT case from 52.6 GHz to 71 GHz for SSB with all supported SCSs.
  + The following methods could be considered to determine whether there is DBTW:
    - Alt. 1: GSCN (licensed or un-licensed);
    - Alt. 2: The indicator in PBCH;
  + Supported DBTW length as the same in NR-U, which is 0.5, 1, 2, 3, 4, 5 msec.
  + The number of candidate SSB positions for SCS 120 kHz and SCS 480 kHz should be 64 and 128 respectively.
  + LBT on/off is not indicated in MIB.
* From [3] Spreadtrum:
  + Confirm that DBTW is supported at least for 120kHz SCS.
* From [4] Interdigital:
  + Enhance the initial access operation to support Discovery Burst (DB) and Discovery Burst Transmission Window (DBTW) in unlicensed spectrum operations that require LBT in beyond 52.6GHz spectrum.
  + Consider indicating enable/disable of DBTW in initial access operations based on a sync raster offset used by SS/PBCH block.
  + Consider the enhancements to indicate the mode of operation regarding the enable/disable of the DBTW, on/off of the LBT, and the license regime based on the combination of Sync. raster offset and MSB of controlResourceSetZero.
  + Support enhancements on the reference tables in indication of Q parameter for up to 64 SSB beams in initial access operations for unlicensed spectrum in beyond 52.6GHz, e.g., subsamples of the Q parameter.
    - Support Alt A, for the total number of options for the Q parameter to not exceed 4.
* From [5] Sony:
  + Discovery Burst Transmission Window should be supported.
  + Enabling/disabling DBTW and should be signalled in MIB
    - Indication of disabling DBTW should be jointly coded with
      * Parameter to signal disabling DBTW and indicates {16, 32, 64, or disabling DBTW} if the number of candidate SSB position is more than 64
      * Parameter to signal disabling DBTW and indicates {8, 16, 32, or disabling DBTW} if the number of candidate SSB position is 64
  + Candidate SSB positions should be extended when DBTW is enabled.
    - For 120 kHz SCS,
      * The number of candidate SSB positions should be 80
      * additional n values (4, 9, 14, 19) should be supported when DBTW is enabled
    - For 480/960 kHz SCS,
      * The number of candidate SSB positions should be 128
      * First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
      * n = {0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18} when DBTW is disabled.
      * n = 0 - 31 when DBTW is enabled
  + For indication of candidate SSB indices, QCL relation, and disabling DBTW, subCarrierSpacingCommon and reserved state of pdcchConfig-SIB1 should be used.
* From [6] Lenovo/Motorola Mobility
  + For NR operation in unlicensed bands between 52.6 GHz and 71 GHz, potential enhancements related to periodic transmission of DRS such as SSB/PBCH/CORESET#0 are needed including:
    - performing directional LBT prior to the transmission of SSB according to the ssb-PositionsInBurst
    - directional LBT on multiple beams at the same time at the beginning of the DRS window
    - Cat 2 LBT (depending on the gap) before actual transmission
* From [7] Samsung:
  + For 480 kHz and 960 kHz,
    - Support the same SS/PBCH block pattern in a slot, and the same pattern is given by Case A/C (i.e., Alt 1 with X=2 and Y=8).
    - Support larger number of slots including candidate SS/PBCH block, when DBTW is enabled.
  + Support discovery burst transmission window for all SCSs on the 60 GHz unlicensed spectrum.
    - The indication of Q can be in MIB for a best effort, and if not possible, in SIB1;
    - The indication of DBTW disabling can be joint coded with the indication of Q, if Q is indicated in MIB; and the indication can use 1 bit in MIB, if Q is not indicated in MIB;
    - The case of an unlicensed operation with DBTW disabled can be supported implicitly, by comparing the Q value and the DBTW window size;
    - Support more than 64 candidate SS/PBCH block locations within a half frame;
      * Current PBCH payload can support timing indication of up to 128 candidate SS/PBCH block candidate locations;
      * Use one PHY bit to indicate the extra candidate SS/PBCH block index (e.g. 7th LSB);
    - For initial access, different synchronization raster entries are applied for licensed and unlicensed operations; for non-initial access, support an explicit indication of licensed or licensed operation when configuring a cell.
* From [8] CATT:
  + The subCarrierSpacingCommon field in MIB can be saved and repurposed.
  + More than 64 SSB transmission opportunities shall be defined within a 5ms SSB burst set to support up to 64 beams for SSB beam sweeping in case of LBT failure. The issue of supporting additional bit(s) for the indicating SSB candidate index needs further study.
  + For no-LBT operation or licensed spectrum operation, value “n” can keep the same value as for the 120KHz SCS case.
  + Additional n value such as #4, #9, #14, and #19 can be used for new SSB candidates if LBT/DBTW is needed for SSB transmission.
  + For up to 71GHz operation and at least for NO-LBT operation, some values of ‘n’ can be reserved for uplink grant scheduling.
  + For NR operation in 60 GHz unlicensed spectrum, the discovery burst transmission window (DBTW) shall be supported for 120 KHz SSB at least when gNB configures more than 56 SSB transmissions.
  + DBTW is not needed for SSB with 480 KHz/960 KHz SCS since the duty cycle is less than 10% over the 100 ms observation window for the short control signaling transmissions.
  + For supporting DBTW of 120KHz SCS SSB, more than 64 SSB (up to a total of 80 ) positions are needed. A total of 7 bits of information is needed to indicate more than 64 SSB candidate locations.
  + For indication of （if needed at for 120kHz SSB）， legacy mechanism can be reused.
  + Considering Contention Exempt Short Control Signalling rules can be applicable to the transmission of SS/PBCH for most cases , only 5ms duration for DBTW operation is supported .
  + For 120 kHz SSB, signaling in MIB can indicate enable/disable of DBTW.
  + If LBT ON/OFF state is indicated in MIB/PBCH, joint coding can be used for indication of LBT ON/OFF, DBTW enabling/disabling and one bit information for candidate SSB index.
  + If LBT ON/OFF state is not indicated in MIB/PBCH, it can be indicated in DCI 1\_0 scrambled by SI-RNTI.
* From [9] ZTE/Sanechips:
  + Discovery burst transmission window (DBTW) should be supported for 120 kHz SSB SCS and other SSB SCSs.
  + In order to reduce the impact of standardization caused by indicating candidate SSB indices, the maximum number of candidate SSB defined in the half-frame can be kept unchanged (maintain 64) or limited to 128 for 480/960 kHz SSB SCS.
  + Four candidate values {8,16,32,64} for are preferred.
  + For 120 kHz SSB, enable/disable of DBTW can be indicated by comparing the value of  in MIB and DBTW length, and explicit signaling is not needed for this purpose.
* From [11] Ericsson:
  + Before RAN1 can agree that DBTW is supported, the following two aspects need to be jointly decided:
    - If and how additional candidate SSB positions are to be supported, and
    - How to signal the following: Q and DBTW on/off
  + Conclude that a DBTW is not supported for the 52.6 – 71 GHz band and that the size of DCI 1\_0 is the same regardless of channel access mode (Option 1). LBT on/off is signaled in SIB1.
* From [12] Futurewei:
  + For 480/960 kHz SS/PBCH DBTW should not be supported.
  + Support enabling and disabling LBT for channel access in shared spectrum, with LBT mode default enabled. Signal LBT disabled in the MIB.
  + For 480/960 kHz SS/PBCH SCS use the field subCarrierSpacingCommon to indicate LBT disabled.
  + For 120 kHz SS/PBCH SCS use the field subCarrierSpacingCommon and the LSB of ssb-SubcarrierOffset to indicate the N\_SSB^QCL, where one of the values indicates LBT disabled.



* + Use the following DBTW lengths values 0.5, 1, 2, 3, 4, 5 msec.
  + For 120 kHz SS/PBCH SCS use DBTW zero length in SIB1 to indicate that DBTW is disabled.
  + For 120kHz SSB the maximum number of candidate positions is 64.
  + Consider using CSI-RS presence in the discovery burst for possible ways to implement beam refinement during the initial channel access.
* From [13] Nokia/NSB:
  + Support operation with and without DBTW for 120 kHz.
  + Support DBTW also for 480/960 kHz SSB.
  + Provide LBT on/off indication in SIB1.
  + Support Option 2: enable/disable of DBTW is indicated by distinct GSCN used by the SSB.
  + Support Alt B) Explicit indication of SSB index and/or SSB candidate location.
  + Support 80 candidate positions for SSB when DBTW is enabled with 120 kHz.
  + Support also 80 candidate positions for SSB when DBTW is enabled with 480/960 kHz (if DBTW is supported for 480/960 kHz).
  + Group additional SSB locations and associate each group to set of regular SSB positions, e.g. after each block of 16 regular SSB positions there is associated group of up to four additional positions that can be used to retransmit any of the associated actual SSBs.
  + Use subCarrierSpacingCommon to indicate whether or not the SSB is in additional SSB position. Use kSSB bits in the SSB located in the additional position (based on subCarrierSpacingCommon) together with SSB index (PBCH DMRS and MSBs in PBCH payload) to provide UE information about the slot timing and actual SSB index transmitted.
  + Supported values for discoveryBurstWindowLength are same as used for Rel-16 NR-U
    - 0.5, 1, 2, 3, 4, 5 ms
  + It is possible to apply SCSe to one part of actually transmitted SSBs and LBT procedure for other/rest of the SSBs.
  + Consider semi-static or predetermined mechanism to determine which SSBs are under SCSe and which under LBT in certain time windows.
  + For 120kHz SSB pattern, introduce additional candidate locations for SSB transmission support for 𝑛 = 4, 9, 14, 19, where n is the slot index in half-frame.
    - The first symbols of the additional candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n.
  + For 480kHz and 960kHz SSB pattern, introduce additional candidate locations for SSB transmission support for 𝑛 = [{8, 9, 10, 11} ,{32,33,34,35}], where n is the slot index in half-frame.
* From [14] Charter:
  + DBTW is not introduced for 120 kHz, 480 kHz, and 960 kHz SCS SSB, including the non-initial access case.
  + If DBTW is introduced, supported DBTW lengths follow Alt 1) 0.5, 1, 2, 3, 4, 5 msec. Number of candidate positions when DBTW is enabled is 64.
* From [15] NEC:
  + DBTW should be supported for SSB transmission with 120 kHz and 480/960 kHz SCS.
  + The long term sensing could be considered as an approach to enabling/disabling DBTW.
  + DBTW indication for SSB transmission could be indicated per SSB/beam.
  + When LBT is used on unlicensed spectrum, enabling/disabling DBTW and LBT on/off indication could be jointly indicated in MIB.
  + At least for 120 kHz SCS SSB, the candidate SSB indication in NR-U should be reused with enhancement to indicate DBTW enabling/disabling and Q value jointly in MIB.
  + Additional discovery burst transmission window in the adjacent frame could be considered as a method of cycling SSB transmission.
  + With concurrent spatial multiplexing DBTWs, all SSBs could be transmitted in a cycling transmission fashion.
  + Additional n values of 4, 9, 14 and 19 should be supported to indicate 80 candidate SSBs in DBTW at least for 120 kHz SCS SSB pattern.
  + The indication of additional candidate SSBs based on additional n values should be investigated.
  + If DBTW is additionally supported for 480/960kHz SCS SSB transmission, 128 SSB candidates should be supported.
* From [16] Panasonic:
  + DBTW is supported regardless of SCS.
  + The number of candidate SSB positions is 64.
  + For enabling/disabling DBTW, Option 1-1 (disabling DBTW is jointly coded with ) with SIB indication of no-LBT mode is supported.
* From [18] Qualcomm:
  + do not support discovery burst transmission window (DBTW) for SSB for SCS 480 and 960 kHz
  + for an unlicensed band that requires LBT, if DBTW for SSB is adopted for 120 kHz SSB:
    - MIB signaling to support indication of for 120 kHz SSB
    - Minimize the number of bits needed to signal (1 or 2 bits) and thus the values (2 or 4 values)
    - Enabling/disabling DBTW can be implicit in the value
    - Consider getting the bits needed from one or more of the following: controlResourceSetZero, searchSpaceZero, ssb-SubcarrierOffset, subCarrierSpacingCommon
    - Number of candidate positions when DBTW is enabled = 64 for 120 kHz SSB
    - Consider having a subset of the SSBs (< 64) transmitted under the short control signal assumption while another subset can be best effort or have multiple positions per beam (have a within the subset)
  + consider increasing the size of the DCI 0\_0 and 1\_0 for NR licensed, by adding a field, to align with the size of the corresponding DCIs for the NR-U
* From [19] LG Electronics:
  + Adopt the following methods to indicate enabled/disabled DBTW for idle and/or connected mode UEs.
    - Separate two sets of GSCN values where one set corresponds to the case of disabled DBTW while the other set corresponds to the case of enabled DBTW
    - Signalling via system information (e.g., measObject)
    - UE-specific RRC signaling (e.g., for SCell addition)
  + Consider all or some of the following bits to indicate candidate values.
    - subCarrierSpacingCommon
    - LSB(s) of ssb-SubcarrierOffset
    - dmrs-TypeA-Position
  + Do not indicate LBT on/off in PBCH. DCI format 1\_0 size should be aligned regardless of LBT on or off.
  + Support of additional n values for the time domain pattern of SS/PBCH block with 120 kHz SCS can be considered to increase SS/PBCH block’s transmission opportunities, only if PBCH payload is sufficient to indicate the increased number of candidate SS/PBCH block indexes.
  + For 480/960 kHz SSB, first symbols of the candidate SSB have index are {4, 8, 16, 20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame (i.e., Alt 2 in previous agreement), and values of ‘n’ are consecutive integers (i.e., n = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15).
* From [20] ETRI:
  + Propose to support DBTW for all SSB SCSs and the same DBTW lengths with Rel-16 NR-U.
  + Propose to support joint coding for LBT, DBTW, and , and study which bits can be used for reinterpretation for the joint coding.
* From [22] Intel:
  + Support DBTW for SSB with SCS 120 kHz
    - The max number of candidate SSB is
    - Support additional values of , such as 4, 9, 14, 19, in the equation defining the first symbols of candidate SS/PBCH blocks
    - Additional candidate SSBs (i.e., with index greater or equal to 64) are indexed in non-ascending order in time
      * An example relationship between candidate SSB index and SSB slot parameter can be specified in a closed form as follows:
  + Support DBTW for SSB with SCS 480 kHz/960 kHz
    - The max number of candidate SSB is
    - All candidate SSBs are indexed in ascending order in time
  + DBTW length is 5 ms.
  + For QCL relationship indication across SSBs, reuse Rel-16 NR-U mechanism by introducing parameter.
  + Explicitly indicate candidate SSB index for and in MIB.
    - No changes to MIB payload size. Further discuss and consider reinterpreting bits from some bit fields within MIB to extend candidate SSB index and provide information
    - FFS:
      * Two or four values of , e.g., or ;
      * Whether the set of values depends on SSB SCS, e.g., for SCS 120 kHz and for SCS 480 kHz/960 kHz.
  + Distinguishing between channel access cases is not needed during reception of DRS based on SS burst.
  + No need to indicate DBTW enabling. The network can configure parameter value to operate as if no DBTW is used.
  + For unlicensed operation, LBT on/off indication is within DCI scheduling SIB1.
  + Indication of licensed vs. unlicensed operation could be done based on SSB raster position. If this is not possible due to future compatibility issues, indicate licensed vs. unlicensed operation in DCI scheduling SIB1
    - To avoid DCI size ambiguity issue for licensed case, apply bit padding to DCI scheduling SIB, i.e., increase the number of reserved bits for DCI 1\_0 scrambled with SI-RNTI.
* From [23] Apple:
  + If DBTW is introduced, for above 52.6GHz frequency band, consider the following:
    - Re-purposing the 1-bit 'subCarrierSpacingCommon'
    - If more than one bit is needed, re-purposing 1-bit MSB of controlResourceSetZero in MIB or providing one more bit information by selecting one sequence from two candidates to scramble CRC bits of PBCH payload.
    - Support joint encoding Q value and licensed/unlicensed band indication.
      * If joint encoding is not possible, licensed/unlicensed band can be signaled in SIB1 and UE monitors the DCI 1\_0 for SIB1 scheduling assuming two different sizes.
* From [24] Sharp:
  + Adopt DBTW for SSB with 120 kHz SCS in above 52.6GHz.
* From [25] NTT Docomo:
  + With 120 kHz SCS, ‘n’ value(s) which can be added on top of the ones agreed already are limited, i.e., ‘n’ = {4, 9, 14, 19} only
  + With 120 kHz SCS, no significant need to support additional ‘n’ values on top of the ones agreed already
  + With 480/960 kHz SCS, not support more than 64 candidate SSB positions
  + DBTW should be supported irrespective of SCS.
    - In a certain region, e.g., Japan, sensing needs to be performed for initiating any transmission by any device in 60 GHz.
  + For DBTW to be supported in Rel-17 NR 52.6 – 71 GHz, similar to DBTW in Rel-16 NR-U, subCarrierSpacingCommon field in MIB should indicate QCL parameter, which is up to 64.
    - Following information can be implicitly indicated via subCarrierSpacingCommon
    - Enabling/disabling of DBTW
    - Licensed/unlicensed band
    - LBT on/off
* From [26] Xiaomi:
  + Alt1 (same as Rel-16 FR1 NR-U) is supported.
  + The number of candidate positions when DBTW is enabled is 64.
* From [27] Convida:
  + Increasing the number of SSB candidate positions to above 64 to increase transmission opportunities to cope with LBT failure should be considered.
  + The number of values for ‘n’ should be dependent on LBT operation and the actual values of ‘n’ for each SCS 480 GHz/960 GHz can be further studied.
* From [28] WILUS:
  + We propose to support discovery burst transmission window (DBTW) for at least 120kHz SCS which makes it possible to define candidate SSB positions within the DBTW with support of DB which was already agreed.
  + It should be further considered that the additional candidate SS/PBCH block locations within a DBTW can be set to the closest slot locations after LBT failure at candidate SS/PBCH blocks locations as defined in FR2.

#### Summary of Discussions

The following are previous agreements on DRS aspects.

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| **Agreement:**  For an unlicensed band that requires LBT, further study whether/how to support discovery burst (DB) and discovery burst transmission window (DBTW) at least for 120 kHz SSB SCS   * If DB supported   + FFS: What signals/channels are included in DB other than SS/PBCH block * If DBTW is supported   + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs     - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.   + PBCH payload size is no greater than that for FR2   + Duration of DBTW is no greater than 5 ms   + Number of PBCH DMRS sequences is the same as for FR2 * The following points are additionally FFS:   + How to indicate candidate SSB indices and QCL relation without exceeding limit on PBCH payload size   + Details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands * Whether or not to support DBTW for SSB SCS(s) other than 120 kHz if other SSB SCS(s) are supported   **Agreement:**   * For operation with shared spectrum channel access of NR 52.6 – 71 GHz, support discovery burst (DB) and define the DB same as in Rel-16 37.213 Section 4.0 * FFS: Support discovery burst transmission window (DBTW) at least for SSB with 120 kHz SCS with the following requirements   + PBCH payload size is no greater than that for FR2   + Duration of DBTW is no greater than 5 ms   + Number of PBCH DMRS sequences is the same as for FR2   + FFS: applicability of DBTW design for 120kHz to SSB with 480kHz and 960kHz SCS   + Support mechanism to indicate or inform that DBTW is enabled/disabled for both IDLE and CONNECTED mode UEs     - FFS: how to support UEs performing initial access that do not have any prior information on DBTW.     - FFS: details of the mechanism for enabling/disabling DBTW considering LBT exempt operation and overlapping licensed/unlicensed bands     - FFS: details of how to inform UEs of the configuration of DBTW   **Agreement:**  FFS: Support DBTW at least for 120kHz   * FFS whether DBTW will be applicable for 480/960 kHz SSB SCS   + If DBTW is supported for 480/960kHz SSB:     - For the case agreed in RAN1 #104bis-e where 480/960 kHz SSB location and SCS are explicitly provided to the UE (non-initial access), indication of DBTW configuration (e.g. enable/disable of DBTW,  , and DBTW length) are supported by dedicated signaling.  * For 120kHz SSB, support mechanism to distinguish at least the following scenarios:   + Case 1) (Unlicensed with LBT off) + DBTW disabled   + Case 2) (Unlicensed with LBT on) + DBTW enabled   + Case 3) (Unlicensed with LBT on) + DBTW disabled   + Case 4) (Licensed) + DBTW disabled   + FFS: Whether/how LBT on/off is indicated in MIB     - If not indicated in MIB, then FFS whether/how the UE determines different sizes of DCI 1\_0 with CRC scrambled by SI-RNTI   + FFS: whether any case(s) can be combined for DBTW signaling design and how to handle implications to DCI 1\_0 size ambiguity if is not distinguished in signaling   + FFS: whether all above cases need an explicit indication   + FFS: Whether a single indication can be used for combination of more than one cases * For 120 kHz SSB, enable/disable of DBTW is indicated by one or more of the following methods:   + Option 1) signaling in MIB     - Option 1-1) disabling DBTW is jointly coded with  * + - Option 1-2) indicated by other bit fields in MIB     - FFS: among options 1-1 and 1-2   + Option 2) distinct GSCN used by the SSB   + Option 3) By comparing the value of  in MIB and DBTW length after UE reads SIB1 or by comparing the value of  in MIB and default DBTW length of 5 ms before UE reads SIB1.  * + FFS: whether to support option 1, 2, 3, or any combination of the options.   + Note: enable/disable signaling of DBTW by MIB or GSCN does not preclude other signaling methods   **Agreement:**  If DBTW is supported,   * Working assumption: MIB signaling to support   + Alt A) indication of at least for 120kHz SSB  * + - In this case, the total number of values of to not exceed 4  * + Alt B) Explicit indication of SSB index and/or SSB candidate location     - FFS on the details of signaling   + FFS betweenAlt A, or B, or supporting both * Supported DBTW lengths   + Alt 1) 0.5, 1, 2, 3, 4, 5 msec     - Note: same as Rel-16 FR1 NR-U   + Alt 2) maximum 5 msec     - FFS other values   + FFS between Alt 1 and 2 * Number of candidate positions when DBTW is enabled   + For 120kHz SSB     - FFS between 64 or 80   + If DBTW is additionally supported for 480/960kHz SSB     - FFS between 64 or 128 |

The following is a summary of company position of various aspects of DRS.

* Supporting DBTW
  + Support: Huawei/HiSilicon, vivo, Spreadtrum (for 120kHz), Interdigital, Sony, Samsung, CATT(if more than 56 SSB with 120kHz), ZTE/Sanechips, Futurewei (for 120kHz), Nokia, NEC, Panasonic, ETRI, Intel, Sharp (for 120kHz), NTT Docomo, WILUS (for 120kHz)
  + Do not support: Ericsson, CATT (for 480/960kHz) Futurewei (for 480/960kHz), Charter, Qualcomm (for 480/960kHz)
* Indication of licensed and unlicensed operation:
  + Raster: Samsung
  + No distinction: Intel, Qualcomm
* Indication of LBT
  + MIB: Huawei/HiSilicon, Interdigital, CATT, Futurewei
  + Other than MIB (e.g. SIB1): vivo, CATT, Ericsson, Nokia/NSB, Intel, Qualcomm
* Indication of DBTW (for initial access)
  + Implicit:
    - MIB: Huawei/HiSilicon, vivo, Interdigital, Samsung, Intel, ZTE, NEC, Qualcomm, NTT Docomo, Panasonic
    - raster: Interdigital, vivo, Nokia/NSB, LGE
  + Explicit:
    - Sony (jointly coded with ), Futuerwei, Samsung (jointly coded with )
* Supporting means of conveying candidate SSB location & SSB beams
  + Supported values:
    - 2 values: Qualcomm
    - {8,64}: Intel
    - 4 values: Huawei/HiSilicon, Interdigital, Sony, Qualcomm, Intel
    - {4,8,16,64}: Intel
    - {8,16,32,64}: Huawei/HiSilicon, ZTE
    - {16, 32,64,reserved}: Sony (if number of candidate is >64)
    - {8, 16,32,reserved}: Sony (if number of candidate is 64)
  + Support explicit indication of SSB index and/or SSB candidate location
    - Nokia
* Supported DBTW lengths
  + {0.5, 1, 2, 3, 4, 5}msec for all SCS (as in NR-U)
    - vivo, Futurewei, Nokia, Charter (if DBTW is supported), Xiaomi, Qualcomm (120 kHz)
  + 5 msec
    - Intel
  + 120 kHz SCS: {40, 32, 24, 16, 8, 4} slots = {5, 4, 3, 2, 1} ms
    - Huawei/HiSilicon
  + 480 kHz SCS: {72, 32, 24, 16, 8, 4} slots = {2.25, 1, 0.75, 0.5, 0.25, 0.125} ms
    - Huawei/HiSilicon
  + 960 kHz SCS: {64, 32, 24, 16, 8, 4} slots = {1, 0.5, 0.375, 0.25, 0.125, 0.0625} ms
    - Huawei/HiSilicon
* Number of SSB candidates for DBTW
  + For 120kHz:
    - 64: vivo, CATT(for no LBT/no DBTW cases), Futurewei. Charter (if DBTW is supported), NTT Docomo, Xiaomi, Qualcomm, Panasonic
    - > 64: Convida
    - 80: Intel, Sony, CATT (for LBT/DBTW cases), Nokia, NEC
  + For 480kHz:
    - 64: Charter (if DBTW is supported), NTT Docomo, Xiaomi, Qualcomm, Panasonic
    - > 64: Convida
    - 80: Nokia
    - 128: vivo, Intel, Sony, Samsung
* DCI sizes between licensed and unlicensed
  + Same size for DCI 1\_0: Ericsson, Qualcomm, LGE, Intel (for SI-RNTI)
  + Same size for DCI 0\_0: Qualcomm
  + Different size for DCI 1\_0: Apple (if joint encoding of Q and licensed/unlicensed band indication is not possible)

#### **1st Round Discussion:**

Please provide comments on the above summary (including aspects that are missing, aspects captured incorrectly, etc). Moderator will provide a suggested proposal once the summary captures all company opinion correctly.

If the above summary is directly edited (please use a color to highlight changes, e.g. RED) and mention the changes/additions in the comment below.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | * For the number of candidate SSBs, we have a question on the motivation to support at most 64 candidate SSBs when DBTW is on. In our understanding, for FR2-2, there is no strong motivation to support a small number of SSB beams, and very likely in implementation, the number of SSB beams will be larger than 32, then the utilization of DBTW with only 64 candidate SSB locations is indeed limited, and that’s the reason we support more than 64 candidate SSB locations when DBTW is on. * For the SCS applicable to DBTW, we want to address that short control signaling is not globally applicable to all the regions, and there are regions requiring LBT as mandatory procedure for channel access, so the application of DBTW should be for all supported SCSs. Also, some companies mentioned the duty cycle of SSB when using 480/960 is small than the requirement of short control signaling, but it’s not a correct observation. The 20 ms periodicity of SSB is only for initial access and from the UE perspective, but the calculation of duty cycle should be from the cell perspective (i.e., channel utilization). In this sense, if gNB configures a 5 ms periodicity for SSB, there are lots of scenarios for 480/960 kHz SCS cannot satisfy the short control signaling duty cycle. * For the indication of Q, we are not sure whether current MIB can have sufficient number of bits that can be re-interpreted for this purpose. I believe we can utilize similar approach as NR-U: using MIB as the best effort, otherwise use SIB1. * For the DCI 1\_0 size issue, one way is aligning the DCI 1\_0 size for operation with/without shared spectrum channel access, and another way could be indicating operation with/without shared spectrum channel access in MIB (no need to know the value of Q). * We also want a clarification on the proposal of using sync raster to indicate DBTW on/off. In our understanding, DBTW on/off is a semi-static configuration, but sync raster is fixed, so we are not sure how to utilize sync raster to indicate DBTW on/off. Our proposal is to use sync raster to indicate licensed/unlicensed, since it’s a fixed information. |
| Qualcomm | Please see our added support above using “Qualcomm” |
| Panasonic | Please see our added support above using “Panasonic” |

### 2.1.2 SSB Resource Pattern

* From [1] Huawei/HiSilicon:
  + Support following patterns for SSB with 480 kHz and 960 kHz SCS:
    - For operations without shared spectrum:
      * {2,9}+14n, (n=0,1,2,…,31) for both 480 kHz and 960 kHz SCS.
    - For operations with shared spectrum:
      * {2,9}+14n, (n=0,1,2,…,31,40,…,71) for 480 kHz SCS;
      * {2,9}+14n, (n=0,1,2,…,63) for 960 kHz SCS.
* From [2] vivo:
  + For initial cell search in 52.6-71GHz, a UE may assume that half frames with SSB occur with smaller period than FR2 (e.g. 5ms), or lower RAN4 requirement for the cell search time.
  + If CP length of at least one SCS (e.g. 960K) can’t afford beam switching time that is finally determined in RAN4, the following way could be considered for ALT1 and ALT2 respectively:
    - For ALT1, leave enough time gap between any consecutive candidate SSBs by specifying proper value of X and Y;
    - For ALT2, the same QCL (i.e. the same beam) for contiguous candidate SSBs is assumed to achieve time gap for any consecutive candidate SSBs with different QCL assumption.
  + The exact value of ‘n’ should be determined after RAN4 concludes the exact DL-UL switching time for NR operation in FR2-2.
* From [3] Spreadtrum:
  + The SSB pattern for SSB with 480/960kHz SCS can reuse Case A/C in the current spec, i.e. ALT 1) with X=2 and Y=8.
* From [4] Interdigital:
  + Support Alt 1 for the SSB resource patterns for 480/960kHz SCS SSB blocks.
    - First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame. value of X and Y are identical for 480kHz and 960kHz
* From [5] Sony:
  + Candidate SSB positions should be extended when DBTW is enabled.
    - For 120 kHz SCS,
      * The number of candidate SSB positions should be 80
      * additional n values (4, 9, 14, 19) should be supported when DBTW is enabled
    - For 480/960 kHz SCS,
      * The number of candidate SSB positions should be 128
      * First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
      * n = {0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18} when DBTW is disabled.
      * n = 0 - 31 when DBTW is enabled
* From [6] Lenovo/Motorola Mobility
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, for higher subcarrier spacings (numerologies) such as 960kHz for SSB, to allow the beam switching between contiguous SSBs, a gap (for example a symbol gap or post-fix) should be supported before beam switching at least for 960kHz
* From [7] Samsung:
  + For 480 kHz and 960 kHz,
    - Support the same SS/PBCH block pattern in a slot, and the same pattern is given by Case A/C (i.e., Alt 1 with X=2 and Y=8).
    - Support larger number of slots including candidate SS/PBCH block, when DBTW is enabled.
* From [8] CATT:
  + For SSB pattern, considering SCS= 960KHz SSB is not supported for initial access，ALT-2 is preferred.
    - ALT 2) First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
  + More than 64 SSB transmission opportunities shall be defined within a 5ms SSB burst set to support up to 64 beams for SSB beam sweeping in case of LBT failure. The issue of supporting additional bit(s) for the indicating SSB candidate index needs further study.
  + For no-LBT operation or licensed spectrum operation, value “n” can keep the same value as for the 120KHz SCS case.
  + Additional n value such as #4, #9, #14, and #19 can be used for new SSB candidates if LBT/DBTW is needed for SSB transmission.
  + For up to 71GHz operation and at least for NO-LBT operation, some values of ‘n’ can be reserved for uplink grant scheduling.
* From [9] ZTE/Sanechips:
  + For SSB with 120kHz SCS for NR 52.6 GHz to 71 GHz: the first symbols of the candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n, where index 0 corresponds to the first symbol of the first slot in a half-frame. For carrier frequencies within 52.6 GHz to 71GHz,
    - if DBTW is not supported or disabled, 𝑛 = 0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18
    - if DBTW is enabled, the additional n values can be equal to 4, 9, 14, 19 to define 16 additional candidate SSB positions
  + For 480kHz/960kHz SSB, the following alternatives can be considered:
    - Alt 1: First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
      * value of X and Y are identical for 480kHz and 960kHz
        + X=2, Y=8
      * if DBTW is not supported or DBTW is disabled
        + For 480kHz SCS, the 64 candidate SSBs are located in 32 slots, with 2 slots spacing between every 8 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17, 20, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36, 37
        + For 960kHz SCS, the 64 candidate SSBs are located in 32 slots, with 4 slots spacing between every 16 consecutive slots to avoid prolonged occupation, i.e. n=0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35
      * if DBTW is supported and it is enabled
        + Additional 64 candidate SSB can be defined after the above original 64 candidate SSB in the half frame
    - Alt 2: First symbols of the candidate SSB have index {4, 8, 16, 20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
      * if DBTW is not supported or DBTW is disabled
        + For 480kHz SCS, the 64 candidate SSBs are located in 32 slots (i.e. 16 slot pairs, where 1 slot pair = 2 slots), with 2 slots spacing between every 4 consecutive slot pairs to avoid prolonged occupation, i.e n=0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18
        + For 960kHz SCS, the 64 candidate SSBs are located in 32 slots (i.e. 16 slot pairs, where 1 slot pair = 2 slots), with 4 slots spacing between every 8 consecutive slot pairs to avoid prolonged occupation, i.e n=0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 16, 17
      * if DBTW is supported and it is enabled
        + Additional 64 candidate SSB can be defined after the above original 64 candidate SSB in the half frame
  + The following options can be considered for supporting beam switching for SSB with SCS 480 kHz and 960 kHz if the CP cannot cover beam switching and other functions simultaneously.
    - Option 1: In a half-frame, any two candidate SSBs are discontinuous in the time domain
    - Option 1-1: SSB pattern with SCS 480/960 kHz can adopt the existing pattern of Case A and Case C in one or two slots defined in Rel-15 NR
    - Option 1-2: SSB pattern with SCS 480/960 kHz should be re-designed to reserve at least one symbol between any two candidate SSBs, e.g. only defining one candidate SSB per slot, or shift the existing SSB by one or more symbols
    - Option 2: Multiple adjacent candidate SSBs are defined to have a same SSB index or QCL assumption
  + In order to reduce the impact of standardization caused by indicating candidate SSB indices, the maximum number of candidate SSB defined in the half-frame can be kept unchanged (maintain 64) or limited to 128 for 480/960 kHz SSB SCS.
* From [11] Ericsson:
  + For SS/PBCH block with 120 kHz SCS, support Case D pattern as defined in Rel-15. No new values of n are supported.
  + Pending confirmation from RAN4 on 59 ns beam switching times, support the FR2 Case D pattern (ALT 2) for time domain pattern for SSB transmissions with 480 kHz and 960 kHz SCS.
  + Conclude that no additional (compared to the already supported 64) candidate SS/PBCH block positions are introduced.
* From [13] Nokia/NSB:
  + Make a working assumption that no beam switching gap need to be assumed between consecutive SSBs at 480kHz and 960kHz sub-carrier spacing.
  + Support in for 480kHz and 960kHz SSB pattern design empty slots without SSB candidate locations at 0.25ms.
  + Define SSB slot patter for 480kHz and 960kHz sub-carrier spacing so that 8 consecutive slots are contain SSB candidate locations, followed by 4 slots are left unoccupied (by SSBs), until all SSBs locations are accounted
    - The slot indexes n={0,1,2,3,4,5,6,7,
      * 12,13,14,15,16,17,18,19,
      * 24,25,26,27,28,29,30,31,
      * 36,37,38,39,40,41,42,43}
    - Note: The additional candidate locations for DBTW are not accounted above.
  + Define SSB symbol level pattern for 480kHz and 960kHz so that first symbols of the candidate SSB locations are {2,8}+14\*n
    - where index 0 corresponds to the first symbol of the first slot in a half-frame, and n is the corresponding SSB slot index
  + For 120kHz SSB pattern, introduce additional candidate locations for SSB transmission support for 𝑛 = 4, 9, 14, 19, where n is the slot index in half-frame.
    - The first symbols of the additional candidate SS/PBCH blocks have indexes {4, 8,16, 20} + 28×n.
  + For 480kHz and 960kHz SSB pattern, introduce additional candidate locations for SSB transmission support for 𝑛 = [{8, 9, 10, 11} ,{32,33,34,35}], where n is the slot index in half-frame.
* From [14] Charter:
  + Support Alt-1 for 480/960 kHz SSB with first symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame. The value of n is the same for LBT and no-LBT operation.
* From [16] Panasonic:
  + For SSB symbol position, Case D SSB pattern is reused (i.e., Alt 2).
  + For SSB slot position, Case D SSB patten is reused (i.e., n = 0, 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 15, 16, 17, 18).
* From [17] OPPO:
  + for SSB pattern design, support Alt-1 {X,Y}+14\*n, with X=1, Y=8.
  + for SSB candidate number within half frame, support the followings
    - For 480kHz, SSB candidate index {1,8}+14\*n, with n=0~63
    - For 120kHz, SSB candidate index {4, 8,16, 20} + 28\*n, with n=0~19
* From [18] Qualcomm:
  + for 480kHz/960kHz SSB, select the following alternative:
    - ALT 1) First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
      * value of X and Y are identical for 480kHz and 960kHz
      * X = 2 and Y = 9
      * Values of ‘n’ shall not be all consecutive integer values (i.e. non-candidate SSB slots are positioned every few candidate SSB slots)
* From [19] LG Electronics:
  + Support of additional n values for the time domain pattern of SS/PBCH block with 120 kHz SCS can be considered to increase SS/PBCH block’s transmission opportunities, only if PBCH payload is sufficient to indicate the increased number of candidate SS/PBCH block indexes.
  + For 480/960 kHz SSB, first symbols of the candidate SSB have index are {4, 8, 16, 20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame (i.e., Alt 2 in previous agreement), and values of ‘n’ are consecutive integers (i.e., n = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15).
* From [20] ETRI:
  + Prefer to keep the current 64 SSB candidate positions for 120kHz.
  + Propose to support ALT 1 as SSB patterns for 480kHz and 960kHz SSB.
    - Details on values for X, Y, and n should be further studied.
* From [21] Mediatek:
  + For SSB SCS=120 kHz, additional SSB candidate positions is not needed.
  + For SSB SCS=480/960 kHz, Alt 2 should be supported as the baseline scheme.
* From [22] Intel:
  + Consider at least 1 symbol gap between consecutive SSBs within a slot.
  + Consider at least 1 symbol gap between SSB and the start of the next slot, where PDCCH could be transmitted.
  + Consider SSB pattern in a slot with 3 SSB containing slots, each slot with 2 SSB position, followed by 1 non-SSB carrying slot for 480 kHz and 6 SSB carrying slots followed by 2 non-SSB carrying slots for 960kHz, to accommodate Rx-Tx switching gap.
    - For 480kHz and 960kHz SCS based SSB, first symbols of the candidate SSB have indexes {2,9} + 14×n, where index 0 corresponds to the first symbol of the first slot in a half-frame.
    - For 480kHz, n = {0,1,2, 4,5,6, 8,9,10, 12,13,14, 16,17,18, 20,21,22, 24,25,26, 28,29,30, 32,33,34, 36,37,38, 40,41}, {42, 44,45,46, 48,49,50, 52,53,54, 56,57,58, 60,61,62, 64,65,66, 68,69,70, 72,73,74, 76,77,78, 80}.
      * The second set of n values could be used to enable larger number of candidate SSBs, i.e.,
    - For 960kHz, n = {0,1,2,3,4,5, 8,9,10,11,12,13, 16,17,18,19,20,21, 24,25,26,27,28,29, 32,33,34,35,36,37, 40,41}, {42,43,44,45, 48,49,50,51,52,53, 56,57,58,59,60,61, 64,65,66,67,68,69, 72,73,74,75,76,77, 80,81,82,83}.
      * The second set of n values could be used to enable larger number of candidate SSBs, i.e.,
* From [23] Apple:
  + Support to introduce a unified SSB Pattern for 480kHz SCS and 960kHz SCS (if supported):
    - The first symbol of candidate SSB have indexes {2,9,16,23} within each SSB burst.
    - Reserve 2 slots for DL/UL and UL/DL switching to allow for fast UL transmission between two SSB bursts.
* From [24] Sharp:
  + Based on SSB resource pattern Case D of FR2, other values of n (e.g., 4, 9, 14, 19) should be added for the SSB with 120kHz SCS in above 52.6GHz.
* From [25] NTT Docomo:
  + On down-selection regarding SSB symbol definition, whether to reuse Case D should be discussed considering whether to practically support SSB-CORESET#0 multiplexing within the same slot
  + With 120 kHz SCS, ‘n’ value(s) which can be added on top of the ones agreed already are limited, i.e., ‘n’ = {4, 9, 14, 19} only
  + With 120 kHz SCS, no significant need to support additional ‘n’ values on top of the ones agreed already
  + With 480/960 kHz SCS, non-consecutive SSB slots should be defined to e.g., make UL transmissions possible in the middle of SSB burst.
    - Larger number of consecutive non-SSB slots can be defined during SSB burst can be defined to obtain scheduling flexibility of a DCI (e.g., with repetition and/or multi-PDSCH/PUSCH scheduling)
  + With 480/960 kHz SCS, not support more than 64 candidate SSB positions
* From [26] Xiaomi:
  + For 480 kHz SSB design, we support the option 1 and the n should be no difference for LBT/no LBT operation.
    - [Moderator Note: This might be Alt 1, instead of option 1]
* From [28] WILUS:
  + At least one symbol gap in time domain between SS/PBCH blocks with different SSB indices should be considered for higher subcarrier spacing by taking a beam switching gap into account due to a RF interruption time of Tx/Rx beams and/or LBT gap in unlicensed spectrum.
  + We prefer to have Alt-1 of two alternatives for SS/PBCH block pattern in time domain
    - ALT 1) First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame
    - value of X and Y are identical for 480kHz and 960kHz
      * FFS: exact value of X and Y

#### Summary of Discussions

In RAN1 #105e the following agreement was made.

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| **Agreement:**  For 480kHz/960kHz SSB, select one of the following alternatives:   * ALT 1) First symbols of the candidate SSB have index {X, Y} + 14\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame   + value of X and Y are identical for 480kHz and 960kHz     - FFS: exact value of X and Y * ALT 2) First symbols of the candidate SSB have index {4, 8, 16,20} + 28\*n, where index 0 corresponds to the first symbol of the first slot in a half-frame * Values of n for 480kHz and 960kHz for ALT 1 and 2   + FFS: whether number of values for ‘n’ depend on LBT operation (i.e. LBT vs no-LBT)   + FFS: exact values of ‘n’ for each SCS   + Values of ‘n’ for one mode of operation shall be strictly a subset of values for another mode of operation, if two mode of operation exist for number of candidate SSBs   + FFS: whether values of ‘n’ shall not be all consecutive integer values (i.e. non-candidate SSB slots are positioned every few candidate SSB slots) |

* SSB pattern for 480/960kHz
  + ALT 1)
    - {X, Y} + 14\*n
      * Interdigital, [Lenovo/Motorola Mobility], Charter, ETRI, [Xiaomi], WILUS
    - (Alt 1-A) {2, 9} + 14\*n



* + - * Huawei/HiSilicon, Qualcomm, Intel, [Apple], Samsung
    - (Alt 1-B) {1,8} + 14\*n



* + - * OPPO, Samsung
    - (Alt 1-C) {2, 8} + 14\*n



* + - * Spreadtrum, Samsung, ZTE/Sanechips, Nokia/NSB
  + ALT 2) Case D {4, 8, 16,20} + 28\*n



* + - Sony, CATT, ZTE/Sanechips, Ericsson, Panasonic, LGE, Sharp
* Supported values of ‘n’
  + Several companies suggested to have few slots that does not have SSB candidates every few slots that have SSB candidates.
  + Moderator notes that supported values of ‘n’ seems to be heavily dependent on DBTW discussion, and therefore suggest to discuss in Section 2.1.1.

#### **1st Round Discussion:**

Moderator suggest to discuss further based on the alternatives presented (above). Also moderator asks if companies who expressed opinion on ALT 1, can support one of the patterns suggested by companies or not.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | * We support Alt 1-C since it’s one of the supported pattern in Rel-15. We are also supporting Alt 1-A or Alt 1-C if any of them can get consensus. Comparing the three alternatives in Alt 1, Alt 1-A is the best, but we discussed this issue before in Rel-16 NR-U… * For Alt 2, our concern is this pattern is not compatible with the Type0-PDCCH configuration in MIB, i.e., a Type0-PDCCH starting from symbol 7 has collision with the SSB symbol. Also, we want to point out that this pattern is mainly for mixed numerology multiplexing, but this is not a design target in FR2-2. |
| Qualcomm | We are supportive of Alt 1-A ({2, 9} + 14\*n) for the following reasons:   * Allow for gNB beam switching gaps (for slower gNBs)   Allow for possibility of back-to-back multiplexing of CORESET0 + SSB of the same beam (2 symb CORESET0 beam 1 + 4 symb SSB beam 1 + GAP + 2 symb CORESET0 beam 2 + 4 symb SSB beam 2) |
| Panasonic | We think the necessity of a gap symbol due to beam switching time needs to be clarified. According to agreed LS in RAN4(R4-2107985), RAN4 tentatively agreed [59 ns] for gNB beam switching time. “59 ns” fulfils the condition where no explicit switching gap is needed between consecutive SSBs for 960 kHz SCS according to TR38.808 section 4.2.2.4. Thus, we support Alt 2 because potential specification works can be reduced. If a gap symbol is needed due to other factors (e.g., UE Rx beam switching time), we slightly prefer Alt 1-A taking into account allocating a gap symbol and PDCCH between SSBs. |

### 2.1.3 CORESET#0 Configuration

* From [1] Huawei/HiSilicon:
  + For CORESET for Type0-PDCCH in 52.6GHz to 71GHz spectrum, support the following:
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {120, 120} kHz, support multiplexing pattern 1 and multiplexing pattern 3 as per Agreement in RAN1 104-e.
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {480, 480} kHz, support multiplexing pattern 1 only.
    - For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {960, 960} kHz, support multiplexing pattern 1 only.
  + For {SS/PBCH Block, CORESET for Type0-PDCCH} SCS equal to {120, 120} kHz, in addition to the supported values of (, ) from Rel-15, support with .
  + Support the following CORESET#0 RB offsets values for {SSB, CORESET#0} SCS={120, 120} kHz:
    - For CORESET#0 with 24 RBs and 48 RBs: the same as supported values in Table 13-8 of 38.213.
    - For CORESET#0 with 96 RBs: 0, 38, 76 RBs for multiplexing pattern 1 and -20 (-21) RBs when for multiplexing pattern 3.
    - Note: All above RB offsets are nominal and may need to be modified after finalizing synch raster and channel raster design in FR2-2.
  + Support at least the following combinations in 52.6GHz to 71GHz spectrum:
    - for {SSB, CORESET#0} ={480, 480} kHz with multiplexing pattern 1, , ={1,2};
    - for {SSB, CORESET#0} ={960, 960} kHz with multiplexing pattern 1, , ={1,2}.
  + To find the offset between an off-synch raster SSB and the corresponding CORESET#0 in 60GHz unlicensed spectrum, RAN1 should uniquely determine the hypothetical on-synch raster SSB that serves as the reference for the offset to the off-synch raster SSB in case more than one synch rasters are included in a channel bandwidth.
* From [2] vivo:
  + Dedicated signalling can’t be used for conveying the Type-0 PDCCH configuration to read the SIB1.
  + The following SSB-Coreset 0 multiplexing patterns are supported for each SCS pair when operation in FR2-2 (52.6-71GHz):
    - (120K, 120K): Pattern 1, Pattern 3
    - (480K, 480K): Pattern 1, Pattern 3
    - (960K, 960K): Pattern 1, Pattern 3
  + For {SSB, PDCCH} SCS {120, 120} kHz, {480, 480} kHz and {960, 960} kHz in licensed band, the tables for CORESET#0 and type0-PDCCH CSS set configuration defined for FR2-1 in Rel-15 can be reused.
  + For the un-licensed band operation from 52.6GHz to 71GHz, the CORESET design principle should consider two aspects: 1. Occupy as much bandwidth as possible; 2. Use as few bits as possible in the CORESET configuration.
  + For {SSB, PDCCH} SCS {120, 120} kHz, {480, 480} kHz and {960, 960} kHz, the tables for PDCCH monitoring occasions for type0-PDCCH CSS set configuration defined for FR2-1 in Rel-15 can be reused with little adjustment.
* From [3] Spreadtrum:
  + The mechanism of two offsets in MIB defined for NR-U, i.e. Alt 2 (use configuration in MIB to support CORESET#0/Type0-PDCCH), can be reused for UE to determine CORESET#0/Type0-PDCCH.
* From [4] Interdigital:
  + Support Alt 2 on using the CORESET#0/Type0-PDCCH configuration in MIB.
  + Introduce the enhancements on SS/PBCH block transmission patterns to deliberately include the CORESET#0 and SIB1 in fixed time locations along with the corresponding SS/PBCH block to ensure the channel occupancy as much as possible, in the initial access operations for unlicensed spectrum in beyond 52.6GHz.
* From [7] Samsung:
  + For SS/PBCH block with 120 kHz SCS,
    - only support CORESET#0 SCS as 120 kHz;
    - additional CORESET#0 RB offsets are needed;
    - support 96 RB as the number of RBs for CORESET#0.
  + For SS/PBCH block with 480 kHz SCS and 960 kHz,
    - only support CORESET#0 SCS same as SS/PBCH block SCS;
    - support at least the same SS/PBCH block and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, and number of symbols as in 120 kHz SCS;
    - support 96 RB as the number of RBs for CORESET#0;
    - Further study the RB offset based on RAN4 design of channel and synchronization rasters.
* From [8] CATT:
  + Multiplexing pattern 2 or 3 can be used for further multiplexing SSB/CORSET#0 with periodic CSI-RS/paging PDCCH&PDSCH in frequency.
  + For SSB and CORESET#0/Type0-PDCCH with 120 KHz SCS, support the following combinations of SSB/CORESET multiplexing pattern, number of RB and symbols for CORESET.
    - {mux pattern 1, 48 PRB CORESET, 1 symbol CORESET}
    - {mux pattern 1, 48 PRB CORESET, 2 symbol CORESET}
    - {mux pattern 3, 48 PRB CORESET, 2 symbol CORESET}
* From [9] ZTE/Sanechips:
  + The multiplexing pattern 1 and 3 for three approved SCS combinations of SSB and Type0-PDCCH can be considered for Rel-17 NR above 52.6 GHz.
    - (SSB, Type0-PDCCH): SCS (120 kHz, 120 kHz)
    - (SSB, Type0-PDCCH): SCS (480 kHz, 480 kHz)
    - (SSB, Type0-PDCCH): SCS (960 kHz, 960 kHz)
  + For {SSB, CORESET#0 for Type0-PDCCH} SCS = {120, 120} kHz, even though RAN4 has agreed the minimum CBW is increased to 100 MHz, at least SSB and CORESET#0 multiplexing patterns, number of RBs for CORESET#0, number of symbols (duration of CORESET#0) that are supported in Rel-15/16 should still be supported.
* From [11] Ericsson:
  + RAN1 should strive to design a common CORESET0 configuration table for use for all 3 supported SCS combinations (120,120), (480,480), and (960, 960).
  + Reuse existing Table 13-12 in 38.213 for operation with 480 and 960 kHz SCS. For subcarrier spacings 480 and 960 kHz. Use and , respectively, instead of when determining the PDCCH monitoring occasions using offset values from the table.
* From [12] Futurewei:
  + In FR2-2 CORESET#0, PDCCH SIB1 support the same SCS as the SCS for SS/PBCH.
* From [13] Nokia/NSB:
  + Consider also SSB and CORESET#0 multiplexing pattern 3 for 120kHz SSB.
  + Pending on the UE minimum BW capability, consider also SSB and CORESET#0 multiplexing pattern 3 for 480kHz SSB.
  + For CORESET#0 with 120kHz sub-carrier spacing, consider supporting also ={96} for multiplexing pattern 1.
  + For SSB and CORESET#0 with 480kHz sub-carrier spacing with SSB and CORESET#0 multiplexing pattern 1, support following options:
    - ={[1],2, 3}
    - ={24, 48}.
  + For SSB and CORESET#0 with 480kHz sub-carrier spacing with SSB and CORESET#0 multiplexing pattern 3, following configuration options could be considered:
    - ={1,2}
    - ={24, 48}.
  + For SSB and CORESET#0 with 960kHz sub-carrier spacing, with SSB and CORESET#0 multiplexing pattern 1 support
    - ={2, 3}.
    - ={24}.
* From [18] Qualcomm:
  + for FR2-2, CORESET0 SCS = SSB SCS for all SCSs
  + consider minimizing the overhead of beam switching gaps by:
    - Supporting multiplexing pattern 3
    - Introducing an SSB/CORESET0 multiplexing pattern for higher SCS SSB (480 and 960 kHz), where TDM grouping of the SSB and the corresponding CORESET0 is considered
* From [19] LG Electronics:
  + Reuse Table 13-8 in TS 38.213 specification for CORESET#0 configuration with 120/480/960 kHz, except for RB offset values.
  + Reuse Table 13-12 in TS 38.213 specification for type0-PDCCH CSS set configuration with 120/480/960 kHz, except for O values for 480/960 kHz.
* From [21] Mediatek:
  + Support only 1 SCS for CORESET#0/Type0-PDCCH for a given SSB SCS.
* From [22] Intel:
  + Consider using Type0-PDCCH search space in symbols {0,1} and {7, 8} for each SSB.
* From [23] Apple:
  + In addition to 24 and 48 PRBs, 96 PRBs can be considered for CORESET#0 BW with 120kHz SCS.
* From [25] NTT Docomo:
  + On down-selection regarding SSB symbol definition, whether to reuse Case D should be discussed considering whether to practically support SSB-CORESET#0 multiplexing within the same slot
  + With all SCSs supported in 52.6 – 71 GHz and with the restriction agreed in RAN#91-e, the existing SSB-CORESET#0 multiplexing pattern 1 specified in 38.213 with Table 13-8 and 13-12 works as it is.
    - Feasibility of a certain case, where e.g., 2 pairs of {Type0-PDCCH, SIB1 PDSCH} are allocated in a slot, is not clear
    - With 960 kHz SCS, smaller ’O’ value can be added considering shorter time duration SSB beam sweeping
* From [26] Xiaomi:
  + It should be clarified that {480,120} kHz combination of SSB with CORESET#0/Type0-PDCCH SCS is not supported.
* From [28] WILUS:
  + We propose that SS/PBCH block and CORESET#0/RMSI can be multiplexed in TDM/FDM within a slot considering multi-beam operation and it can be closely located without the gap between SSB and CORESET#0/RMSI for not allowing any in-between channel access operation in the unlicensed band.

#### Summary of Discussions

The following are a summary of company views on CORESET#0 configuration aspects.

* For {SSB, CORESET#0/Type0-PDCCH} = {120, 120} kHz
  + controlResourceSetZero
    - Addition of 96 PRB CORESET#0
      * Support: Huawei/HiSilicon, Samsung, Nokia/NSB, Apple
      * Do not support:
* For {SSB, CORESET#0/Type0-PDCCH} = {480, 480} kHz
  + controlResourceSetZero
    - Support {24, 48} PRB with {1,2} symbol durations
      * Huawei/HiSilicon
    - Use Table 13-8 (originally intended for {120,120} kHz) except RB offset
      * {mux pattern 1, 24 PRB, 2 symbol}
      * {mux pattern 1, 48 PRB, 1 symbol}
      * {mux pattern 1, 48 PRB, 2 symbol}
      * {mux pattern 3, 24 PRB, 2 symbol}
      * {mux pattern 3, 48 PRB, 2 symbol}
      * [vivo], ~~[~~Samsung (with 96 RB as well)~~]~~, [Ericsson], LGE, NTT Docomo, Qualcomm
    - Support mux pattern 1 with {24, 48} PRB and {[1],2,3} symbol duration
      * Nokia/NSB
    - Support mux pattern 3 with {24, 48} PRB and {1,2} symbol duration
      * Nokia/NSB, Samsung
    - Support mux pattern 3
      * Qualcomm, Samsung
  + searchSpaceZero
    - Use Table 13-12 (originally intended for {120,120} kHz)
      * NTT Docomo
    - Use Table 13-12 (originally intended for {120,120} kHz) except O values
      * LGE, Samsung
    - Use symbols {0,1} and {7,8} for Type0-PDCCH for each SSB
      * Intel, Qualcomm
* For {SSB, CORESET#0/Type0-PDCCH} = {960, 960} kHz
  + controlResourceSetZero
    - Support {24} PRB with {1,2} symbol durations
      * Huawei/HiSilicon
    - Use Table 13-8 (originally intended for {120,120} kHz) except RB offset
      * {mux pattern 1, 24 PRB, 2 symbol}
      * {mux pattern 1, 48 PRB, 1 symbol}
      * {mux pattern 1, 48 PRB, 2 symbol}
      * {mux pattern 3, 24 PRB, 2 symbol}
      * {mux pattern 3, 48 PRB, 2 symbol}
      * [vivo], ~~[~~Samsung (with 96 RB as well)~~]~~, [Ericsson], LGE, NTT Docomo, Qualcomm [24 RB only]
    - Support mux pattern 1 with {248} PRB and {2,3} symbol duration
      * Nokia/NSB, Samsung
    - Support mux pattern 3
      * Qualcomm, Samsung
  + searchSpaceZero
    - Use Table 13-12 (originally intended for {120,120} kHz)
      * NTT Docomo
    - Use Table 13-12 (originally intended for {120,120} kHz) except O values
      * LGE, Samsung
    - Use symbols {0,1} and {7,8} for Type0-PDCCH for each SSB
      * Intel, Qualcomm

#### **1st Round Discussion:**

There were some suggestions on mux pattern 3 support. Since the updated WID explicitly mentions to prioritize mux pattern 1, moderator suggests it is suggested to discuss mux pattern 1 aspects first and once concluded continue further discussion mux pattern 3 aspects.

Companies are asked to comment further on the following issues:

Q1) addition of 96 PRB CORESET#0 for {120kHz, 120kHz}={SSB, PDCCH} pair to ‘controlResourceSetZero’ field

Q2) Supported PRB and symbol duration with mux pattern 1 for {480kHz, 480kHz}={SSB, PDCCH} pair and {960kHz, 960kHz}={SSB, PDCCH} pair

Q3) supported search space configurations for {480kHz, 480kHz}={SSB, PDCCH} pair and {960kHz, 960kHz}={SSB, PDCCH} pair. For example, whether Table 13-12 can be used with little or no modifications.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | Q1) We support adding 96 RB CORESET#0 for better coverage.  Q2) The same RB and symbol duration with Pattern 1 for {120, 120} can be supported for {480, 480} and {960, 960}.  Q3) Table 13-12 can be used as a baseline with necessary modifications, e.g. the O value. |
| Qualcomm | Q1: we do not think there is a strong need to introduce 96 RB option, however, it can be considered if needed  Q2:   * For 480 + 480 kHz: support the same combinations as for 120 + 120 kHz   + 24 RB + 2 symbols   + 48 RB + 1 or 2 symbols * For 960 + 960 kHz: due to min UE BW constraint (400 MHz) and to compensate for coverage,   + 24 RB + 1 or 2 or [3] symbols   Q3: Start with table 13-12 as baseline. However, for the values of “O”, since the SSB beam sweep time for 480 and 960 kHz is short (1 and 0.5 ms), the values of “O” of 2.5, 5, and 7.5 ms may be too long and we may to consider some reduction factor.  In addition, we can also support “Use symbols {0,1} and {7,8} for Type0-PDCCH for each SSB” as indicated above using “Qualcomm” |

### 2.14 ANR/CGI Reporting Aspects

* From [4] Interdigital:
  + Consider introducing the parameters for the neighbor cell SIB1 related to CGI reporting, where the time and frequency allocations and the multiplexing patterns are (pre)configured in fixed settings.
* From [7] Samsung:
  + No need to support extra method for providing the CORESET#0/Type0-PDCCH configuration for ANR purpose.
* From [8] CATT:
  + There is no need to study additional method(s) to enable support to obtain neighbor cell SIB1 contents related to CGI reporting in Rel-17.
* From [17] OPPO:
  + For ANR design, RAN1 considers one of the two options
    - Option 1: RAN1 holds ANR discussion until RAN4 concludes the channelization, LBT bandwidth and sync raster relationship.
    - Option 2: RAN1 does not follow R16 baseline solution and redesign ANR.
* From [18] Qualcomm:
  + for ANR, do not consider additional methods (compared to current NR) to signal the NCGI

#### Summary of Discussions

The updated WID contains FFS on additional method(s) to enable support to obtain neighbor cell SIB1 contents related to CGI reporting.

Three companies mentioned there is no need to consider further, and two companies mentioned methods to support CGI reporting.

#### **1st Round Discussion:**

Further discuss on “FFS: additional method(s) to enable support to obtain neighbour cell SIB1 contents related to CGI reporting”.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | We don’t think additional method for CGI reporting is needed.   * First, in the CGI reporting scenario, the serving operator may not have information on the configuration of CORESET#0/Type0-PDCCH of a neighboring operator, so the feasibility of the additional method (e.g. dedicated signaling) is concerned. * Secondly, even if the serving operator knows such CORESET#0/Type0-PDCCH configuration, the dedicated signaling can only provide the same information as the indication in the MIB, otherwise such SSB cannot be used as cell-defining SSB for the neighboring operator. * Lastly, the UE anyway needs to read MIB of the SSB from the neighboring cell, e.g. to acquire timing and other information in MIB, so there is no need to have an additional method to provide the CORESET#0/Type0-PDCCH configuration. |
| Qualcomm | Current NR support is enough and there may not be a need to have any additional methods to support signaling the NCGI |
| Fujitsu | We share the views that no additional signaling on top of MIB is needed for providing CORESET#0/Type0-PDCCH configuration. However, some enhancements on providing CORESET#0/Type0-PDCCH configuration by MIB of off-sync SSB may be needed.  In NR-U, the MIB of an off-sync SSB provides CORESET#0/Type0-PDCCH CSS set configuration based on a nominal SSB on the sync raster in the channel where the off-sync SSB is transmitted. It is feasible since each channel includes one and only one sync raster. But for FR2-2, the relation between channels and sync rasters may be different and thus enhancement for off-sync SSB may be needed. Considering that channels and sync rasters are still under discussion, this discussion point could be deprioritized at the current stage. |

### 2.1.5 Various other aspects on SSB Design

* From [3] Spreadtrum:
  + SSB with 240kHz SCS can be down-prioritized.
  + Supporting initial cell selection with 480kHz SSB should be an optional UE capability separately from supporting other processing with 480/960kHz SCS.
* From [6] Lenovo/Motorola Mobility
  + For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, with higher subcarrier spacings (numerologies), coverage enhancement of channels and signals used for initial access should be considered for NR beyond 52.6 GHz
* From [17] OPPO:
  + The raster step size for 120kHz and 480kHz are 3\*17.28MHz and 15\*17.28MHz, respectively, leading to a total number of raster entries 428.
* From [19] LG Electronics:
  + Discuss how to signal actually transmitted SSBs via ssb-PositionsInBurst when can be indicated to be less than 64 in MIB.
* From [27] Convida:
  + SSB coverage enhancement should be studied for higher SCS.

#### Summary of Discussions

* Companies have provided the following issues
  + Capability
    - Supporting initial cell selection with 480kHz SSB should be an optional UE capability separately from supporting other processing with 480/960kHz SCS.
  + Coverage enhancement
    - For supporting NR from 52.6 GHz to 71 GHz in Rel. 17, with higher subcarrier spacings (numerologies), coverage enhancement of channels and signals used for initial access should be considered for NR beyond 52.6 GHz
    - SSB coverage enhancement should be studied for higher SCS.
    - Note from Moderator: WID explicitly mentions “Note: coverage enhancement for SSB is not pursued.”, therefore not sure if this needs to be further discussed.
  + Raster
    - The raster step size for 120kHz and 480kHz are 3\*17.28MHz and 15\*17.28MHz, respectively, leading to a total number of raster entries 428.
  + ssb-PositionsInBurst
    - Discuss how to signal actually transmitted SSBs via ssb-PositionsInBurst when can be indicated to be less than 64 in MIB

#### **1st Round Discussion:**

Among the additional issues brought up, Moderator assumes that coverage aspects are excluded by the WID and raster issues are for discussion in RAN4 domain. Moderator suggest to further discuss on the two issues brought up.

* Initial cell selection capability for 480kHz
* Signaling for ssb-PositionsInBurst when is indicated.

If there are other issues that require further discussion, please comment here as well.

|  |  |
| --- | --- |
| Company | Comments |
| Samsung | * The capability of 480 kHz for initial access can be discussed in a later phase of the WI (anyway do not impact RAN1 progress). * The indication and interpretation of ssb-PositionsInBurst can be discussed later when the DBTW is finalized. |
|  |  |

## 2.2 PRACH Aspects

### 2.2.1 PRACH Sequence and Format

* From [2] vivo:
  + Support 120KHz and 480KHz as candidate SCS of initial UL BWP.
  + Support 480KHz and 960KHz SCS in addition to 120KHz SCS for PRACH.
* From [7] Samsung:
  + Support short PRACH format for all PRACH sequence lengths and all SCSs , and don’t support long PRACH format.
* From [8] CATT:
  + Consider supporting increasing symbols in time domain to enhance PRACH coverage.
  + Consider repeating and concatenating the PRACH preamble sequence to enhance PRACH coverage for unlicensed spectrum operation.
* From [9] ZTE/Sanechips:
  + Support PRACH with additional SCSs (480 kHz and/or 960 kHz) for both initial and non-initial access cases.
  + For 480kHz and 960kHz, reuse the same RO configuration table as in Rel-15/16 with the same RO density for 120kHz PRACH.
* From [11] Ericsson:
  + For PRACH with 960 kHz SCS for non-initial access use cases, L = 139 is supported, and L = 571 and 1151 are not supported.
  + For 480 kHz SCS for both initial access and non-initial access use cases, L = 139 is supported, and L = 1151 is not supported. It can be further discussed whether or not L = 571 is supported.
* From [12] Futurewei:
  + For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2.
  + For non-initial access use cases, support 480 and 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.
* From [13] Nokia/NSB:
  + Support L=571 for PRACH with 480kHz.
* From [18] Qualcomm:
  + consider only using PRACH sequence length = 139 for SCS = 480 kHz and 960 kHz
* From [19] LG Electronics:
  + The 120 kHz PRACH SCS with sequence lengths L=571 and L=1151 are not required for the licensed spectrum where the regulatory requirements are not defined on PSD limit.
  + PRACH only with sequence length L=139 is supported for the 480 kHz SCS for initial/non-initial access and 960 kHz SCS for non-initial access.
* From [21] Mediatek:
  + Support only sequence length L=139 when PRACH SCS=480 kHz and 960 kHz.
* From [22] Intel:
  + Support PRACH formats A1~A3, B1~B4, C0, C2 for with SCS 480 kHz, i.e., .
* From [23] Apple:
  + If 480kHz and 960kHz SCS are used for PRACH transmission, support L=139 only.
* From [24] Sharp:
  + Only support L = 139 for PRACH with 480kHz and 960 kHz SSB SCS.

#### Summary of Discussions

The following are previous agreements on PRACH sequence and formats.

|  |
| --- |
| **Agreement:**   * For initial access and non-initial access use cases, support 120kHz PRACH SCS with sequence length L=571, 1151 (in addition to L=139) for PRACH Formats A1~A3, B1~B4, C0, and C2. * For non-initial access use cases,   + if 480kHz and/or 960 kHz SSB SCS is agreed to be supported, support 480 and/or 960 kHz PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively.     - FFS: support of sequence length L = 571, 1151 * FFS: Support of 480 and/or 960 kHz PRACH SCS for initial access use cases, if 480 and/or 960 kHz SSB SCS is agreed to be supported for initial access |

* Supported sequence lengths
  + Support PRACH lengths L=571, 1151 for 480kHz, and 960kHz PRACH
    - Samsung
  + Support PRACH length L=571 for 480kHz PRACH
    - Intel, Nokia/NSB
  + Do not support PRACH lengths L=571, 1151 for 960kHz PRACH
    - Ericsson, Qualcomm, Apple, Sharp
  + Do not support PRACH lengths L=1151 for 480kHz PRACH
    - Ericsson
  + Do not support PRACH lengths L=571, 1151 for 480kHz PRACH
    - Qualcomm, Apple, Sharp
* Consideration of additional formats/PRACH repetition lengths
  + CATT

#### **1st Round Discussion:**

Based on previous agreements and updated WID, moderator assume the following can be confirmed.

* Confirm agreement:
  + Support 480 PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively for initial and non-initial access cases
  + Support 960 PRACH SCS with sequence length L=139 for PRACH Formats A1~A3, B1~B4, C0, and C2, respectively for non-initial access cases

Also two companies has suggested to support L=571 for 480kHz, while a number of companies suggested not to support L=571 and L=1191 for 480 and 960kHz.

Moderator suggest to discuss on the following options:

* Option 1) Support PRACH length L=571, 1191 for 480 and 960 kHz PRACH
* Option 2) Support PRACH length L=571 for 480kHz PRACH, do not support PRACH length L=571, 1191 for 960kHz PRACH and L=1191 for 480kHz PRACH.
* Option 3) Do not support PRACH length L=571, 1191 for 480 and 960kHz PRACH

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | Support option 3, since SCS = 480/960 kHz with sequence length = 139 is enough to achieve the desired BW requirement for the maximum EIRP allowed |
| LG Electronics | Support Option 3 considering the regulatory requirements (e.g., PSD) and the bandwidth occupied by the PRACH. In detail, the 480 kHz PRACH sequence with length L=571 occupies bandwidth of 275 MHz which is larger than 100 MHz that can achieve the conducted power limit of 27 dBm according to US regulation. |
| Fujitsu | 1. Considering BW of PRACH, we slightly prefer Option 3).  2. To confirm the definition of initial access case in the previous agreements:  As discussed in previous meetings, the definition of initial access case for PRACH is ambiguous and confusing. To avoid misunderstanding, could we confirm that initial access case implies that the corresponding ROs are configured by SIB1? |

### 2.2.2 RACH Occasion Resources

* From [1] Huawei/HiSilicon:
  + For 480kHz and 960kHz PRACH, support the reference slot duration corresponding to 60 kHz SCS (Option 1 in RAN1 105-e Agreement).
  + Support a gap symbol between consecutive ROs for 480kHz and 960kHz PRACH configurations.
  + For 480kHz and 960kHz PRACH, at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH configuration in FR2 should be supported (Alt 2 in RAN1 105-e Agreement).
  + For 480kHz and 960kHz PRACH configuration, support 1, 2, and 4 PRACH slots per 60kHz reference slot with the following PRACH slot indexes:
    - For 1 PRACH slot per 60kHz reference slot: for 480kHz and for 960kHz PRACH
    - For 2 PRACH slots per 60kHz reference slot: for 480kHz and for 960kHz PRACH.
    - For 4 PRACH slots per 60kHz reference slot: supported values are FFS.
* From [2] vivo:
  + For RO configuration for PRACH with 480/960kHz SCS:
  + Reuse the exiting FR2 RACH configuration table and the location of duration containing PRACH slot pattern within 10ms is same as FR2.
  + How to determine the RACH slot index:
    - Alt.1: Reuse the same reference slot as FR2 and maintain the same number of PRACH slots per reference slot.
    - Alt.2: Reuse the same reference slot as FR2 and increase the number of PRACH slots to more than 2 per reference slot.
  + If gaps between consecutive ROs are needed for LBT and or beam switching, at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported.
* From [4] Interdigital:
  + In PRACH configuration, we support Option 1 as it is in compliance with NR Rel.16.
    - Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
  + In PRACH density configuration, support Alt 2 with the same RO density as 120kHz PRACH. Moreover, support further study for higher PRACH slot density for 480kHz and 960kHz PRACH, compared to the 120kHz PRACH.
    - ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
  + For 52.6 – 71 GHz with 120kHz, 480kHz, and 960kHz PRACH, inserting gaps to achieve non-consecutive RACH occasions is not supported.
  + For 52.6 – 71 GHz, support sharing and extending the COT for LBT-free PRACH transmission in the consecutive ROs.
* From [7] Samsung:
  + Using the RO pattern for SCS = 120 kHz derived from the PRACH configuration table as the reference for larger SCS cases.
  + Option 2 for RO pattern determination should be supported.
    - Option 2) Each 120kHz RO corresponds to 4 and 8 candidate RO positions for 480kHz and 960kHz PRACH, respectively. Information about the number and locations of 480/960kHz candidate RO(s) are configured or pre-selected within each 120kHz RO. The reference 120kHz RO is determined by the current PRACH configuration method in Rel-15/16 specification.
  + Support non-consecutive RO configuration to alleviate the RACH LBT failure.
* From [8] CATT:
  + The reference slot duration corresponds to 60 kHz SCS. PRACH slot index corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
  + For 480/960 kHz PRACH slots configuration, higher PRACH slot density or higher RO density in time domain can be supported to compensate the impact from MSGS –FDM decreasing and LBT/beam switching GAP.
* From [9] ZTE/Sanechips
  + For 480kHz and 960kHz, reuse the same RO configuration table as in Rel-15/16 with the same RO density for 120kHz PRACH.
  + Proposal 12: Support 60kHz for reference slot as in FR2 with the less spec effort in beyond 52.6GHz.
* From [10] Fujitsu:
  + For 480kHz and 960kHz PRACH, support gaps between consecutive ROs in time domain.
    - If Option 1) supports gaps between consecutive ROs, it is preferred because it is more aligned with the legacy PRACH configuration framework than Option 2).
    - If Option 1) does not support gaps between consecutive ROs, Option 2) is preferred because it supports the gaps by nature.
  + For PRACH density, if gaps between consecutive ROs are supported (by Option 1) or Option 2)), adopt Alt 2) for further discussion on higher density. Otherwise, it is fine to adopt Alt 1) or Alt 2), because there would be no difference between the baseline of the two alternatives.
* From [11] Ericsson:
  + For 480/960 kHz PRACH, support PRACH configurations that allow maintaining the same PRACH processing load (operations/unit time) as for 120 kHz PRACH configurations.
  + For 480/960 kHz PRACH, reuse the current PRACH configuration table in 38.211 for FR2 "as is." Specify rule for which 1 or 2 480/960 kHz slots within a 60 kHz reference slot are used depending on the value in the existing column "Number of PRACH slots within a 60 kHz slot" in the current PRACH configuration table. The rule should be common for all PRACH configurations in the table.
  + Support Option 1 and Alt 1. Regarding the FFS for Alt-1, do not support higher PRACH slot density (number of PRACH slots per reference slot).
  + It is not necessary to optimize PRACH design to allow for LBT gaps between consecutive PRACH occasions within a PRACH slot, especially since PRACH can be classified as short control signaling transmissions consistent with EN 302 567 (see [8]).
  + UE beam switching gaps between consecutive PRACH occasions within a PRACH slot are not needed, since the UE is allowed to send only one PRACH preamble before the end of the RAR window, and will hence not need to transmit in back-to-back PRACH occasions in a slot.
* From [12] Futurewei:
  + For the reference slot duration support Option 1.
  + For PRACH slot density use the same density (i.e. number of PRACH slots per reference slot) as for 120kHz PRACH in FR2-1 is supported (ALT 1).
* From [13] Nokia:
  + Adopt Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot. FFS: to have LBT gaps between ROs
  + Adopt ALT 2) i.e. the number of ROs per reference slot is the same as for 120kHz PRACH in FR2.
  + If LBT gaps are needed between ROs, it would be better to define fixed LBT gap time between valid ROs that do not depend on the time domain allocation of the PRACH. In that case the LBT gap length would not depend on the used PRACH format.
* From [18] Qualcomm:
  + a maximum of 4 and 2 FD multiplexed ROs for SCS = 120 kHz and sequence length = 571 and 1151, respectively
  + for SCS = 120 kHz, if the maximum number of FD ROs are reduced, consider ways to increase the TD ROs (to maintain the same capacity) with minimal specification impact
  + for higher RACH SCS (480 and 960 kHz), the gap and CP length may not be long enough to absorb the gNB beam switching delay requirement
  + for higher RACH SCS (480 and 960 kHz), consider including a symbol-level gap between ROs to allow for gNB beam switching delay
  + for 480kHz and 960kHz PRACH:
    - The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot
    - ROs for a given PRACH configuration can span more than one PRACH slot if gaps between consecutive ROs are supported for LBT and/or beam switching purposes
    - The same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
* From [19] LG Electronics:
  + If the reference slot SCS is kept as 60 kHz and the density of PRACH occasion is the same as in 120 kHz in the time-domain (e.g., 2 slots out of 8 slots for 480 kHz), the PRACH slot index for 480 and 960 kHz SCS can be determined based on the selected two values of with the pre-configured rule or based on the configured/indicated value(s) of by the gNB.
  + If the reference slot SCS is kept as 60 kHz and the density of PRACH occasion is increased compared to 120 kHz in the time-domain, the additional PRACH slots for 480 and 960 kHz SCS can be indicated/configured by the parameter X to allocate the consecutive X slots before the last slot given by (e.g., for 480 and 960 kHz SCS, respectively).
  + When LBT is used to transmit the PRACH preamble, consider to insert CCA gap between adjacent RACH occasions in time domain (e.g. X usec or Y symbol) to avoid inter-UE LBT blocking due to the propagation delay of PRACH transmitted in an earlier RO.
  + Considering the potential gap to account for LBT is needed to be inserted between the adjacent RACH occasions, at least the same RO density (i.e. number of RO per reference slot) as for 120 kHz PRACH in FR2-2 is supported for the PRACH density.
* From [20] ETRI:
  + Support Option 1 and ALT 2 for 480kHz and 960kHz PRACH slot configurations.
* From [22] Intel:
  + For 480kHz and 960kHz PRACH, select Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.
  + For PRACH SCS 480 kHz and 960 kHz, introduce optional time gaps between consecutive ROs;
  + Modify equation defining the first OFDM symbol of PRACH RO given Section 5.3.2 from TS 38.211 as follows:
    - ,
    - where is the gap duration (number of OFDM symbols) and for no gap.
  + On PRACH density for 480kHz and 960kHz PRACH, select ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported.
* From [23] Apple:
  + Maximum 4 PRACH ROs can be configured for 120kHz SCS with .
  + Maximum 2 PRACH ROs can be configured for 120kHz SCS with .
  + Reuse the existing FR2 PRACH configuration Table to indicate the time-domain PRACH slot location.
  + Support to keep the same PRACH capacity as Rel-16 FR2 for 480kHz and 960kHz SCS to minimize the signaling overhead.
  + The configured PRACH slots should be distributed over the 60kHz reference slot.
* From [24] Sharp:
  + Option 1 for RO design is preferred. Reuse Table 6.3.3.2-4 (Random access configurations for FR2 and unpaired spectrum) in Rel-16 38.211 as much as possible. 60kHz reference slot should be also inherited.
  + Regarding PRACH configuration design for 480/960kHz SCS, keep the same RO density and Alt 2 is preferred.
  + Gaps between consecutive ROs are needed at least for beam switching purposes, which should be considered during RO design.
  + A starting symbol index of a PRACH occasion is given by If non-zero duration gaps are configured between consecutive ROs and the ROs would span multiple PRACH slots, for 480 and 960 kHz SCS, respectively. Otherwise, for 480 and 960 kHz SCS, respectively.
* From [25] NTT Docomo:
  + For RO configuration for PRACH with 480/960 kHz SCS,
    - Support Option 1 to specify only 480/960 kHz PRACH slot within a 60 kHz referenced slot in addition to the existing RO configuration in FR2.
    - Only one or two 480/960 kHz PRACH slot(s) within the 60 kHz referenced slot is sufficient.
    - No need to enhance RA-RNTI calculation for NR operation in 52.6 – 71 GHz
    - No need to consider either LBT or beam switching gap for RO design in 52.6 – 71 GHz
* From [26] Xiaomi:
  + Inconsecutive RO time domain configuration should be supported at least for 480 kHz case.

#### Summary of Discussions

The following are previous agreements on PRACH sequence and formats.

|  |
| --- |
| **Agreement:**   * PRACH configuration for 480/960 kHz SCS (if agreed)   + The minimum PRACH configuration period is 10 ms (as in FR2)   + For RO configuration for PRACH with 480/960kHz SCS,     - FFS: details of how to configure the 480/960 kHz PRACH ROs using [60 or 120 kHz] reference slot considering at least:       * location of 480/960 kHz PRACH slot per reference slot       * location of duration containing 480/960khz PRACH slot pattern within 10ms       * potential impact to RA-RNTI calculation   **Agreement:**  For 480kHz and 960kHz PRACH,   * Down-select among option 1 and 2   + Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.  * + - FFS: supported values of the starting PRACH slot index within reference slot and whether or not the ROs for a given PRACH configuration can span more than one PRACH slot if gaps between consecutive ROs are supported for LBT and/or beam switching purposes  * + Option 2) Each 120kHz RO corresponds to 4 and 8 candidate RO positions for 480kHz and 960kHz PRACH, respectively. Information about the number and locations of 480/960kHz candidate RO(s) are configured or pre-selected within each 120kHz RO. The reference 120kHz RO is determined by the current PRACH configuration method in Rel-15/16 specification. * Following alternatives are considered on PRACH density   + ALT 1) At least the same density (i.e. number of PRACH slots per reference slot) as for 120kHz PRACH in FR2 is supported     - FFS: support for higher PRACH slot density (number of PRACH slots per reference slot)   + ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported     - FFS: support for higher RO density   + An “example” illustration of PRACH slots for 480/960kHz is shown below:      * FFS: whether and how to account for LBT in RO configuration (if needed) * FFS: whether and how to account for beam switching gap in RO configuration (if needed) |

The following is a summary of company views.

* RO definition for 480 and 960kHz
  + Option 1) The reference slot duration corresponds to 60 kHz SCS. A PRACH slot index, , corresponds to one of the starting 480/960 kHz PRACH slots within the reference slot.



* + - Huawei/HiSilicon, Interdigital, Ericsson, Futurewei, Nokia/NSB, [Qualcomm], ETRI, Intel, [Apple], Sharp, NTT Docomo, LGE, Fujitsu (1st preference, with configurable gaps between ROs)
  + Option 2) Each 120kHz RO corresponds to 4 and 8 candidate RO positions for 480kHz and 960kHz PRACH, respectively. Information about the number and locations of 480/960kHz candidate RO(s) are configured or pre-selected within each 120kHz RO. The reference 120kHz RO is determined by the current PRACH configuration method in Rel-15/16 specification.
    - Samsung, Fujitsu (2nd preference)
* PRACH density
  + ALT 1) At least the same density (i.e. number of PRACH slots per reference slot) as for 120kHz PRACH in FR2 is supported
    - Ericsson, Futurewei
  + ALT 2) at least the same RO density (i.e. number of RO per reference slot) as for 120kHz PRACH in FR2 is supported
    - Interdigital, Nokia/NSB, ETRI, Intel, Sharp, LGE, Fujitsu
* Gap between consecutive ROs
  + Support: Huawei/HiSilicon, Samsung, Qualcomm, LGE, Intel (Configurable gap between consecutive RO), [Sharp], Fujitsu
  + Do not support: Interdigital, Ericsson, NTT Docomo
* Slot index for 480/960 kHz PRACH
  + for 480kHz and for 960kHz PRACH
    - Huawei/HiSilicon (For 1 PRACH slot per 60kHz reference slot), Sharp (gap not configured)
  + for 480kHz and for 960kHz PRACH.
    - Huawei/HiSilicon (For 2 PRACH slots per 60kHz reference slot)
  + for 480 and 960 kHz SCS, respectively
    - Sharp (gap configured)
  + The selected two values of with the pre-configured rule or based on the configured/indicated value(s) of by the gNB
    - LGE
* Maximum FDM of ROs
  + 4 FDM and 2 FDM ROs for 120kHz PRACH with L=571 and 1151, respectively
    - Qualcomm, Apple

#### **1st Round Discussion:**

Suggest to continue discussion on the above issues. Moderator asks companies to provide further comments. Moderator will provide a suggested proposal once the summary captures all company opinion correctly.

If the above summary is directly edited (please use a color to highlight changes, e.g. RED) and mention the changes/additions in the comment below.

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | RO definition for 480 and 960kHz: Support 60 kHz reference slot in order to minimize the spec changes  PRACH density: Alt 2 |
| LG Electronics | We added our preference for Option 1 and Alt 2 in the above summary.  We prefer to keep the reference slot subcarrier spacing as 60 kHz and if the density of PRACH occasion is the same as in 120 kHz in the time-domain (e.g., 2 slots out of 8 slots for 480 kHz), the PRACH slot index for 480 and 960 kHz SCS can be determined based on the selected two values of with the pre-configured rule or based on the configured/indicated value(s) of by the gNB. For PRACH density, at least the same RO density (i.e. number of RO per reference slot) as for 120 kHz PRACH in FR2-2 is supported considering the potential gap to account for LBT is needed to be inserted between the adjacent RACH occasions. |
| Fujitsu | We added our preferences in the above summary. |

### 2.2.3 RAR Window & RA Preamble ID

* From [1] Huawei/HiSilicon:
  + Introduce additional bits in the DCI scheduling RAR to resolve the issue of RA-RNTI/MsgB-RNTI calculation for 480 kHz and 960 kHz RACH procedure.
  + Support maximum of 40 ms for ra-ResponseWindow for operation with shared spectrum and msgB-ResponseWindow for both operations with and without shared spectrum. Support indicating two LSBs of SFN at which gNB has received msg1 (MsgA) in DCI format 1\_0 with CRC scrambled by RA-RNTI (MsgB-RNTI).
* From [2] vivo:
  + For larger PRACH SCS (480KHz/960KHz), the following options can be considered for RA-RNTI calculation:
    - Alt.1: Modify the RA-RNTI formula as following and introduce some contention resolution mechanism to resolve the conflict.
      * RA-RNTI = (1+s\_id+14×t\_id+14×X×f\_id +14×X×8×ul\_carrier\_id) mod A
    - Alt.2: Reuse the current RA-RNTI formula while introducing additional indicator field to indicate the time-frequency resource together with RA-RNTI.
    - Alt.3: Depending on the RO configuration pattern, reuse/modify the RA-RNTI formula and express the slot indexes t\_id based on a new specific subcarrier spacing.
* From [8] CATT:
  + For supporting Msg1 transmission with 480 KHz/960 KHz SCS, RA-RNTI is divided into two parts. One part of RA-RNTI is carried by DCI, and the remaining 16-bit of RA-RNTI could be used to scramble CRC of the DCI1. Two possible options are:
    - Option A:
      * RA-RNTI = (1 + s\_id + 14 × t\_id + 14 ×× f\_id + 14 × × 8 × ul\_carrier\_id) mod
      * inDCI\_bit = floor ((1 + s\_id + 14 × t\_id + 14 ×× f\_id + 14 × × 8 × ul\_carrier\_id) /)
      * s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
    - Option B:
      * RA-RNTI = 1 + s\_id + 14 ×(t\_id mod 80) + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id
      * inDCI\_bit =
      * s\_id is the index of the first OFDM symbol of the PRACH occasion (0 ≤ s\_id < 14)
      * t\_id is the index of the first slot of the PRACH occasion in a system frame (0 ≤ t\_id < 640)
* From [9] ZTE/Sanechips:
  + For higher PRACH SCS (480 and/or 960 kHz), consider the following options for further down-selection of RA-RNTI enhancements:
    - Option 2)
      * Segment the PRACH into N segments
      * Non-overlapping PRACH slot location in each segment(80 slots)
    - Option 3)
      * Segment the PRACH into N segments
      * is the index of the PRACH slot that contains the PRACH occasion in a segment.
      * In DCI: RA-indication = Segment index
    - Option 7)
      * is the index of the first 120kHz slot that contains the PRACH occasion in a system frame.
      * is the index of the first OFDM symbol of the PRACH occasion based on the value of specified in clause 5.3.2 of TS 38.211.
* From [10] Fujitsu:
  + For 480kHz and 960kHz PRACH, the following should be considered to uniquely identify a RO:
    - When calculating RA-RNTI, t\_id is determined in a way that more than one slot can have the same t\_id; and
    - DCI scheduling RAR indicates the local index among the slots having the same t\_id.
* From [11] Ericsson:
  + For 480/960 kHz PRACH, reuse the RA-RNTI expressions from Rel-15/16, with the additional statement that for 480/960 kHz PRACH, t\_id should be determined based on a subcarrier spacing of 120 kHz.
  + Postpone further discussions of RA-RNTI design until the PRACH configuration design is settled.
* From [13] Nokia:
  + Reuse RA-RNTI formula defined for 120 kHz SCS also for the cases PRACH is configured with 480 or 960 kHz SCS where
    - assumes 480/960 kHz SCS
    - assumes 120 kHz SCS
* From [19] LG Electronics:
  + If the reference slot SCS remains as 60 kHz and the density of PRACH occasion is the same as in 120 kHz in the time-domain (e.g., 2 slots out of 8 slots for 480 kHz), the existing RA-RNTI/MSGB-RNTI equation can be reused for 480 and 960 kHz SCS by reinterpreting the slot indexes t\_id based on a new specific subcarrier spacing as the slot indexes of 120 kHz SCS (e.g., floor(t\_id/n) where n=4 for 480 kHz SCS and n=8 for 960 kHz).
  + If the reference slot SCS remains as 60 kHz and the density of PRACH occasion is increased compared to 120 kHz in the time-domain, to calculate RA-RNTI/MSGB-RNTI associated with the PRACH occasion for 480 and 960 kHz SCS using the existing RA-RNTI equation, the following options can be considered:
    - Option 1: Divide the RAR window for RA-RNTI (or msg2 window for MSGB-RNTI) into N sub-periods (where each sub-period is 80 slots using the used SCS) + signal the sub-period index using the DCI that schedules the MSG2/MSGB.
    - Option 2: Divide the frequency index or the symbol index into M subset (if M=4, the subset index 0/1/2/3 can be configured to the frequency index {0, 1}, {2, 3}, {4, 5}, {6, 7}, respectively) + signal the subset index using the DCI that schedules the MSG2/MSGB
* From [20] ETRI:
  + Propose to reuse the current equation with minor modifications for RA preamble ID calculation.
    - RA-RNTI = 1 + s\_id + 14 × t\_id + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id
      * t\_id is the index of 120kHz slot that contains RO in a system frame
      * s\_id is the index of the first OFDM symbol of RO based on the value of specified in clause 5.3.2 of TS 38.211
* From [22] Intel:
  + RA-RNTI computation equation should be adjusted to avoid overflow in case of PRACH SCS 480 kHz and 960 kHz;
  + Support the following modified equation for RA-RNTI computation:
    - ,
    - where t\_id is based on the value of specified in clause 5.3.2 of TS 38.211.
* From [23] Apple:
  + modifying the existing calculation equation or redefine t\_id based on 120kHz SCS to solve the RA-RNTI overflowing problem:
* From [24] Sharp:
  + Assuming RO density per reference slot is unchanged, without modifying the formula and definition of s\_id. Modify the definition of t\_id as the slot index referring to 120kHz SCS.

#### Summary of Discussions

The following list of options are from last meetings discussion.

|  |
| --- |
| * + **Plain Modulus Category**     - Option 1)   + **PRACH Sub-segmentation Method Category**     - Option 2)       * The same PRACH slot location in each 120kHz slot duration     - Option 3)       * Segment the PRACH into N segments       * is the index of the PRACH slot that contains the PRACH occasion in a segment.       * In DCI: RA-indication = Segment index     - Option 4)       * Segment the PRACH into N segments       * In DCI:     - Option 5)       * Segment the PRACH into N segments       * In DCI:     - Option 6)       * In DCI:   + **Compressing some indices Category (may require a matching RO configuration to work properly)**     - Option 7)       * is the index of the first 120kHz slot that contains the PRACH occasion in a system frame.       * is the index of the first OFDM symbol of the PRACH occasion based on the value of specified in clause 5.3.2 of TS 38.211.     - Option 8)       * RA-RNTI = 1 + s\_id + 14 × floor(t\_id / ) + 14 × 80 × f\_id + 14 × 80 × 8 × ul\_carrier\_id,       * t\_id is based on the value of specified in clause 5.3.2 of TS 38.211. |

The following is summary of company views.

* Alt 1) Plain Modulus Category, some example in option 1
  + Vivo, Apple
* Alt 2) PRACH Sub-segmentation Method Category, some examples in option 2 ~ 6
  + Huawei/HiSilicon, vivo, CATT, ZTE/Sanechips, Fujitsu, LGE
* Alt 3) Compressing some indices Category (may require a matching RO configuration to work properly) , some examples in option 7 ~ 8
  + vivo, ZTE/Sanechips, Ericsson, Nokia/NSB, ETRI, Intel, Sharp

#### **1st Round Discussion:**

Moderator suggest to further discuss the three categories and the detailed options.

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | Although requires some extra signaling, but we prefer Alt2.  For Alt 1, the RA-RNTI can be more than FFFF and modular operation needs to be applied. Due to the modular operation, some ROs:   * May have the same RA-RNTI * May collide with FFF0–FFFD (reserved) or P-RNTI (FFFE) or SI-RNTI (FFFF)   Hence, some restrictions need to be applied:   * ROs with RA-RNTI conflicting with the pre-allocated RNTIs should not be used. * When multiple ROs have the same RA-RNTI but not conflicting with the pre-allocated RNTIs, only one of the ROs can be used (e.g., the first RO among those ROs with the same RA-RNTI) or rely on the existing contention resolution mechanisms   For Alt3, some restrictions may be needed to the RO design for it to work |
| Fujitsu | 1. For down selection of options for RA-RNTI calculation, the impact on MSBG-RNTI should be considered. For example, if RA-RNTI is calculated by Alt 1), additional method may be needed for handling collision between RA-RNTI and MSBG-RNTI. From this perspective, Alt 1) is not preferred. Then between Alt 2) and Alt 3), considering flexibility, Alt 2) is preferred.  2. It seems that option 2) should belong to Alt 3) rather than Alt 2). |

### 2.2.4 Other aspects on PRACH

* From [12] Futuerwei:
  + If the UE RACH transmission can be LBT exempt under the short control signaling exclusion, support signaling to indicate UE that LBT is disabled or enabled for the RACH procedure.
* From [13] Nokia/NSB:
  + Discuss whether 960 kHz SCS PRACH procedure is supported from IDLE/Inactive state.

#### Summary of Discussions

The following are issues that were mentioned by companies.

* Short control signal exemption applicability for PRACH
* Whether 960kHz PRACH is supported for IDLE/inactive state.

#### **1st Round Discussion:**

Moderator assumes applicability of short control signal exemption will be discussed under channel access agenda. Moderator suggest companies to provide comments on the following issue.

* Whether 960kHz PRACH is supported for IDLE/inactive state

If there are other issues that require further discussion, please comment here as well.

|  |  |
| --- | --- |
| Company | Comments |
| Qualcomm | Initial access SSB (and hence PRACH) is limited to 480 kHz. We think this is outside the RAN1 and RAN agreements so far. |
|  |  |

## 2.3 Others Aspects

* From [3] Spreadtrum:
  + The SSB-based TRS/CSI-RS validation can be supported.
* From [11] Ericsson:
  + The current RSSI and CO measurement in Rel-16 should be enhanced to support NR unlicensed operation in the spectrum beyond 52.6 GHz in Rel-17. The enhancement at least includes extension of reference SCS and indication of channel bandwidth. The enhancement details of the RRC configuration for RSSI and CO measurement should be decided by RAN2.
* From [12] Futurewei:
  + In 60 GHz shared spectrum band, where the LBT is enabled, allow a COT a gap between consecutive transmissions of at least one slot 480 kHz SCS duration (32us) without LBT.
  + Consider using CSI-RS presence in the discovery burst for possible ways to implement beam refinement during the initial channel access.
* From [13] Nokia:
  + It is proposed that RAN1 discusses whether IDLE mode procedures (camping, reselection) are supported for 960kHz sub-carrier spacing.

#### Summary of Discussions

The following are issues that were mentioned by companies.

* The SSB-based TRS/CSI-RS validation can be supported.
* The current RSSI and CO measurement in Rel-16 should be enhanced to support NR unlicensed operation in the spectrum beyond 52.6 GHz in Rel-17. The enhancement at least includes extension of reference SCS and indication of channel bandwidth. The enhancement details of the RRC configuration for RSSI and CO measurement should be decided by RAN2.
* In 60 GHz shared spectrum band, where the LBT is enabled, allow a COT a gap between consecutive transmissions of at least one slot 480 kHz SCS duration (32us) without LBT.
* Consider using CSI-RS presence in the discovery burst for possible ways to implement beam refinement during the initial channel access.
* It is proposed that RAN1 discusses whether IDLE mode procedures (camping, reselection) are supported for 960kHz sub-carrier spacing.

#### **1st Round Discussion:**

Moderator suggest to continue discussion on the above issues.

If there are other issues that require further discussion, please comment here as well.

|  |  |
| --- | --- |
| Company | Comments |
|  |  |
|  |  |

# Summary of Proposed Agreements/Conclusions

[To be filled]

# Summary of Agreements/Conclusions from RAN1 #106-e

[To be filled]

# Reference

1. R1-2106442, “Initial access signals and channels for 52-71GHz spectrum,” Huawei, HiSilicon
2. R1-2106579, “Discussions on initial access aspects for NR operation from 52.6GHz to 71GHz,” vivo
3. R1-2106692, “Discussion on initial access aspects for NR for 60GHz,” Spreadtrum Communications
4. R1-2106766, “Discussions on initial access signals and channels for operation in 52.6-71GHz,” InterDigital, Inc.
5. R1-2106795, “Considerations on initial access aspects for NR from 52.6 GHz to 71 GHz,” Sony
6. R1-2106831, “Initial access aspects for NR from 52.6 GHz to 71GHz,” Lenovo, Motorola Mobility
7. R1-2106873, “Initial access aspects for NR from 52.6 GHz to 71 GHz,” Samsung
8. R1-2106956, “Initial access aspects for up to 71GHz operation,” CATT
9. R1-2107000, “Discussion on the initial access aspects for 52.6 to 71GHz,” ZTE, Sanechips
10. R1-2107032, “Considerations on initial access for NR from 52.6GHz to 71 GHz,” Fujitsu
11. R1-2107050, “Initial Access Aspects,” Ericsson
12. R1-2107097, “Initial access for Beyond 52.6GHz,” FUTUREWEI
13. R1-2107104, “Initial access aspects,” Nokia, Nokia Shanghai Bell
14. R1-2107112, “Further discussion of initial access for NR above 52.6 GHz,” Charter Communications
15. R1-2107149, “Discussion on initial access aspects supporting NR from 52.6 to 71 GHz,” NEC
16. R1-2107176, “Initial access aspects for NR from 52.6GHz to 71 GHz,” Panasonic Corporation
17. R1-2107237, “Discusson on initial access aspects,” OPPO
18. R1-2107330, “Initial access aspects for NR in 52.6 to 71GHz band,” Qualcomm Incorporated
19. R1-2107435, “Initial access aspects to support NR above 52.6 GHz,” LG Electronics
20. R1-2107471, “Discussion on initial access aspects for NR from 52.6 to 71GHz,” ETRI
21. R1-2107517, “Discussion on initial access of 52.6-71 GHz NR operation,” MediaTek Inc.
22. R1-2107577, “Discussion on initial access aspects for extending NR up to 71 GHz,” Intel Corporation
23. R1-2107726, “Initial access signals and channels,” Apple
24. R1-2107789, “Initial access aspects,” Sharp
25. R1-2107845, “Initial access aspects for NR from 52.6 to 71 GHz,” NTT DOCOMO, INC.
26. R1-2107912, “On initial access aspects for NR from 52.6GHz to 71 GHz,” Xiaomi
27. R1-2108008, “NR SSB design consideration from 52.6 GHz to 71 GHz,” Convida Wireless
28. R1-2108148, “Discussion on initial access aspects for NR beyond 52.6GHz,” WILUS Inc.