**3GPP TSG-RAN WG1 Meeting #106-eR1-210xxxx**

**e-Meeting, August 16th – August 27th, 2021**

**Agenda item:** **7.2.5**

**Source: Moderator (Apple Inc.)**

**Title: Summary of email discussion [106-e-NR-L1enh-URLLC-03] on sub-slot-based HARQ-ACK timing in Rel-16**

**Document for: Discussion and Decision**

# 1 Introduction

This contribution provides the summary for the following email discussion in RAN1#106-e:

* [106-e-NR-L1enh-URLLC-03] Issue#7: HARQ-ACK timing for sub-slot based HARQ-ACK feedback by August 20 – Sigen (Apple)

Section 2 provides the background information. Section 3 captures the detailed email discussions. Section 4 summarizes the outcome of the email discussion.

# 2 Background

For HARQ-ACK, the PUCCH for HARQ-ACK is transmitted in UL slot *n+k*, where *k* is indicated in UL DCI, and *n* is determined based on PDSCH. When UL SCS is larger than DL SCS, two different interpretations existed in the history of RAN1 discussions. This was discussed in RAN1#104b-e [1] and RAN1#105-e [2], and it was concluded that the two different interpretations can exist in Rel-15, but for Rel-16, a working assumption was made to adopt interpretation 2 below. The main reasons for adopting interpretation 2 are that it is aligned with earlier RAN1 agreement and it is also aligned with the Type-1 HARQ-ACK codebook construction in TS 38.213.

***Conclusion:*** *(RAN1#104b-e)*

*For HARQ-ACK timing in Rel-15, in case UL SCS is larger than DL SCS, there are two different interpretations:*

*-       Interpretation 1: k = 0 corresponds to the last UL slot that overlaps with the PDSCH*

*-       Interpretation 2: k = 0 corresponds to the last UL slot that overlaps with the DL slot for the PDSCH*

*Further discuss this issue for Rel-16 in future meetings.*

***Working Assumption*** *(RAN1#105-e)*

*For HARQ-ACK timing in Rel-16 with slot-based HARQ-ACK feedback, in case UL SCS is larger than DL SCS, k = 0 corresponds to the last UL slot that overlaps with the DL slot for the PDSCH.*

* *Further discuss the HARQ-ACK timing for sub-slot-based HARQ-ACK feedback*
* *FFS specification impact*

What remains open is the HARQ-ACK timing for sub-slot-based HARQ-ACK feedback. As discussed in [2], similar to slot-based HARQ-ACK feedback, two options are available:

*For HARQ-ACK timing in Rel-16 with sub-slot-based HARQ-ACK feedback,*

* *Option 1: k = 0 corresponds to the last UL sub-slot that overlaps with the PDSCH.*
* *Option 2: k = 0 corresponds to the last UL sub-slot that overlaps with the DL slot for the PDSCH.*

Option 1 is aligned with the following RAN1#97 agreement, while Option 2 is aligned with the working assumption that was made for slot-based HARQ-ACK timing in RAN1#105-e.

*Agreements: (RAN1#97)*

*For sub-slot-based HARQ-ACK feedback procedure, K1 is the number of sub-slots from the sub-slot containing the end of PDSCH to the sub-slot containing the start of PUCCH.*

* *Use UL numerology to define the sub-slot grid for PDSCH-to-sub-slot association.*
* *FFS: The configurable value range of K1 needs to be extended, and impact to related DCI field bitwidth.*
* *Note: It has been agreed that K1 is defined following R15 approach but in unit of sub-slot.*

This issue was discussed in [3]-[6] submitted to RAN1#106-e. A draft CR is also provided in [3].

Option 2 is preferred in [3][6], while Option 1 is preferred in [4][5]. The arguments for each option are summarized as follows:

* Option 1
	+ Reduced latency in some cases (e.g. when PDSCH is at the beginning of the DL slot and the earliest symbols for HARQ-ACK feedback are UL symbols) compared to Option 2, as shown in Figure 1.
* Option 2
	+ Consistent behavior between slot-based and sub-slot-based HARQ-ACK feedback timing
	+ Principle of Type 1 HARQ-ACK codebook construction can be reused for sub-slot-based HARQ-ACK feedback.
	+ Less gNB/UE complexity and less specification impact



Figure 1 *k = 0* for Option 1 and Option 2

# 3 Email Discussions

## 3.1 First Round of Email Discussion

For HARQ ACK timing in Rel-16 with sub-slot-based HARQ-ACK feedback,

* Option 1: k = 0 corresponds to the last UL sub-slot that overlaps with the PDSCH.
* Option 2: k = 0 corresponds to the last UL sub-slot that overlaps with the DL slot for the PDSCH.

**Companies please indicate which option you support.**

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| --- | --- |
| **Option 1** | Nokia/NSB, Qualcomm, OPPO, vivo, CATT, HW/HiSi (slight preference), DOCOMO, Sharp, Intel, ZTE |
| **Option 2** | Intel (can accept), Apple, Ericsson, MTK |

**Companies please provide detailed reasons why you support Option 1 or 2.**

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| --- | --- |
| **Company** | **Comments** |
| Nokia, NSB | Option 1 to have the reduced latency. We should not forget that the main motivation in Rel-16 to introduce sub-slot PUCCH actually was to reduce the HARQ-ACK latency which would be now lost. Actually, we don’t think that option one creates more specification changes as actually the current specs describe Option 1 (so changes will be needed for the slot-based decision, not the other way around)!On the Type 1 CB, we anyhow need changes there so also here we don’t think there is a need for much different handling – moreover, this is not existing specifications yet (see AI 8.3.1.1 where we introduce this now in Rel-17)  |
| Qualcomm | We support Option 1. As pointed out by Nokia, Option 1 is what we agreed in RAN1 Rel-16 URLLC, and is what’s been implemented in the spec (TS 38.213, v16.6.0). On the type-1 CB, Rel-16 doesn’t support sub-slot based Type-1 HARQ-ACK CB. So we are not sure why this should be taken into account for a Rel-16 CR discussion (at this late stage).  |
| OPPO | We support option 1. As commented by Nokia and QC, option 1 can reduce the HARQ feedback latency, which is the intention to introduce sub-slot based HARQ-ACK feedback in Rel-16. And we share similar view with QC that Rel-16 does not support sub-slot based Type-1 HARQ-ACK CB so some changes (if needed) can leave to Rel-17 HARQ-ACK AI. |
| vivo | Agree with Nokia, Qualcomm and OPPO. Option 2 is against the intention of sub-slot to reduce the HAQ-ACK feedback latency. Sub-slot based type-1 CB is not supported in Rel-16. |
| CATT | Same view as above. |
| HW/HiSi | We have a slight preference for Option 1, since it does not extent the feedback delay, which could be the case with Option 2, if the PDSCH is scheduled in the front-part of the slot. Additionally, Option 1 is aligned with the previous agreement. |
| DOCOMO | Option 1 should be supported based on the RAN1#97 agreement. We need to revert the agreement to support Option 2. |
| Samsung | At least, our preference is to have unified design regardless of whether slot-based or sub-slot-based HARQ-ACK feedback is configured. So, before deciding which option is supported for sub-slot based HARQ-ACK feedback, we would like to hear other companies’ view on this aspect firstly.  |
| Sharp | Option 2 increases latency for sub-slot based HARQ-ACK reporting. Option 1 reduces the latency. |
| Intel | We see the motivation behind Option 2 and do not see the latency impact as significant. However, given that we have an explicit agreement from RAN1 #97 that points towards Option 1, it would be appropriate to go with Option 1. |
| Apple | We prefer Option 2 because we think the latency impact is minimal in practical network. In most cases, we would not see any difference in the latency. Only in the rare cases when the conditions are perfectly lined up, we see some impact on latency. Option 2 on the other hand allows a unified design between slot-based and sub-slot-based HARQ-ACK feedback. |
| Ericsson | Option 2. The reason for the CR is not only for Type-1 HARQ-ACK CB. It is also needed for Type-2 CB in order to have a proper timing for CB construction. Hence, the arguments related to Type-1 HARQ-ACK CB for Rel-16 are not justified since Rel-16 does not support Type-1 CB for sub-slot.The argument from latency is not clear to us. Why should Option 2 results in higher latency than Option 1? If DL is on 15 kHz, and UL on 15 kHz configured with sub-slot of 7 symbols, we run in the same issue. The codebook construction would be rely on the duration and position of any scheduled PDSCH in a slot.Hopefully the NW vendors consider this complexity.Lastly, it is not preferred to have different approaches. Unified solution is always preferred. |
| ZTE | Slightly prefer Option 1.  |
| MTK | We tend to agree with Ericsson and prefer Option 2. To us, it is better to apply a unified solution and pursue less gNB/UE complexity and less specification impact, although we understand Option 1 fits better with previous RAN1 agreement in RAN1 #97. |
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The TP for both slot-based and sub-slot-based HARQ-ACK feedback will be discussed together after this issue is concluded.

## 3.2 Second Round of Email Discussion

From the first round of email discussion, here are companies’ preferences:

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| **Option 1** | Nokia/NSB, Qualcomm, OPPO, vivo, CATT, HW/HiSi (slight preference), DOCOMO, Sharp, Intel, ZTE |
| **Option 2** | Intel (can accept), Apple, Ericsson, MTK |

Samsung prefers a unified solution between slot-based and sub-slot-based HARQ-ACK timing.

Given that majority companies prefer Option 1, here is the proposal for discussion:

### Proposal 1:

**For HARQ ACK timing in Rel-16 with sub-slot-based HARQ-ACK feedback, adopt Option 1.**

* **Option 1: k = 0 corresponds to the last UL sub-slot that overlaps with the PDSCH.**

**Companies please comment with detailed reasons if this proposal is not acceptable to you.**

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| **Company** | **Comments** |
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# 4 Outcome of the Email Discussion

# References

1. R1-2104105, Summary of email discussion [104b-e-NR-7.1CRs-04] on the correction for HARQ-ACK timing, Moderator (Apple Inc.), RAN1#104b-e, April 2021.
2. R1-2106301, Summary of email discussion [105-e-NR-7.1CRs-13] on the correction for HARQ-ACK timing in Rel-16, Moderator (Apple Inc.), RAN1#105-e, May 2021.
3. R1-2107063, Draft CR on Timing for slot-based and sub-slot-based HARQ-ACK Feedback, Ericsson, RAN1#106-e, Aug. 2021.
4. R1-2107266, Remaining issues on HARQ-ACK timing for sub-slot based HARQ-ACK feedback, OPPO, RAN1#106-e, Aug. 2021.
5. R1-2107681, Correction for HARQ-ACK timing in Rel-16, Huawei, HiSilicon, RAN1#106-e, Aug. 2021.
6. R1-2107713, Discussions on HARQ-ACK timing for sub-slot-based HARQ-ACK feedback in Rel-16, Apple, RAN1#106-e, Aug. 2021.