**Proposal 3-1b: For DMRS-less PUCCH, capture Table 1, Table 2, and Table 3 in the TR.**

Table 1: Performance (SNR) gain observed for DMRS-less PUCCH over Rel-15/16 baseline

|  |  |  |  |
| --- | --- | --- | --- |
| Simulated scenario | Performance metric | Observed SNR gains | Source |
| **Scenario 1: 2 bits UCI**  **Baseline: PF1**  **Enhancement: DMRS-less PUCCH** | 1% FA, 1% ACK miss detection, 0.1% NACK->ACK error | 3dB | QC |
| 3dB | OPPO |
| 3~4dB | Huawei |
| **Scenario 2: 3/4/6 bits UCI**  **Baseline: PF3**  **Enhancement: DMRS-less PUCCH**  Note: Intel simulated 3-7 bits UCI | 1% BLER | 3dB | QC |
| 3dB | Sharp |
| 1.5 ~ 2.1dB | Eurecom |
| 1% FA, 1% BLER | 0dB | Intel |
| 0.3~0.5dB | VIVO |
| 1% FA, 1% ACK miss detection, and 0.1% NACK to ACK | 1~2dB | VIVO |
| 2.8dB | QC |
| [0dB] (Note 1) | Ericsson |
| **Scenario 3: 11 bits UCI**  **Baseline: PF3**  **Enhancement: DMRS-less PUCCH**  Note: Intel simulated 8-11 bits UCI | 1% BLER | 3~4dB | QC |
| 3~4dB | HW |
| 2~3dB | ZTE |
| 1.5~2.1dB | Eurecom |
| 0 ~ 0.2dB | Ericsson |
| 1 ~ 2.7dB | CMCC |
| 1% FA, 1% BER | 0.3dB | Intel |
| 2.1dB | QC |
| 1% FA, 1% ACK miss detection, and 0.1% NACK to ACK error | 4dB | VIVO |
| 3.8dB | ZTE |
| 4dB | QC |
| [0dB] (Note 1) | Ericsson |
| 1% FA, 1% BLER, and 5% undetectable error rate | 4dB | QC |
| **Scenario 3: 22/24 bits UCI**  **Baseline: PF3**  **Enhancement: DMRS-less PUCCH** | 1% BLER | [-2dB] (Note 1) | Eurecom |
| 1dB | QC |

Note 1: this is a late submission/report of result. The result is captured in the TR. But it should not be used to draw any observation/conclusion, according to RAN1 agreed working procedure.

Table 2: Performance (PAPR/CM) gain observed for DMRS-less PUCCH over Rel-15/16 baseline

|  |  |  |
| --- | --- | --- |
| Modulation order | Observed PAPR/CM gain | Source |
| QPSK | 3.5dB PARR gain  1dB CM gain | QC |
| 6.3dB PAPR gain | Eurecom |
| 4.5dB PAPR gain | Huawei |
| Pi/2 BPSK | 0.5dB PAPR gain  0.6dB CM gain | QC |
| 4.8 dB PAPR gain | Eurecom |

Table 3: Key simulation assumptions for DMRS-less PUCCH study over Rel-15/16 baseline

|  |  |
| --- | --- |
| Company | Key simulation assumptions |
| ZTE | Receiver for Rel-15/16 PUCCH: ML coherent receiver  Receiver for sequence based PUCCH: ML noncoherent sequence detector |
| Intel | Receiver for Rel-15/16 PUCCH: ML coherent receiver (MMSE channel estimator and equalizer) and non-coherent receiver  Receiver for sequence based PUCCH: ML noncoherent sequence detector/correlator |
| Qualcomm | Receiver for Rel-15/16 PUCCH: ML coherent receiver  Receiver for sequence based PUCCH: ML noncoherent receiver (correlator with 2D-FFT or fast Hadamard transform) |
| Sharp | Receiver for Rel-15/16 PUCCH: MMSE channel estimation (with genie Doppler and delay spread) + ML coherent detection  Receiver for sequence based PUCCH: ML noncoherent sequence detector/correlator |
| CMCC | Receiver for Rel-15/16 PUCCH: ML coherent receiver  Receiver for sequence based PUCCH: ML noncoherent sequence detector/correlator |
| vivo | Receiver for Rel-15/16 PUCCH: ML coherent receiver Receiver for sequence based PUCCH: ML noncoherent sequence detector/correlator  Ideal noise power estimation is used for both receiver for both legacy PUCCH and new sequence based PUCCH, and the noise power is used only in DTX detection. |
| Ericsson | Receiver for Rel-15/16 PUCCH: conventional and ML noncoherent  receiver  Receiver for sequence based PUCCH: ML noncoherent receiver |
| EURECOM | Receiver for Rel-15/16 PUCCH: advanced receivers for <=11 bits(non-coherent ML), conventional receiver for 22 bits (LS channel estimation + MMSE/MRC)  Receiver for sequence based PUCCH: ML noncoherent sequence detector/correlator for 4/11 bit case; non-coherent LLR unit adapted to 3GPP polar code for 22-bit case. Also simulated low-complexity receiver for 11-bit UCI case. |
| Huawei, HiSi | Receiver for Rel-15/16 PUCCH: 2D-Wiener filter based channel estimation + MMSE equalization  Receiver for sequence based PUCCH: CHIRRUP algorithm based sequence detection |
| OPPO | Receiver for Rel-15/16 PUCCH: LMMSE-IRC receiver.  Receiver for sequence based PUCCH: ML correlation. |

**Proposal 3-3a-1: For DMRS-less PUCCH, capture the following in the TR**

* Receiver needs to implement a non-coherent sequence detector/correlator for reception of the new PUCCH format.
* For reception of the new PUCCH format, channel and noise covariance matrix estimation is not required.
* Computation efficient implementations of the receiver for the new PUCCH format have been studied. Their complexity can be lower or higher than the decoder for existing NR PUCCH coherent receiver depending on the adopted sequence, on the UCI payload size and on the implementation of the considered coherent receiver.

**Proposal 3-3b: For DMRS-less PUCCH, capture the following in the TR**

* Receiver implementation for the new PUCCH format is an extension of the PUCCH format 0 receiver with similarity that both are noncoherent sequence detectors, while the new receiver needs to perform correlation over a larger sequence pool. The size of the sequence pool over which the receiver for the new PUCCH format needs to perform correlation increases exponentially with the number of UCI bits.

**Proposal 3-4: For DMRS-less PUCCH, capture the following in the TR**

* UE needs to implement a UCI to sequence mapping and sequence to RE mapping for the new PUCCH format
* Four potential approaches to implement the sequences for DMRS-less PUCCH were studied.
  + Approach 1: Reuse Rel-15/16 CGS/ZC/Gold/m-sequences generation with the same sequence length being supported in Rel-15/16
  + Approach 2: Reuse Rel-15/16 CGS/ZC/Gold/m-sequences generation with a different sequence length being supported in Rel-15/16
  + Approach 3: Modification of NR Rel-15/16 UCI encoding scheme to generate the sequences
  + Approach 4: implement a new sequence generation which is not covered by above, if the new sequence is adopted in spec.

**Proposal 4-1a-2: For PUSCH repetition type-B like PUCCH repetition, capture the following in the TR**

**Restriction of the scheme:**

* Only applicable to UCI <=11 bits

**Proposal 4-1b: For PUSCH repetition type-B like PUCCH repetition, captured Table 4 in the TR.**

Table 4: Performance gain observed for PUSCH repetition Type-B like PUCCH repetition

|  |  |  |
| --- | --- | --- |
| Company | Observed performance gain | Key simulation assumptions |
| VIVO | 0.5dB (w/o DMRS bundling)  1~1.5dB (w DMRS bundling)  Note: the 1~1.5 gain observed is a combination of DMRS bundling gain and type-B PUSCH repetition. | 11 bits UCI, w/ DTX detection, 1% BLER  Receiver for Rel-15/16 PUCCH: coherent detection, DTX is performed based on union of DMRS and UCI symbols.  Receiver for PUCCH enhancement scheme: with and without joint channel estimation for the consecutive PUCCH repetitions, in addition to receiver for Rel-15 and Rel-16 UEs.  Note: Ideal noise power estimation is used for above receivers, and the noise power is used only in DTX detection. |

**Proposal 4-2: For PUSCH repetition type-B like PUCCH repetition, capture the following in the TR**

**Potential Spec impact:**

* Nominal repetition, actual repetition, segmentation for type B PUCCH repetition, and flexible time domain resource allocation in each slot need to be specified
* Procedure to handle postpone/cancel PUCCH repetitions (including interaction with dynamic SFI) needs to be specified
* [Upper bound on UCI info bits size needs to be specified]
* [PUSCH type B repetition specification can be leveraged]
* ~~[Procedure to transmit actual repetition in DFT-S-OFDM waveform with 1/2/3 OFDM symbols needs to be specified, if 1/2/3 OFDM symbol actual type B PUCCH repetition is supported]~~
  + ~~[Potentially new DMRS patterns need to be specified]~~
* The issue of whether supporting type B PUCCH repetitions with different PUCCH formats was studied and three options were identified to resolve this issue:
  + Option 1:  Restrict type B PUSCCH repetition applicable to actual repetitions with the same PUCCH format.
  + Option 2: Allow type B PUCCH repetition with different PUCCH formats. The procedure to handle format switch between repetitions needs to be specified.
  + Option 3: Introduce and specify PUCCH format 3/4 of length 1/2/3 OFDM symbols to support type B PUCCH repetition.
* ~~[Procedure and RAN4 requirements to handle different PUCCH formats (with potential switching between different waveforms of OFDM and DFT-S-OFDM) cross actual repetitions needs to be specified, if option 2 is adopted]~~
* Power control for actual repetitions needs to be specified
* ~~[CSI and HARQ-ACK multiplexing with type B PUCCH repetition need to be specified]~~

**Proposal 5-1b: For dynamic PUCCH repetition factor indication, capture Table 5 in the TR.**

Table 5: Performance gain observed for Dynamic PUCCH repetition factor indication

|  |  |  |
| --- | --- | --- |
| Company | Observed performance gain | Key simulation assumptions |
| Ericsson | 5 dB (with repetition factor 8) | 11 bits CSI, w/o DTX detection, 10% BLER  Receiver for Rel-15/16 PUCCH: conventional DMRS based receiver  Receiver for PUCCH enhancement scheme: conventional DMRS based receiver (without cross slot channel estimation). |
| ZTE | Reducing the number of PUCCH repetitions for more than 70% cases. | 11 bits UCI, w/o DTX detection, 1% BLER |

**Proposal 6-1a: For DMRS bundling cross PUCCH repetitions, capture the following in the TR**

**Restriction of the scheme:**

* Phase coherency cross PUCCH repetitions is required
* The same frequency resource allocation cross PUCCH repetitions is required
* The same power cross PUCCH repetitions is required

**Proposal 6-1b: For DMRS bundling cross PUCCH repetitions, capture Table 6 in the TR**

Table 6: Performance gain observed for DMRS bundling cross PUCCH repetitions over Rel-15/16 baseline

|  |  |  |
| --- | --- | --- |
| Company | Observed performance gain | Key simulation assumptions |
| ZTE | 1 dB | 22 bits UCI, w/o DTX detection, 1% BLER, 4 PUCCH repetitions  Receiver for Rel-15/16 PUCCH: ML coherent receiver, w/o cross-slot channel estimation  Receiver for PUCCH enhancement scheme: ML coherent receiver, w/ cross-slot channel estimation |
| Intel | ~1.2 dB | 22 bits UCI, w/o DTX detection, 1% BLER, 8 PUCCH repetitions  Receiver for Rel-15/16 PUCCH: coherent receiver, w/o cross-slot channel estimation  Receiver for PUCCH enhancement scheme: coherent receiver, w/ cross-slot channel estimation |
| VIVO | 0.85 ~ 1.3 dB | 11 bits UCI, w/ DTX detection, 1% BLER, 2 PUCCH repetitions  Receiver for Rel-15/16 PUCCH: Coherent detection, DTX is performed based on union of DMRS and UCI symbols. Channel estimation is performed individually for each repetition.  Receiver for PUCCH enhancement scheme: Joint channel estimation is used for PUCCH repetitions in consecutive slots, in addition to receiver for Rel-15 and Rel-16 UEs.  Note: Ideal noise power estimation is used for both receivers, and the noise power is used only in DTX detection. |

**Proposal 6-3: For DMRS bundling cross PUCCH repetitions, capture the following in the TR**

* New channel estimator needs to be implemented at receiver to process DMRS across multiple repetitions
* Same phase and transmission power need to be maintained at UE cross PUCCH repetitions
* [Maintaining phase coherence across slots requires UE to alter how slot boundaries events (such as timing or power adjustments) are handled]