**3GPP TSG RAN WG1 #103-e R1-200xxxx**

**e-Meeting, October 26th – November 13th, 2020**

**Agenda item:** 7.2.6

**Source:** Moderator (vivo)

**Title:** [103-e-NR-eMIMO-04] Maintenance and TPs for UL Full-Power

**Document for:** Discussion and Decision

Issue1: Draft CR UL.2

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| Following TP can be starting point.**Text proposal for 38.214 v16.3.0**6.2.3.1 UE PT-RS transmission procedure when transform precoding is not enabled< Unchanged parts are omitted >For partial-coherent and non-coherent codebook-based UL transmission, the actual number of UL PT-RS port(s) is determined based on TPMI and/or number of layers which are indicated by *Precoding information and number of layers* field in DCI format 0\_1 and DCI format 0\_2 or configured by higher layer parameter *precodingAndNnumberOfLayers*:- if the UE is configured with the higher layer parameter *maxNrofPorts* in *PTRS-UplinkConfig* set to 'n2', the actual UL PT-RS port(s) and the associated transmission layer(s) are derived from indicated TPMI as:- PUSCH antenna port 1000 and 1002 in indicated TPMI share PT-RS port 0, and PUSCH antenna port 1001 and 1003 in indicated TPMI share PT-RS port 1 except for the cases that *ul-FullPowerTransmission* is configured to *fullpowerMode1*, and TPMI=2 in Table 6.3.1.5-1, or one of the TPMI 12-15 in Table 6.3.1.5-2 and Table 6.3.1.5-3 in [4, TS 38.211] is indicated.- UL PT-RS port 0 is associated with the UL layer 'x' of layers which are transmitted with PUSCH antenna port 1000 and PUSCH antenna port 1002 in indicated TPMI, and UL PT-RS port 1 is associated with the UL layer 'y' of layers which are transmitted with PUSCH antenna port 1001 and PUSCH antenna port 1003 in indicated TPMI, where 'x' and/or 'y' are given by DCI parameter *PTRS-DMRS association* as shown in DCI format 0\_1 and DCI format 0\_2 described in Clause 7.3.1 of [5, TS38.212].- For the cases that *ul-FullPowerTransmission* is configured to *fullpowerMode1*, and TPMI=2 in Table 6.3.1.5-1, or one of the TPMI 12-15 in Table 6.3.1.5-2 and Table 6.3.1.5-3 in [4, TS 38.211] is indicated, PUSCH antenna port 1000, 1001, 1002 and 1003 in the indicated TPMI share PT-RS port 0.< Unchanged parts are omitted > |

Draft CR UL.2, option 2 (R1-2007819)

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| For partial-coherent and non-coherent codebook-based UL transmission, the actual number of UL PT-RS port(s) is determined based on TPMI and/or number of layers which are indicated by *Precoding information and number of layers* field in DCI format 0\_1 and DCI format 0\_2 or configured by higher layer parameter *precodingAndNnumberOfLayers*:- if the UE is configured with the higher layer parameter *maxNrofPorts* in *PTRS-UplinkConfig* set to 'n2', the actual UL PT-RS port(s) and the associated transmission layer(s) are derived from indicated TPMI as:- PUSCH antenna port 1000 and 1002 in indicated TPMI share PT-RS port 0, and PUSCH antenna port 1001 and 1003 in indicated TPMI share PT-RS port 1 except for the cases that *ul-FullPowerTransmission-r16* is set to '*fullpowerMode1*', and TPMI=2 in Table 6.3.1.5-1, or one of the TPMI 12-15 in Table 6.3.1.5-2 and Table 6.3.1.5-3 in [4, TS 38.211] is indicated.- UL PT-RS port 0 is associated with the UL layer 'x' of layers which are transmitted with PUSCH antenna port 1000 and PUSCH antenna port 1002 in indicated TPMI, and UL PT-RS port 1 is associated with the UL layer 'y' of layers which are transmitted with PUSCH antenna port 1001 and PUSCH antenna port 1003 in indicated TPMI, where 'x' and/or 'y' are given by DCI parameter *PTRS-DMRS association* as shown in DCI format 0\_1 and DCI format 0\_2 described in Clause 7.3.1 of [5, TS38.212]. - For the cases that *ul-FullPowerTransmission-r16* is set to '*fullpowerMode1*', and TPMI=2 in Table 6.3.1.5-1, or one of the TPMI 12-15 in Table 6.3.1.5-2 and Table 6.3.1.5-3 in [4, TS 38.211] is indicated, the actual number of UL PT-RS port is 1, where UL PT-RS port 0 is associated with the layer of the UL transmission. |

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| Company  | comments |
| CATT | Support to resolve this issue, with option 2 (c.f. R1-2007819) added above. In our view there are two issues to be resolved: 1. The number of PTRS ports is 1, when rank-1 full-coherent transmission is scheduled.
2. PTRS port 0 is associated with the scheduled UL layer. Our understanding is that 38.214 intends to specify the “*association between PTRS and transmission layer*”, as the 1st paragraph in the current specification reads. Similarly in the 2nd paragraph (current specification) what is specified is the association between “UL PTRS port 0 to UL layer”. Hence specifying PTRS/layer association is consistent with the current specification.
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| Huawei, HiSilicon | Supportive on the proposal. The issue of mismatch between full power Mode-1 and 2-Port PTRS need to be addressed. In current spec, the mapping between PTRS ports and DMRS ports are one-to-one in FDM manner, where the RE mapping of PTRS ports is shown in 6.4.1.2.2.1 in TS 38.211. There is no such case that 2-port PTRS mapping to the one DMRS port in current spec. For the full coherent precoding $\left[1 1 j j\right]$, only 1 port PTRS can be used, shown in 38.214:*“If a UE has reported the capability of supporting full-coherent UL transmission, the UE shall expect the number of UL PT-RS ports to be configured as one if UL-PTRS is configured.”*So, it is ambiguity for supporting two-PTRS ports for the new introduced precoding $\left[1 1 j j\right]$ in Mode-1 full power transmission. |
| QC | Disagree with the proposal. No TP/CR is needed.  This issue has been discussed in last meeting. We don’t see the point to repeat the discussion in this meeting. But since the issue is in email discussion, we share our view as below.Based on current specification, the two PTRS ports are mapped to one identical DMRS port. Current spec has no issue. The CR is not needed. A little bit more explanation as below.Let’s take this example: in full power mode 1, for a 4-Tx partial coherent UE, if gNB schedule 1 layer Tx on DMRS port 0 and TPMI is [1, 1, 1, 1]^T. Based on following current spec, PTRS port 0 is associate to DMRS port 0 and PTRS port 1 is associate to DMRS port 0. Since the two PTRS ports are associated to an identical DMRS port, the two PTRS ports use the same DMRS sequence and same RE mapping. So there is no problem. -     PUSCH antenna port 1000 and 1002 in indicated TPMI share PT-RS port 0, and PUSCH antenna port 1001 and 1003 in indicated TPMI share PT-RS port 1-    UL PT-RS port 0 is associated with the UL layer [x] of layers which are transmitted with PUSCH antenna port 1000 and PUSCH antenna port 1002 in indicated TPMI, and UL PT-RS port 1 is associated with the UL layer [y] of layers which are transmitted with PUSCH antenna port 1001 and PUSCH antenna port 1003 in indicated TPMI, where [x] and/or [y] are given by DCI parameter PTRS-DMRS association as shown in DCI format 0\_1 described in Clause 7.3.1 of [5, TS38.212]. |
| Intel | Support to resolve the issue.We share similar view with CATT and Huawei. The current spec is not clear and needs clarification. |
| Apple | No TP/CR is needed. The outcome is the same with or without TP/CR. |

Issue2: Draft LS UL.4

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| Proposed text for draft LS to RAN2.In RAN1#102-e, the FG 16-5c-3 was agreed with “Candidate component values: any of {2-port {2-bit bitmap}, one of 4-port non-coherent {G0~G3}, one of 4-port partial-coherent {G0~G6}}” which was included in the UE features list in R1-2007326. In RAN1#98, following agreement was made**Agreement**For mode 2, in case of non-coherent with 2 ports, support following TPMI indication for rank 1 which support UL full power transmission:* Rank 1: support {TPMI=0} and {TPMI=1}
* FFS: Details on UE capability signalling

In RAN1#99, following agreements were made**Agreement**For 2 ports, number of bits to indicate TPMI(s) which can deliver UL full power: * 2 bits (bitmap)
* Whether is this capability reporting is optional or not will be discussed as part of UE capability discussions

**Agreement**For 4 ports, number of bits to indicate TPMI(s) which can deliver UL full power:* + Non Coherent 2 bits
	+ Partial coherent 4 bits
		- Additional entries on top of existing entries may be added to table 1 and table 2
	+ Whether is this capability reporting is optional or not will be discussed as part of UE capability discussions

Table 1.

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| 4Tx, nonCoherent | 4Tx, partial coherent (4bit) |
| G0 | G0 |
| G1 | G1 |
| G2 | G2 |
| G3 | G3 |
|  | G4 |
|  | G5 |
|  | G6 |
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Definition of G0~G6 can be found in the table below.Table 2.

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|  | TPMI groups |
| G0 | $\frac{1}{2}\left[\begin{array}{c}1\\0\\0\\0\end{array}\right]$, |
| G1 | $\frac{1}{2}\left[\begin{array}{c}1\\0\\0\\0\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}0\\0\\1\\0\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$, |
| G2 | $\frac{1}{2}\left[\begin{array}{c}1\\0\\0\\0\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}0\\1\\0\\0\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}0\\0\\1\\0\end{array}\right],\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$,$\frac{1}{2}\left[\begin{array}{c}\begin{matrix}0&0\end{matrix}\\\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right],$ $\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0&0\end{matrix}\\\begin{matrix}0&1&0\end{matrix}\\\begin{matrix}0&0&1\end{matrix}\\\begin{matrix}0&0&0\end{matrix}\end{array}\right]$ |
| G3 | $\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$,$\frac{1}{2}\left[\begin{array}{c}\begin{matrix}0&0\end{matrix}\\\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0&0\end{matrix}\\\begin{matrix}0&1&0\end{matrix}\\\begin{matrix}0&0&1\end{matrix}\\\begin{matrix}0&0&0\end{matrix}\end{array}\right]$ |
| G4 | $\frac{1}{2}\left[\begin{array}{c}1\\0\\1\\0\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}1\\0\\-1\\0\end{array}\right],\frac{1}{2}\left[\begin{array}{c}1\\0\\j\\0\end{array}\right]$,$\frac{1}{2}\left[\begin{array}{c}1\\0\\-j\\0\end{array}\right],\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$ |
| G5 | $\frac{1}{2}\left[\begin{array}{c}1\\0\\1\\0\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}1\\0\\-1\\0\end{array}\right],\frac{1}{2}\left[\begin{array}{c}1\\0\\j\\0\end{array}\right]$,$\frac{1}{2}\left[\begin{array}{c}1\\0\\-j\\0\end{array}\right]\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$,$\frac{1}{2}\left[\begin{array}{c}\begin{matrix}0&0\end{matrix}\\\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0&0\end{matrix}\\\begin{matrix}0&1&0\end{matrix}\\\begin{matrix}0&0&1\end{matrix}\\\begin{matrix}0&0&0\end{matrix}\end{array}\right]$ |
| G6 | $\frac{1}{2}\left[\begin{array}{c}1\\0\\1\\0\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}1\\0\\-1\\0\end{array}\right],\frac{1}{2}\left[\begin{array}{c}1\\0\\j\\0\end{array}\right]$,$\frac{1}{2}\left[\begin{array}{c}1\\0\\-j\\0\end{array}\right]$,$ \frac{1}{2}\left[\begin{array}{c}0\\1\\0\\1\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}0\\1\\0\\-1\end{array}\right],\frac{1}{2}\left[\begin{array}{c}0\\1\\0\\j\end{array}\right]$,$\frac{1}{2}\left[\begin{array}{c}0\\1\\0\\-j\end{array}\right]$$\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$, $\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\end{array}\right]$,$\frac{1}{2}\left[\begin{array}{c}\begin{matrix}0&0\end{matrix}\\\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\\\begin{matrix}0&0\end{matrix}\end{array}\right]$,$\frac{1}{2}\left[\begin{array}{c}\begin{matrix}0&0\end{matrix}\\\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\end{array}\right], \frac{1}{2}\left[\begin{array}{c}\begin{matrix}0&0\end{matrix}\\\begin{matrix}0&0\end{matrix}\\\begin{matrix}1&0\end{matrix}\\\begin{matrix}0&1\end{matrix}\end{array}\right],\frac{1}{2}\left[\begin{array}{c}\begin{matrix}1&0&0\end{matrix}\\\begin{matrix}0&1&0\end{matrix}\\\begin{matrix}0&0&1\end{matrix}\\\begin{matrix}0&0&0\end{matrix}\end{array}\right]$ |

RAN1 concluded that the definition of G0~G6 TPMI groups should be captured in 38.306.Action to RAN2:RAN1 respectfully ask RAN2 to take above into account.  |

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| Company  | comments |
| CATT | OK with the LS |
| Huawei, HiSilicon | OK |
| QC | The LS looks fine.  |
| Intel | Fine with the draft. |
| Apple | OK |

Issue3: Draft CR in R1-2008676

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| Company  | comments |
| CATT | OK |
| Huawei, HiSilicon | OK |
| QC | The CR looks fine |
| Intel | OK |
| Apple | OK |

# References

[1] R1-2008140, “Summary for Rel.16 NR eMIMO maintenance”, RAN1#103-e