**3GPP TSG-RAN WG1 Meeting #101-eR1-200xxxx**

**e-Meeting, May 25th – June 5th, 2020**

**Agenda Item:** 7.2.5.7

**Source:** Moderator (LG Electronics)

**Title:** Summary of [101-e-NR-L1enh-URLLC-IIoTenh-02]

**Document for:** Discussion and decision

# Introduction

According to discussion at the preparation phase, the following email thread is allocated by Chairman for further discussion:

[101-e-NR-L1enh-URLLC-IIoTenh-02] Email discussion on the following issues by 5/29 and corresponding TP (if any) by 6/5 – Duckhyun (LGE)

* 3.4. SPS PDSCH release and SPS PDSCH receptions

To address the identified issues from companies’ contributions related to the above email thread, the suggestions for the issues are provided in Section 2. [In Section 3, a few open issues identified are listed up so companies are encouraged to provide your input/feedback in the next meeting in order to facilitate the discussion]. In section [4], the outcome from [101-e-NR-L1enh-URLLC-IIoTenh-02] are provided including all the agreements and all the endorsed TPs.

# Email discussions

## Issue 3.4: SPS PDSCH release and SPS PDSCH receptions

It seems that the issue is how to handle the scenario where **SPS release DCI and SPS PDSCH for the same configuration are received in the same slot**. This scenario can happen at least if 1 slot periodicity is configured.

In this scenario, we will face the following cases:

* Case 1: In a slot, if SPS release DCI is received before the end of the SPS PDSCH for the same SPS configuration
	+ Case 1-1: A UE is not required to receive the SPS PDSCH if HARQ-ACK for the SPS release and the SPS reception would map to different PUCCHs
		- Expected consequence: separate HARQ-ACK bits but NACK for the SPS PDSCH?
	+ Case 1-2: A UE is not required to receive the SPS PDSCH if HARQ-ACK for the SPS release and the SPS reception would map to the same PUCCH
		- Expected consequence: only 1 bit for SPS release
* Case 2: In a slot, if SPS release DCI is received after the end of the SPS PDSCH for the same SPS configuration
	+ Case 2-1: SPS PDSCH is received if HARQ-ACK for the SPS release and the SPS reception would map to different PUCCHs
		- Expected consequence: Separate HARQ-ACK bits
	+ Case 2-2: A UE is not required to receive the SPS PDSCH if HARQ-ACK for the SPS release and the SPS reception would map to the same PUCCH
		- Expected consequence: only 1 bit for SPS release

There were two Questions from the last meeting

**Q1: Which cases are to be disallowed? For any case(s) disallowed, what is the expected UE behavior on HARQ-ACK feedback (especially please provide your feedback if you disagree with the above observation on the expected consequence).**

**Q2: Do you think how to handle the cases above should be differentiated between a UE having processing capability of a single unicast PDSCH reception per slot and a UE having processing capability of more than one unicast PDSCH reception per slot? If so, please provide your reason, and specific solution.**

For the above issues, most companies show their view and preference on Q1.

* Case 1: **ZTE, vivo, Ericsson, Nokia, NEC(1-2 only), Intel(1-2 only), Spreadtrum, LG(1-1 only), QC(1-2 only), Huawei,**
	+ Expected consequence of Case 1-1 (release received first and different PUCCHs)
		- separate HARQ-ACK bits
			* **Nokia, Spreadtrum, LG, Huawei,**
			* **Spreadtrum: NACK for SPS PDSCH**
			* **Nokia**: unless the PUCCH for SPS reception would only contain 1 bit of (NACK) feedback, in which case the PUCCH for SPS reception is not reported
		- only 1 bit for SPS release
			* **Vivo, Ericsson**
	+ Expected consequence of Case 1-2: (release received first and same PUCCHs)
		- separate HARQ-ACK bits
		- only 1 bit for SPS release
			* **Vivo, Ericsson, Nokia, Spreadtrum, Huawei**
		- HARQ-ACK bit for SPS release and SPS PDSCH can be bundled as 1bit if the UE detects that the SPS PDSCH corresponding to the SPS release DCI is actually transmitted in the slot, otherwise, UE generates only the 1-bit HARQ-ACK for the SPS release.
			* **ZTE**
* Case 2: **Ericsson, Nokia(2-1 only), Spreadtrum, LG(1-1 only), Huawei,**
	+ Expected consequence of Case 2-1 (release received later and different PUCCHs)
		- separate HARQ-ACK bits
			* **Spreadtrum, Huawei**
		- only 1 bit for SPS release
			* **Ericsson**
	+ Expected consequence of Case 2-2: (release received later and same PUCCHs)
		- separate HARQ-ACK bits
		- only 1 bit for SPS release
			* **Ericsson, Spreadtrum, Huawei**

For Q2, following are proposed by [1][2][5][7]

* ZTE[1]: No need to differentiate the lower processing capability of a single unicast PDSCH reception per slot and higher capability of more than one unicast PDSCH reception per slot. The key issue is the SPS release DCI and SPS PDSCH occur in one slot. The capability of processing whether one or more than one unicast PDSCH reception doesn’t affect the capability of DCI reception.
* Vivo[2]: For a UE having processing capability of a single unicast PDSCH reception per slot and a UE having processing capability of more than one unicast PDSCH reception per slot, a UE is not required to receive the SPS PDSCH if HARQ-ACK for the SPS release and the SPS reception would map to different PUCCHs or the same PUCCH. UE generates only 1-bit HARQ-ACK for SPS release.
* CATT[5]:
	+ ***For a UE* *not indicating a capability to receive more than one unicast PDSCH per slot,***
		- ***only HARQ-ACK corresponding to the SPS PDSCH release is transmitted and the HARQ-ACK corresponding to the SPS PDSCH is omitted.***
	+ ***For a UE indicating a capability to receive more than one unicast PDSCH per slot,***
		- ***If the HARQ-ACK bit location for the SPS PDSCH release collides with that for an SPS PDSCH, only HARQ-ACK corresponding to the SPS PDSCH release is transmitted and the HARQ-ACK corresponding to the SPS PDSCH is omitted.***
* Intel[7]: UE behavior can be generalized for both types of UEs. The context of Q1 (and Q2) is when release and PDSCH occasion are for/include the same configuration. Thus, the same case (Case 1-2 only) applies for both cases.
* LG[10]:
	+ For a UE not indicating a capability to receive more than one unicast PDSCH per slot
		- Case 2-1 (and 2-2) is not allowed
	+ For a UE indicating a capability to receive more than one unicast PDSCH per slot
		- Case 2-1 is allowed (no spec impact)

## FL’s suggestion on the issue 3.4

There were so diverge views on each case. And the reason why to support each case are also different per companies. One common proposal is Case 1 can be supported. (SPS release received earlier than the end of SPS PDSCH). From FL’s perspective, considering UE processing complexity aspect, I would like to take Case 1 as a baseline and discuss details and whether to extend Case 1.

**Proposal 1: At least, it is allowed that SPS release DCI is received before the end of the SPS PDSCH for the same SPS configuration in a slot.**

* **FFS if SPS release DCI is received after the end of the SPS PDSCH for the same SPS configuration**

Companies are encouraged to provide your feedback (or editorial correction) if any on above proposal.

**Comment:**

|  |  |
| --- | --- |
| Company | Comment if any |
| vivo | We are fine with the proposal in general. Maybe we can also move a little forward by adding UE behavior for above case. For example:**Proposal 1: At least, ~~it is allowed~~ support the case that SPS release DCI is received before the end of the SPS PDSCH for the same SPS configuration in a slot.*** **1 bit HARQ-ACK is generated for SPS release and a UE is not required to receive the SPS PDSCH.**
* **FFS whether and how to support the HARQ-ACK for the SPS release and the SPS reception mapping to different PUCCHs**
* **FFS if SPS release DCI is received after the end of the SPS PDSCH for the same SPS configuration**
 |
| QC | We don’t agree with the proposal, as decision on it quite depends on HARQ-ACK bit generation and UE behavior. We support proposal by vivo, when the second FFS is removed or absorbed under the first FFS, since SPS release DCI after the end of SPS PDSCH may (or may not, needs FFS) be OK only for the case of separate PUCCH for HARQ-ACK report of SPS release and SPS PDSCH. |
| CATT | As we commented during the preparation phase, we have different understandings on the issues. Our understanding is that the issue was first brought up by Nokia for a UE capable of receiving 1 unicast PDSCH only per slot. For this kind of UE, according to Rel-15 Type-1 HARQ-ACK codebook, at most 1 bit is generated per DL slot in a HARQ-ACK codebook so that UE is not expected to receive an SPS PDSCH release in a slot in which UE is expected to receive a unicast PDSCH. However, due to the down to 1 slot SPS PDSCH periodicity, the restriction is not acceptable. Two solutions were proposed. One solution is to assign different K1 values for SPS PDSCH release and for SPS PDSCH so that the HARQ-ACK for the SPS PDSCH release and for SPS PDSCH are to be transmitted in different PUCCH slots. Another solution was to send SPS PDSCH release in the same slot in which the SPS PDSCH for the same SPS configuration is expected to be received and only HARQ-ACK for SPS PDSCH release is included in the HARQ-ACK codebook. Then timeline issue was raised for the second solution.From our point of view, both solutions have its advantage. It can be left to gNB to decide. For the second solution, we do not think the timeline is needed given that there is always sufficient processing time for the last SPS PDSCH or SPS PDSCH release and we do not expect UE to generate/update the HARQ-ACK codebook each time a SPS PDSCH or SPS PDSCH release DCI is decoded. Instead, we expect that UE would generate the HARQ-ACK codebook when all the HARQ-ACK bits for the HARQ-ACK codebook are ready.Based on the above understandings, our proposals are as follows taking both same-carrier and cross-carrier scheduling into account and take both UE capabilities of 1 unicast PDSCH and more than one unicast PDSCH per slot into account.***For same-carrier scheduling, if an SPS PDSCH release is received in a slot in which UE is configured to receive SPS PDSCH(s) and the HARQ-ACK corresponding to the SPS PDSCH release and SPS PDSCH(s) are to be transmitted in the same PUCCH, or******For cross-carrier scheduling, if*** ***UE is configured to receive SPS PDSCH(s) on scheduled cell in the last slot overlapping with*** ***an SPS PDSCH release on scheduling cell and the HARQ-ACKs for the SPS PDSCH release and the SPS PDSCH(s) on the scheduled cell are expected to be transmitted in the same PUCCH,**** ***For a UE*** ***not indicating a capability to receive more than one unicast PDSCH per slot,***
	+ ***only HARQ-ACK corresponding to the SPS PDSCH release is transmitted and the HARQ-ACK corresponding to the SPS PDSCH is omitted.***
* ***For a UE indicating a capability to receive more than one unicast PDSCH per slot,***
	+ ***If the HARQ-ACK bit location for the SPS PDSCH release collides with that for an SPS PDSCH, only HARQ-ACK corresponding to the SPS PDSCH release is transmitted and the HARQ-ACK corresponding to the SPS PDSCH is omitted.***
 |
| ZTE | Agree |
| Nokia, NSB | As Vivo pointed out, the proposal seems incomplete since it is not specifying what the UE behavior should be for the SPS PDSCH and HARQ-ACK reporting – and there seems to be some relation in this respect with other proposals below. We overall agree with Vivo’s proposal, and the following edits are proposed to address QC’s concerns:**Proposal 1: At least, ~~it is allowed~~ support the case that SPS release DCI is received before the end of the SPS PDSCH for the same SPS configuration in a slot.*** **1 bit HARQ-ACK is generated for SPS release and a UE is not required to receive the SPS PDSCH.**
* **FFS whether and how to support the HARQ-ACK for the SPS release and the SPS reception mapping to different PUCCHs**

**FFS ~~if~~ whether and how to support the case that SPS release DCI is received after the end of the SPS PDSCH for the same SPS configuration** |
| NEC | We agree with the proposal in general however, as pointed out by Nokia, UE behavior should be added. Therefore, we support Proposal 1 from Nokia. |
| Apple | We agree with Nokia’s proposal, since the gNB is going to release the SPS configuration, reception of the last SPS PDSCH is not important.  |
| Samsung | We are fine with the intention of the proposal. However, we would like to clarify whether the timeline is for all the cases or it is limited to Type-1 HARQ-ACK codebook.As we have commented during last meeting, the timeline needs to be clarified for SPS PDSCH overlapping handling and for SPS PDSCH HARQ-ACK codebook as well. If a UE receives a DCI indicating SPS release, the accurate time when the SPS PDSCH configuration should be considered to be released should be clarified, otherwise, there might be misunderstanding between UE and gNB. For the SPS PDSCH HARQ-ACK codebook, the construction is for activated SPS PDSCHs, the release of an SPS PDSCH configuration will change the construction of the HARQ-ACK codebook. The timeline also impacts the SPS PDSCH overlapping handling. If there is misunderstanding between UE and gNB, UE may receive unexpected SPS PDSCH(s).For simplicity, we suggest that a unified timeline should be defined |
| Intel | We can accept Proposal 1 from Nokia. BTW, the last FFS in Nokia’s proposal should perhaps be a sub-bullet. |
| LG | Support revised proposal from Nokia.  |
| HW/HiSi | Fine with the proposal, but also capturing the UE behavior would be desirable. Therefore we also agree to the proposal from Nokia. |
| DOCOMO | Agree with the proposal from Nokia |

According to following specification, PUCCH for SPS PDSCH release is determined by a value of a PDSCH-to-HARQ\_feedback timing indicator. Thus, there was no restriction of same PUCCH between release and SPS PDSCH at least for a UE having processing capability of more than one unicast PDSCH reception per slot.

|  |
| --- |
| 9.1.2 Type-1 HARQ-ACK codebook determinationThis clause applies if the UE is configured with *pdsch-HARQ-ACK-Codebook = semi-static*.A UE reports HARQ-ACK information for a corresponding PDSCH reception or SPS PDSCH release only in a HARQ-ACK codebook that the UE transmits in a slot indicated by a value of a PDSCH-to-HARQ\_feedback timing indicator field in a corresponding DCI format 1\_0 or DCI format 1\_1. The UE reports NACK value(s) for HARQ-ACK information bit(s) in a HARQ-ACK codebook that the UE transmits in a slot not indicated by a value of a PDSCH-to-HARQ\_feedback timing indicator field in a corresponding DCI format 1\_0 or DCI format 1\_1.  |

**Proposal 2: At least for a UE having processing capability of more than one unicast PDSCH reception per slot, it is allowed to receive SPS PDSCH release in same slot where corresponding SPS PDSCH is configured to be received if HARQ-ACK for the SPS release and the corresponding SPS reception would map to different PUCCHs.**

Companies are encouraged to provide your feedback (or editorial correction) if any on above proposal.

**Comment:**

|  |  |
| --- | --- |
| Company | Comment if any |
| vivo | We would like to clarify the relation between proposal 1 and proposal 2. Proposal 1 seems applied to UEs both capable and incapable of processing more than one unicast PDSCH reception per slot. If the updated proposal including the red sentences is acceptable, then proposal 2 is covered by proposal 1.  |
| QC | Please see comment under proposal 1. We share a similar view with vivo that proposal 2 can be put as FFS under proposal 1. |
| CATT | Please see our comments under proposal 1. |
| ZTE | Agree. But one more thing needs clarification.For semi-persistent codebook construction, the PUCCH1 is assumed to be used for the HARQ-ACK codebook of SPS release, the codebook will be constructed based on the k1 set. As the SPS release and SPS PDSCH are in the same slot, although the valid HARQ-ACK of SPS PDSCH will be transmitted in the other PUCCH2, but following the principle of that the codebook for release is based on k1 set, there could be one NACK bit for SPS PDSCH (ignored by gNB) in PUCCH1 but actually there is only one bit capacity for HARQ-ACK information of release and PDSCH in PUCCH1, this is the controversial point here. |
| Nokia, NSB | We agree with the intention, but as noted by vivo there is some related with the first proposal. If we have the FFS on HARQ-Ack, then at least this case is covered above already (and independently of the UE capability).  |
| NEC | We agree with other companies that proposal 2 can be covered with the FFS under proposal 1. |
| Apple | The solution to Q.1 can be used for Q.2 also. |
| Samsung | We don’t understand the intention of the proposal. For a UE having processing capability of more than one unicast PDSCH reception per slot, this proposal is the Rel-15 behavior, if we would like to clarify it, proposed conclusion is preferred. There should be no spec impact.  |
| Intel | Agree with vivo and Qualcomm |
| HW/HiSi | Agree with comments from other companies. Proposal 2 is not needed, since it is covered by proposal 1. |
| DOCOMO | Agree with the intention but we are fine to keep this proposal as FFS |

As a next, I also would like to ask some principle to solve the problem in order to step forward.

For the processing capability of a single unicast PDSCH reception per slot, there are two meaning. One is that UE is only capable to decode one PDSCH per single slot. The other is that UE generates most single HARQ-ACK bit per slot (Of course, they can be transmitted in one PUCCH by multiplexing). Based on proposals from companies’ contributions, there is no issue with former one. However, I think a latter part can be related to this issue. Thus, the additional Question is,

**Q3: For a UE having processing capability of a single unicast PDSCH reception per slot, is it possible to generate two HARQ-ACK bits for SPS PDSCH release and SPS PDSCH reception in a slot?**

Companies are encouraged to provide your feedback (or editorial correction) if any on above Question.

**Comment:**

|  |  |
| --- | --- |
| Company | Comment if any |
| vivo | No, from our understanding the HARQ-ACK generation is part of PDSCH processing. So, for a UE having processing capability of a single unicast PDSCH reception per slot, one HARQ-ACK is generated.  |
| QC | No, For a UE incapable of processing more than one unicast PDSCH per slot, only single HARQ-ACK bit is supposed to be generated per slot  |
| CATT | Although we understand the intention, the question is not accurate.Our understanding is that for a UE having processing capability of a single unicast PDSCH reception per slot, it is NOT possible to generate more than one HARQ-ACK bits for SPS PDSCH release and SPS PDSCH reception in a slot for a Type-1 HARQ-ACK codebook in an UL slot. |
| ZTE | Not agree. We don’t support **two** HARQ-ACK bits in the **same** PUCCH for SPS PDSCH release and SPS PDSCH reception in a slot. If there are two PUCCHs for SPS PDSCH release and SPS PDSCH reception, the two separate HARQ-ACK bits will be in different PUCCHs, it is possible.Just as the clarification answer for proposal 2, it is impossible to place the two HARQ-ACK bits of release and PDSCH into the PUCCH with 1 bit capacity. So this question 3 is not relevant with whether multiple SPS PDSCH or only one SPS PDSCH as UE may not receive. And we assume the question 3 is not relevant to the different PUCCHs for release DCI and SPS PDSCH here. |
| Nokia, NSB | Yes, for Type-2 HARQ-ACK codebook: separate HARQ-ACK bits are generated for SPS PDSCH release and SPS PDSCH reception in a same slot.No for Type-1 codebook (as also pointed out by vivo and QC): only single HARQ-ACK bit is generated per slot.  |
| NEC | According to our understanding, for a UE having processing capability of a single unicast PDSCH reception per slot, only single HARQ-ACK bit is generated. |
| Apple | The need to generate HARQ-ACK for SPS reception which is to be released in the same slot is not obvious; a single HARQ feedback bit is enough. |
| Samsung | Not support. This will double the size of Type-1 HARQ-ACK codebook. Since the size of Type-1 HARQ-ACK codebook is determined by RRC, to support this feature, there will always be two bits per slot in the HARQ-ACK codebook per carrier. |
| Intel | No; agree with vivo and Qualcomm. Changing UE behavior for support of multiple HARQ-ACK bits for a single DL slot is not reasonable for a UE supporting a single unicast PDSCH per slot. |
| HW/HiSi | No. Only a single HARQ-ACK bit is generated |
| DOCOMO | No. Only single HARQ-ACK bit is generated per slot |

Depending on the upcoming discussion, UE may receive SPS PDSCH release of which HARQ-ACK would map to same or different PUCCH with the corresponding SPS PDSCH reception. Thus, it would be helpful to discuss for each cases in advance.

If HARQ-ACK for the SPS release and the SPS reception would map to the **same PUCCH**, i.e., SPS PDSCH release is indicated with same value of K1 with SPS configuration, they would be mapped to same HARQ-ACK bit position in the PUCCH based on current specification. In this case, we should consider DCI missing case.



**Figure: An example of DCI missing case when both HARQ-ACKs are mapped to same PUCCH**

In the situation above, there could be ambiguity on HARQ-ACK bit between SPS PDSCH release and SPS reception due to DCI missing case. Based on the contribution, most of companies proposed “UE generates only 1 bit for SPS release” when same PUCCH is used. In this case, gNB is able to ensure no successful transmission on the SPS PDSCH by gNB implementation so that UE always report NACK for the SPS reception bit even if UE fails to detect SPS release DCI.

**Proposal 3:** **If it is supported that HARQ-ACKs corresponding to a SPS release and a SPS reception in a slot map to the same PUCCH (i.e., same HARQ-ACK bit in the PUCCH), UE generates only 1 bit corresponding to the SPS release for the slot.**

Companies are encouraged to provide your feedback (or editorial correction) if any on above proposal.

**Comment:**

|  |  |
| --- | --- |
| Company | Comment if any |
| vivo | Agree. We would like to point out the example may not exist. Since if gNB wants to send SPS release, it should not transmit SPS PDSCH; if gNB wants to transmit the ‘last’ SPS PDSCH in slot n-2, then gNB can send SPS release only in slot n-1.  |
| QC | We share the same view with vivo. Basically, for the case of UE receives SPS release PDCCH in a same slot that UE is configured to receive SPS PDSCH, UE does NOT expect to detect SPS PDSCH on that slot. That is how single bit HARQ-ACK works: where a NACK means UE has missed SPS release PDCCH, while Ack means UE has detected SPS release. No ambiguity between UE and gNB. |
| CATT | According to our proposal under Q1, we agree to generate 1 bit HARQ-ACK for SPS PDSCH release for a UE capable of 1 unicast PDSCH per slot if the HARQ-ACK for the SPS PDSCH release and the SPS PDSCH are to be transmitted in the same PUCCH.  |
| ZTE | Partially agree, We agree only one bit to feedback the HARQ-ACK information corresponding to a SPS release and a SPS reception in a slot in the scope of this proposal. The one bit can correspond to the SPS release, or can correspond the bundling result of HARQ-ACK information of SPS release and SPS PDSCH. We are open to the two alternatives and could following the majority views.The simplest solution is that the UE is not expected the SPS release DCI and corresponding SPS PDSCH in the same slot. But if most companies think we should consider this scenario, there could be some solutions for it.1. One bit only for SPS release,

If the HARQ-ACK for release and PDSCH are in the same PUCCH, the consequence is SPS PDSCH will be 100% retransmitted as no HARQ-ACK for SPS PDSCH.If the HARQ-ACK for release and PDSCH are in the different PUCCHs, the specification work is also needed to define the PUCCH corresponding to the SPS release will not include the HARQ-ACK information of SPS PDSCH although it is NACK for SPS PDSCH if we following the current specification.1. HARQ-ACK bundling between the HARQ-ACK information of SPS release and SPS PDSCH reception.

The bundling approach could solve the 100% retransmission of SPS PDSCH in case of the same PUCCH, the possibility of retransmission of SPS PDSCH will be reduced to 10% for eMBB traffic and 0.01% for URLLC traffic, the shortcoming is that the reliability of release DCI reception would be cut down to the same level of SPS PDSCH of eMBB. The shortcoming is not applied to URLLC traffic as the missing detection requirement of URLLC is comparable to or better than release DCI missing detection rate. If SPS PDSCH with 1 slot periodicity is mainly for URLLC traffic, considering the balance between the reliability and possibility of retransmission, we suggest HARQ-ACK bundling solution in the case of SPS release and a SPS reception in a slot mapping to the same PUCCH. |
| Nokia, NSB | We suggest to have separate proposals for Case 1 (release DCI received before the end of SPS PDSCH) and Case 2 (release DCI received after the end of SPS PDSCH, which would be FFS based on the modified Proposal 1). - For Case 1, we agree with the proposal since only 1 bit is anyway generated. - For Case 2, we prefer to first agree on the UE behavior for receiving or not the SPS PDSCH since this would determine the number of HARQ-ACK bits that are generated in the slot. |
| NEC | Agree. |
| Apple | Agree with the FL proposal, supporting case 1 should be sufficient. |
| Samsung | We agree with the intention of the proposal but the wording seems to be misleading. Does it refer to the case where UE is capable of receiving one PDSCH per slot? If so, 1 bit per slot is the Rel-15 behavior. We also share similar understanding with vivo regarding the example. Bundling operation proposed by ZTE seems to be optimization. We don’t need to discuss about it in the CR phase. |
| Intel | Agree with response from vivo and QC. There should not be an ambiguity in the first place, the SPS release is prioritized under condition that the release DCI precedes the SPS PDSCH. |
| HW/HiSi | Agree |
| DOCOMO | Agree with the proposal |

If HARQ-ACK for the SPS release and the SPS reception would map to the **different PUCCH**, i.e., SPS PDSCH release is indicated with different value of K1 with SPS configuration, there seems no ambiguity at the gNB perspective. Based on contributions, the majority of companies thinks that UE can generates separated PUCCH in this case.



**Figure: An example of DCI missing case when both HARQ-ACKs are mapped to same PUCCH**

For the decoding of SPS reception, there are a lot of view per different conditions. First of all, I would like to suggest to consider baseline above first.

**Proposal 4:**

* **At least for a UE having processing capability of more than one unicast PDSCH reception per slot,**
	+ **If SPS release DCI is received before the end of the SPS PDSCH for the same SPS configuration in a slot and (i.e., Case 1),**
	+ **If HARQ-ACK for the SPS release and the SPS reception would map to the different PUCCHs,**
	+ **Down-select among following options:**
		- **Opt. 1: the UE is not required to receive the SPS PDSCH if SPS release is detected.**
		- **Opt. 2: the UE is required to receive the SPS PDSCH even if SPS release is detected.**

Companies are encouraged to provide your feedback (or editorial correction) if any on above proposal.

**Comment:**

|  |  |  |
| --- | --- | --- |
| Company | Preferred Options | Comment if any |
| vivo | Option 1  | Irrespective of a UE having processing capability of more than one unicast PDSCH reception per slot or not, it should be the common understanding that if gNB plans to send the SPS release PDCCH in a slot, then the gNB will not schedule the SPS PDSCH in the same slot. So, from gNB perspective, it does not expect to receive the HARQ-ACK feedback for the released SPS PDSCH. From UE perspective, based on the last e-meeting email discussion, as long as the SPS release DCI is received before the end of the SPS PDSCH for the same SPS configuration, HARQ-ACK generation for SPS PDSCH can be interrupted, instead the 1-bit HARQ-ACK can be generated only for SPS release. Therefore, we prefer option 1. In addition, we are fine to support case 1-2 only.  |
| QC | Do not support | In our view, case 1-2 only is sufficient to address the issue of releasing a SPS configuration in a slot that SPS PDSCH is configured to be received. Further, we think separate PUCCH is not a good solution. At least it shall not be the only solution for this issue. Under the assumption that separate PUCCH is not the only specification, option 1 is more meaningful that is UE does not expect to detect SPS PDSCH in a slot that UE receives SPS release PDCCH.  |
| CATT |  | Please see our comments under proposal 1. |
| ZTE | Option2 | As the above analysis, UE can feedback the valid HARQ-ACK information bits for SPS release and SPS PDSCH separately in different PUCCH. So UE is required to receive the SPS PDSCH even if SPS release is detected.In the PUCCH corresponding to SPS release, there is only one bit correspond to SPS release. |
| Nokia, NSB | Option 1 | This case seems very related to updated proposal 1 from Vivo.And if we go for Option 1 (i.e. SPS PDSCH is not received), then actually there would not be HARQ-Ack for SPS (.. and then it would not really matter if they would point to the same or different PUCCH in the end, as either the release DCI is Acked or the UE misses and reports NACK for the PDSCH which is not transmitted. Therefore, the 2nd bullet point (i.e. *If HARQ-ACK for the SPS release and the SPS reception would map to the different PUCCHs*’) to our understanding based on Option 1 would not be needed.  |
| NEC | Option 1 | It is our understanding that Option 1 implies that the gNB does not expect HARQ-ACK feedback for the released SPS PDSCH. |
| Apple | Option 1 | Supporting case 1 should be sufficient. Agree with some comments from vivo also, since the gNB is going to release the SPS configuration, we question how useful the HARQ feedback for the last SPS reception is, even if the UE receives the SPS reception.  |
| Samsung | Option 1 | According to 38.321, UE does not expect to receive an SPS PDSCH after the SPS release DCI being received. If the timeline is clear, UE does not expect to receive the SPS PDSCH.TS 38.3212> if the NDI in the received HARQ information is 0:3> if PDCCH contents indicate SPS deactivation:4> clear the configured downlink assignment for this Serving Cell (if any); |
| Intel | Option 1 | UE should never be required to receive an SPS PDSCH ending after a release DCI is received in the same slot for the same configuration (can be seen as a direct consequence of the explanation from Samsung above).  |
| HW/HiSi | Option 1 | We share the view of vivo. |
| DOCOMO | Option 1 | Agree with vivo |

<updated 5/27>

## 2nd FL suggestion (5/27)

As I mentioned, Proposal 1 is to determine our baseline for further discussion. So there is no issue to have multiple FFS for proposal 1. The reason why I had not added FFS is that 7 or 8 FFS would be need and also not meaningful.

We have multiple classification of at least following based on comments.

* Timeline of release DCI
* Same/different PUCCH
* UE capability of single or more than one unicast PDSCH per slot
* Whether to receive SPS PDSCH in the slot
* Self-carrier/cross carrier scheduling
* Type 1/Type 2 codebook

For sure, we cannot discuss these 64(2^6) case for each. We cannot agrees those things at once as well by one proposal. Therefore, all proposal is for step by step discussion so that any proposal doesn’t preclude any other case expect when it is explicitly mentioned. Regardless of FFS or not, we should solve identified issue and it is highly recommended to finalize in this meeting. Please consider above. I understand some companies want to support A-B combination and other companies want to support A-C combination. In that case, I hope that both of them won’t object ‘A’. We really need to reduce cases before final decision.

Based on the comment, hopefully there seems majority views on few things:

* **At least support the case that SPS release DCI is received before the end of the SPS PDSCH for the same SPS configuration in a slot for cases which we want to support.**
* **For a UE having processing capability of a single unicast PDSCH reception per slot, same PUCCH case should be considered for cases which we want to support.**
	+ **HARQ-ACK for the SPS release and the SPS reception would map to the same PUCCHs**
	+ **1 bit HARQ-ACK is generated for SPS release and a UE is not required to receive the SPS PDSCH.**
* **for a UE having processing capability of more than one unicast PDSCH reception per slot,**
	+ **HARQ-ACK for the SPS release and the SPS reception would map to the same/different PUCCHs for cases which we want to support**
		- **In case of same PUCCH, 1 bit HARQ-ACK is generated for SPS release and a UE is not required to receive the SPS PDSCH.**
		- **In case of different PUCCH, the UE is not required to receive the SPS PDSCH if SPS release is detected.**
* **It is FFS whether and how to support the case that SPS release DCI is received after the end of the SPS PDSCH for the same SPS configuration**

I made revised proposal 1 based on Nokia’s modification, which has majority support.

**@All:**

On the previous proposal 3, I agree with that gNB would ensure no PDSCH transmission in the slot where UE received release DCI if there could be ambiguity. but It would be not desirable to specify gNB’s behavior. I think “1 bit HARQ-ACK is generated for SPS release and a UE is not required to receive the SPS PDSCH” is sufficient. If UE misses release DCI, anyway UE would try to receive. If UE receives release DCI, UE is not required to receive the SPS PDSCH. Please check revised proposal.

**@CATT:**

I cannot sure I understood correctly. I understand we can leave something to gNB implementation. But we need to solve that issue for some UE, and some cases. And we are discussing which case need to be solved and what gNB’s proper behavior is. I think we are still in between two solutions.

Regarding self-/cross-carrier scheduling, I need bit more explanations. According to your proposal, I don’t see what makes difference between self-/cross-carrier scheduling, expect for they can be in different HARQ-ACK bit in the same PUCCH. But it is existing case

**@Samsung:**

I think codebook shouldn’t impact on timeline in principle. Though, Type 2 codebook make a bit difference on HARQ-ACK bit position. I replace the wording “same HARQ-ACK bit” with “same PUCCH”. Since for type 1, anyway they are mapped to same HARQ-ACK bit.

**@QC:**

I saw you have a concern on last FFS part. However, as a feature lead, it is not good way to preclude something without discussion/consensus. Regardless of FFS, we can discuss that since it listed in the last meeting. Please consider this.

**@ZTE:**

For HARQ-ACK bundling, I saw that most companies thinks gNB would ensure that UE does not detect PDSCH in that slot. In this case, bundling has no meaning anymore. For sake of the progress, please consider that.

**Revised Proposal 1&2&3: At least, support the case that SPS release DCI is received before the end of the SPS PDSCH for the same SPS configuration in a slot.**

* **For a UE having processing capability of a single unicast PDSCH reception per slot,**
	+ **1 bit HARQ-ACK is generated for SPS release and a UE is not required to receive the SPS PDSCH.**
	+ **HARQ-ACK for the SPS release and the SPS reception would map to the same PUCCHs**
* **for a UE having processing capability of more than one unicast PDSCH reception per slot,**
	+ **1 bit HARQ-ACK is generated for SPS release and a UE is not required to receive the SPS PDSCH**
	+ **HARQ-ACK for the SPS release and the SPS reception would map to the same or different PUCCHs**
* **FFS whether and how to support the case that SPS release DCI is received after the end of the SPS PDSCH for the same SPS configuration**

Companies are encouraged to provide your feedback (or editorial correction) if any on above proposal.

**Comment:**

|  |  |
| --- | --- |
| Company | Comment if any |
| HW/HISI | We are fine with the proposal. |
| Nokia, NSB | Disagree on different handling (i.e. no need to distinguish based on UE capability here). We do not understand the motivation for specifying separate behaviors for UEs with or without the capability of receiving multiple unicast PDSCH per slot, especially when the only difference is that, for single PDSCH reception per slot, HARQ-ACK of SPS release and SPS PDSCH is restricted to same PUCCH (i.e. different PUCCH is not allowed).The behavior for SPS PDSCH reception and SPS release of the same configuration in a slot is exactly the same regardless of the UE capability: they are mapped to the same bit position if they are associated to the same PUCCH, but it should also be possible to report them on different PUCCHs.  |
|  |  |
| QC | We share a similar view with Nokia/NSB. Klaus’s proposal seems fine to us with this change**Proposal: At least, it is allowed to support the case that SPS release DCI is received before the end of the SPS PDSCH for the same SPS configuration in a slot.*** **1 bit HARQ-ACK is generated for SPS release and a UE does not expect to detect the SPS PDSCH.**
* **HARQ-ACK for the SPS release and the SPS reception would map to the same PUCCHs**
* **FFS whether and how to support the HARQ-ACK for the SPS release and the SPS reception mapping to different PUCCHs**
* **FFS if whether and how to support the case that SPS release DCI is received after the end of the SPS PDSCH for the same SPS configuration**

“UE does not expect to detect” is to ensure no PDSCH transmission in the slot where UE received release DCI, as we know this may cause ambiguity of ACK. |
| DOCOMO | As only 1 bit HARQ-ACK is generated for SPS release and UE is not required to receive the SPS PDSCH for both of the UE having/not having the capability of more than one unicast PDSCH reception per slot, it is enough to support the case when HARQ-ACK for the SPS release and the SPS reception would map to the same PUCCH. We are also OK with the proposal from Qualcomm. |

</updated 5/27>

# Open issues to be discussed

For section 3, it is recommended for companies to take into account the issues carefully and to come back with sufficiently specific options/preference/suggestions to the next meeting so that we can complete RAN1 works on the relevant functionalities with respect to specification.

# Final outcome from [101-e-NR-L1enh-URLLC-IIoTenh-02]

# References

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