3GPP TSG-RAN WG1 Meeting #100bis-e R1-20xxxxx

e-Meeting, 20th – 30th April, 2020

Agenda Item: 7.2.2.1.3

Source: Moderator (Ericsson)

Title: FL Summary for [100b-e-NR-unlic-NRU-ULSignalsChannels-01] Email discussion/approval

Document for: Discussion, Decision

# 1 Introduction

Based on the conclusion of the e-meeting preparation phase [21] and the vice-Chairman’s guidance, the following e-mail discussion has been kicked-off:

[100b-e-NR-unlic-NRU-ULSignalsChannels-01] Email discussion/approval on the following issues

by 4/23; if necessary, followed by endorsing the corresponding TPs by 4/29 – Steve (Ericsson)

* Finalize design for FDRA field of DCI 0\_0 for UL resource allocation Type 2
* Editorial correction on interlace configuration

The following topics are included in this email discussion

|  |  |  |  |
| --- | --- | --- | --- |
| **Issue** | **Description** | **Tdoc References** | **Class** |
| 1 | FDRA field for DCI 0\_0 for UL resource allocation Type 2:   * Issue 1-1:   DCI 0\_0 in a CSS: Agree on rule for RB set allocation for PUSCH   * Isuee 1-2:   DCI 0\_0 in a USS: Agree on whether or not FDRA field includes Y bits for RB set allocation + rule for RB set allocation for PUSCH (if Y bits not included) or value of Y (if Y bits included)  TPs needed to 38.212 §7.3.1.1.1 and 38.214 §6.1.2.2.3 | R1-2002321: P1,P2  R1-2002030: P1,P2  R1-2001875: P1-P3  R1-2001533: P1  R1-2001934: P1-P4  R1-2001973: P2-P4  R1-2002433: P1  R1-2001758: P1  R1-2002116: P1  R1-2002382: P1-P3  R1-2002276: P1-P2  R1-2001704: P1-P2  R1-2001651: P1-P2 | Critical |
| 2 | Clarify that minimum number of resource blocks within an interlace contained in a BWP is 10 (Interlaced transmission not supported for 10 MHz SCell)  Simple TP needed to 38.211 §4.4.4.6 | R1-2002030: P6  R1-2001533: P2  R1-2001986: §2.2 | Editorial |

The following company views were captured in the e-meeting preparation phase [21]:

**Issue 1-1: Alternatives for RB set allocation for PUSCH scheduled by DCI 0\_0 in CSS:**

* Alt-1: PUSCH allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received
* Alt-2: PUSCH allocated to RB set 0 of the active UL BWP
* Alt-3: PUSCH allocated to all RB sets of the active UL BWP
* Alt-4a/b: PUSCH allocated to RB set(s) according to the following logic:
  + Alt-4a (ref: [4]):
    - If the active UL BWP does not include all of the RBs of the initial UL BWP or the active UL BWP has different SCS than the initial UL BWP, then
      * RB set 0 of the active UL BWP
    - Otherwise
      * RB set of the initial UL BWP
  + Alt-4b (ref: [18]):
    - If the active UL BWP includes all of the RBs of the initial UL BWP and the SCS/CP of the active UL BWP is the same as that of the initial UL BWP or the initial UL BWP is active
      * the initial UL BWP
    - Otherwise
      * All RB sets of the active UL BWP

|  |  |
| --- | --- |
| **Company** | **View/Position** |
| Apple | Alt-1 |
| Ericsson | Alt-1 |
| Fujitsu | Alt-1 |
| LGE | Alt-1 |
| DOCOMO | Alt-1 |
| OPPO | Alt-4a |
| Samsung | Alt-3 |
| Sharp | Alt-4b |
| Spreadtrum | Alt-2  Please do not update this table. See new table in Section 2.1.1. |
| ZTE | Alt-1 |
| vivo | Alt-2 |
| Lenovo | Alt-2 |
| Qualcomm | Alt-2 |
| Nokia, NSB | Alt-1 |
| Huawei | Alt-1 |

**Issue 1-2: Alternatives for FDRA field of DCI 0\_0 in a USS:**

* Alt-1: FDRA field of DCI 0\_1 in a USS contains X bits only
  + Alt-1a: PUSCH allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received
  + Alt-1b: PUSCH allocated to RB set 0 of the active UL BWP
* Alt-2: FDRA field of DCI 0\_1 in a USS contains X + Y bits
  + Alt-2a: Y is variable and given by size of active UL BWP
  + Alt-2b: Y is fixed at [4] bits

|  |  |
| --- | --- |
| **Company** | **View/Position** |
| Apple | Alt-2a |
| Ericsson | Alt-1a |
| Fujitsu | Alt-1a |
| Huawei | Alt-2a |
| LGE | FFS between Alt-1a and Alt-2a |
| Lenovo | Alt-1b |
| DOCOMO | Alt-1a |
| OPPO | Alt-2a |
| Samsung | Alt-2b  Please do not update this table. See new table in Section 2.1.2. |
| Sharp | Alt-2 |
| Spreadtrum | Alt-1b |
| ZTE | Alt-2 |
| vivo | Alt-2a |
| Qualcomm | Alt-1b |
| Nokia, NSB | Alt-1a |

# 2 Discussion

## 2.1 FDRA Field for DCI 0\_0

### 2.1.1 Issue #1-1: DCI 0\_0 in a CSS

Judging by company responses in the preparation phase, there is clear majority support for either Alt-1 and Alt-2 for PUSCH scheduled by DCI 0\_0 received in a CSS. It is the FL’s proposal to limit discussion to of these two alternatives during this week.

1. The following is proposed for discussion this week, with down selection completed by 10/23. FL to draft TPs after down-selection.

* For PUSCH scheduled by DCI 0\_0 received in a CSS when UL resource allocation Type 2 is configured, down-select to one out of the following two alternatives for the RB set allocation:
  + **Alt-1**: PUSCH is allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received
  + **Alt-2**: PUSCH is allocated to RB set 0 of the active UL BWP

One technical aspect that has not been addressed in contributions is that Alt-2 effectively introduces “cross RB Set” scheduling (unless DCI 0\_0 is also transmitted in RB Set 0). In other words, the gNB transmits DCI 0\_0 in an arbitrary RB set, but the PUSCH transmission is always in RB Set 0. If LBT is successful at the gNB in DL RB Set X, isn’t there a higher chance that LBT is successful at the UE in the UL RB Set that overlaps X? Recall that the goal of DCI 0\_0 is for robust behaviour.

**FL recommendation**: A solution is needed for this issue in order to complete the DCI 0\_0 design. Companies are encouraged to provide technical merits of their preferred alternative. If no consensus can be achieved by 10/23, it is recommended to go with the majority view. Note: Currently there are 8 companies supporting Alt-1 and 4 companies supporting Alt-2.

Please provide your company view on the above two alternatives:

|  |  |
| --- | --- |
| **Company** | **View/Position** |
| Sharp | I have a question for both alternatives. When the size of uplink carrier is 80 MHz and the active UL BWP is 20 MHz, and intra-cell guard bands nor RB-sets provided, how is the UE scheduled a PUSCH? The RB-set in which the PUSCH is scheduled is the RB-set which corresponds to the uplink carrier? |
| LG Electronics | Alt-1  Also, regarding to this issue, the reference BWP to determine the size of X bit in FDRA field of DCI format 0\_0 needs to be clarified as below.  - For DCI format 0\_0 transmitted in CSS, X bit size of FDRA field in the DCI format 0\_0 is determined based on the SCS of the initial UL BWP as in legacy Rel-15 |
| Lenovo, Motorola Mobility | We support Alt-2 since it is simpler than Alt-1.  Comments to Alt-1: if the current active DL BWP has no any overlapping with current active UL BWP in frequency domain, how can it work? |
| NTT DOCOMO | Support Alt-1. Agree with FL that Alt-1 has higher chance that LBT is successful in the UL RB set allocated to the PUSCH |
| ZTE | Support Alt.1 |
| Huawei | Basically support Alt-1, which is benefit for UE to share the COT from gNB. But we have similar concern as Sharp, if no intra-cell guardband is configured, there is only one RB set. Then “the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received” is not clear. Our suggestion is waiting for the conclusion in wideband discussion. |
| Nokia, NSB | Alt - |
| Panasonic | Alt-1. It can more likely utilize the RB set where LBT is successful.  As the DL and UL BWPs of a DL / UL BWP pair share the same center frequency in TDD band, there is some overlap. |
| Samsung | We understand that the motivation of Alt-1 is to utilize the RB set where DL type-1 channel access is successful. But we have two questions for Alt-1:   1. If gNB fails LBT on DL RB sets overlapping with UL RB sets, e.g. gNB fails LBT on both DL RB set 2 &3 but succeeds LBT on DL RB set 1&4 in the figure 1 below, gNB can not schedule a PUSCH by DCI 0\_0 in CSS? 2. If the boundary of one DL RB set and one UL RB set is not well-aligned, e.g. due to different guardband configuration for UL/DL, how to determine the UL RB set overlapping with DL RB set DCI 0\_0 received ? For example, if one DL RB set (partially) overlaps with two UL RB sets, which UL RB set for PUSCH transmission? |
| Fujitsu | Support Alt-1 |
| Qualcomm | Though Alt-1 is more flexible than Alt-2, it does not support the case that if legacy coreset is used (rb-Offset-r16 is UE capability), DCI 0\_0 may be across multiple RB sets (say a Rel.15 multi-cluster coreset is configured). In this case, there is ambiguity on which RB set this DCI 0\_0 is referring to. However, it might work if we use the RB set contains the first REG of the DCI 0\_0. May need some discussion. Or Alt-2 is simpler. |
| Intel | We support Alt-1 which benefits from the COT sharing from the gNB as the corresponding RB-set is always available. |

### 2.1.2 Issue #1-2: DCI 0\_0 in a USS

In the company responses for PUSCH scheduled by DCI 0\_0 in a USS, there is no clear majority between the variants of Alt-1 and the variants of Alt-2, except that within the variants of Alt-2 there is a clear preference for Alt-2a vs. Alt-2b. Hence, it is the FL’s proposal to limit discussion to the technical merits of the following three alternatives during this week.

1. The following is proposed for discussion this week, with down selection completed by 10/23. FL to draft TP(s) after down-selection.

* For PUSCH scheduled by DCI 0\_0 received in a USS when UL resource allocation Type 2 is configured, down-select to one out of the following three alternatives:
  + **Alt-1a**: FDRA field of DCI 0\_0 contains X bits only
    - PUSCH is allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received
  + **Alt-1b**: FDRA field of DCI 0\_0 contains X bits only
    - PUSCH is allocated to RB set 0 of the active UL BWP
  + **Alt-2**: FDRA field of DCI 0\_1 contains X + Y bits
    - Y is variable and determined by the size of the active UL BWP

**FL recommendation**: A solution is needed for this issue in order to complete the DCI 0\_0 design. Companies are encouraged to provide technical merits of their preferred alternative, also considering the situation for Issue #1-1. If no consensus can be achieved by 10/23, it is recommended to go with the majority view.

Please provide your company view on the above three alternatives:

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| --- | --- |
| **Company** | **View/Position** |
| Sharp | Alt 2. One of the target use case for DCI format 0\_0 monitored in USS should be for user data scheduling. Wideband scheduling with dynamic RB-set indication is a straight forward solution. |
| LG Electronics | Alt-1a  Also, regarding to this issue, the reference BWP to determine the size of X bit in FDRA field of DCI format 0\_0 needs to be clarified as below.  - For DCI format 0\_0 transmitted in USS, X bit size of FDRA field in the DCI format 0\_0 is determined based on the SCS of the active UL BWP as in legacy Rel-15 |
| Lenovo, Motorola Mobility | We support Alt-1b since it is simpler than Alt-1a and saves overhead than Alt-2.  Meanwhile, unified solution for DCI format 0\_0 in either CSS or USS is kept for Alt-1b. |
| NTT DOCOMO | Support Alt-1a to be consistent with issue #1-1. |
| ZTE | Alt 2. More flexible with no impact on the DCI size. |
| Huawei | Support Alt 2. If interlace is configured, it is most likely that the payload size of DCI 0\_0 is much smaller than DCI 1\_0, according to DCI size alignment step 1 in TS38.212 (zero padding bits are generated for the smaller one (DCI 0\_0) until the payload size equals that of the larger one (DCI 1\_0)).There is no need to save the Y bits |
| Nokia, NSB | Alt-1a to align with the CSS case |
| Panasonic | Alt-1a to align with the CSS case |
| Samsung | Alt-2.  It is obvious that Alt-1 and Alt-2 in issue #1-1 suffers either scheduling restriction, e.g. PUSCH can not be scheduled if gNB fails LBT on DL RB sets overlapping with UL RB sets by Alt-1(something like either type-2 UL LBT or no PUSCH transmission at all), or lower transmission opportunity, e.g. PUSCH can not take advantage of type-2 UL LBT if gNB fails DL LBT on the DL RB set overlaps with UL RB set 0 by Alt-2.  Adding Y bits in DCI 0\_0 in USS avoids the restrictions above and it does not increase DCI size.  And it is noted that such flexibility for DCI 0\_0 in USS is very important if gNB only configures DCI 0\_0 for a UE. |
| Fujitsu | Support Alt-1a |
| Qualcomm | Alt1-a is more efficient, but we see the same issue described in the CSS case. If we go with Alt-1a, need to discuss to come up with a fix. Or we can go with Alt-1b for simplicity. |
| Intel | Alt-1a to align with the CSS case and to make the operation simpler. |

## 2.2 Issue #2: Minimum Number of RBs Within an Interlace

**Description**:

In RAN1 AH 1901, the following agreement was reached on interlace design for the case of 20 MHz carrier bandwidth which states that the number of RBs within an interlace is N = 10 or 11.

Agreement:

For interlace transmission of at least PUSCH and PUCCH, the following PRB-based interlace design is supported for the case of 20 MHz carrier bandwidth:

a. 15 kHz SCS: M = 10 interlaces with N = 10 or 11 PRBs / interlace

b. 30 kHz SCS: M = 5 interlaces with N = 10 or 11 PRBs / interlace

Note: PRACH design to be considered separately, including multiplexing aspects with PUSCH and PUCCH

In RAN1#98, the following agreement was reached on interlace design for the case of arbitrary bandwidths which states that the number of PRBs in an interlace N scales with the carrier bandwidth. The case of 10 MHz carrier bandwidth where N could potentially be less than 10 was left as FFS.

Agreement:

The working assumption from RAN1 AH1901 is converted to an agreement with the following modifications:

* For a given SCS, the following PRB-based interlace design is supported ~~at least~~ for PUSCH and PUCCH:
  + Same spacing (M) between consecutive PRBs in an interlace for all interlaces regardless of carrier BW, i.e., the number of PRBs per interlace is dependent on the carrier bandwidth
  + Point A is the reference for the interlace definition
* For 15 kHz SCS, M = 10 interlaces and for 30 kHz SCS, M = 5 interlaces for all bandwidths
* ~~FFS: Interlace design for PUCCH for bandwidths greater than 20 MHz~~
* FFS: Whether and how partial interlace allocation is supported considering mechanisms specific to PUSCH and PUCCH
* FFS: PUCCH bandwidth
* FFS: Whether or how an interlace design for PUSCH and/or PUCCH is supported on 10 MHz according to the revised WID objective

But, in the same meeting, the following conclusion was reached for 10 MHz carrier bandwidth.

Conclusion:

For 10 MHz carrier bandwidth, enhancements to Rel-15 UL signals and channels are not necessary.

This resolves the FFS: if a serving cell is configured with 10 MHz bandwidth, interlaced transmission for PUCCH/PUSCH is not supported. In other words, the minimum number of RBs within an interlace N is 10. This restriction is not yet captured in RAN1 specifications.

**Affected Specification(s)**:

* 38.211 Section 4.4.4.6

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| **Company** | **View/Position** |
| Sharp | We are fine with the proposal. |
| LG Electronics | Support the proposal |
| Lenovo, Motorola Mobility | Ok with the proposal |
| NTT DOCOMO | OK with TP#1 |
| ZTE | Agree with the TP |
| Huawei | Agree with the TP |
| Nokia, NSB | Agree with the TP |
| Panasonic | Agree with the TP |
| Samsung | Agree with the TP |
| Fujitsu | Agree with the TP |
| Qualcomm | Agree with the TP |
| Intel | Agree with the TP |

------------------------------------- Text Proposal (TP#1) for 38.211, Section 4.4.4.6 --------------------------------

\*\*\* Unchanged text omitted \*\*\*

4.4.4.6 Interlaced resource blocks

Multiple interlaces of resource blocks are defined where interlace consists of common resource blocks , with being the number of interlaces given by Table 4.4.4.6-1. The relation between the interlaced resource block in bandwidth part and interlace and the common resource block is given by

where is the common resource block where bandwidth part starts relative to common resource block 0. When there is no risk for confusion the index may be dropped. The UE expects that the number of common resource blocks in an interlace contained within bandwidth part *i* is no less than 10.

**Table 4.4.4.6-1: The number of resource block interlaces.**

|  |  |
| --- | --- |
|  |  |
| 0 | 10 |
| 1 | 5 |

\*\*\* Unchanged text omitted \*\*\*

------------------------------------------------------ End Text Proposal -------------------------------------------------------

# References

1. R1-2001533 Maintainance on uplink signals and channels Huawei, HiSilicon
2. R1-2001651 Remaining issues on physical UL channel design in unlicensed spectrum vivo
3. R1-2001704 Remaining issues on the UL channels for NR-U ZTE, Sanechips
4. R1-2001758 Discussion on the remaining issues of UL signals and channels OPPO
5. R1-2001875 Remaining issues on UL signals and channels for NR-U Fujitsu
6. R1-2001903 Remaining issues on UL signals and channels for NR-U MediaTek Inc.
7. R1-2001934 Remaining issues of UL signals and channels for NR-U LG Electronics
8. R1-2001973 Remaining issues for UL signals and channels for NR-U Lenovo, Motorola Mobility
9. R1-2001986 UL signals and channels for NR-unlicensed Intel Corporation
10. R1-2002030 UL signals and channels Ericsson
11. R1-2002075 TP for SRS configuration CATT
12. R1-2002116 UL signals and channels for NR-U Samsung
13. R1-2002192 Remaining Issues on UL Signals and Channels for NR-U Nokia, Nokia Shanghai Bell
14. R1-2002246 UL signals and channels ETRI
15. R1-2002276 Remaining issues in UL signals and channels Spreadtrum Communications
16. R1-2002321 Remaining issues of UL signals and channels Apple
17. R1-2002365 TPs on uplink signals in NRU NEC
18. R1-2002382 Remaining issues on UL signals/channels for NR-U Sharp
19. R1-2002433 Remaining issues on UL signals and channels for NR-U NTT DOCOMO, INC.
20. R1-2002529 TP for UL signals and channels for NR-U Qualcomm Incorporated
21. R1-2002036, “Feature lead summary for Maintenance of UL Signals and Channels,” Moderator (Ericsson), RAN1#100bis-e, April, 2020.