3GPP TSG-RAN WG1 Meeting #100bis-e R1-20xxxxx

e-Meeting, 20th – 30th April, 2020

Agenda Item: 7.2.2.1.3

Source: Moderator (Ericsson)

Title: FL Summary for [100b-e-NR-unlic-NRU-ULSignalsChannels-01] Email discussion/approval

Document for: Discussion, Decision

# 1 Introduction

Based on the conclusion of the e-meeting preparation phase [21] and the vice-Chairman’s guidance, the following e-mail discussion has been kicked-off:

[100b-e-NR-unlic-NRU-ULSignalsChannels-01] Email discussion/approval on the following issues

by 4/23; if necessary, followed by endorsing the corresponding TPs by 4/29 – Steve (Ericsson)

* Finalize design for FDRA field of DCI 0\_0 for UL resource allocation Type 2
* Editorial correction on interlace configuration

The following topics are included in this email discussion

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| **Issue** | **Description** | **Tdoc References** | **Class** |
| 1 | FDRA field for DCI 0\_0 for UL resource allocation Type 2:   * Issue 1-1:   DCI 0\_0 in a CSS: Agree on rule for RB set allocation for PUSCH   * Isuee 1-2:   DCI 0\_0 in a USS: Agree on whether or not FDRA field includes Y bits for RB set allocation + rule for RB set allocation for PUSCH (if Y bits not included) or value of Y (if Y bits included)  TPs needed to 38.212 §7.3.1.1.1 and 38.214 §6.1.2.2.3 | R1-2002321: P1,P2  R1-2002030: P1,P2  R1-2001875: P1-P3  R1-2001533: P1  R1-2001934: P1-P4  R1-2001973: P2-P4  R1-2002433: P1  R1-2001758: P1  R1-2002116: P1  R1-2002382: P1-P3  R1-2002276: P1-P2  R1-2001704: P1-P2  R1-2001651: P1-P2 | Critical |
| 2 | Clarify that minimum number of resource blocks within an interlace contained in a BWP is 10 (Interlaced transmission not supported for 10 MHz SCell)  Simple TP needed to 38.211 §4.4.4.6 | R1-2002030: P6  R1-2001533: P2  R1-2001986: §2.2 | Editorial |

The following company views were captured in the e-meeting preparation phase [21]:

**Issue 1-1: Alternatives for RB set allocation for PUSCH scheduled by DCI 0\_0 in CSS:**

* Alt-1: PUSCH allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received
* Alt-2: PUSCH allocated to RB set 0 of the active UL BWP
* Alt-3: PUSCH allocated to all RB sets of the active UL BWP
* Alt-4a/b: PUSCH allocated to RB set(s) according to the following logic:
  + Alt-4a (ref: [4]):
    - If the active UL BWP does not include all of the RBs of the initial UL BWP or the active UL BWP has different SCS than the initial UL BWP, then
      * RB set 0 of the active UL BWP
    - Otherwise
      * RB set of the initial UL BWP
  + Alt-4b (ref: [18]):
    - If the active UL BWP includes all of the RBs of the initial UL BWP and the SCS/CP of the active UL BWP is the same as that of the initial UL BWP or the initial UL BWP is active
      * the initial UL BWP
    - Otherwise
      * All RB sets of the active UL BWP

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| **Company** | **View/Position** |
| Apple | Alt-1 |
| Ericsson | Alt-1 |
| Fujitsu | Alt-1 |
| LGE | Alt-1 |
| DOCOMO | Alt-1 |
| OPPO | Alt-4a |
| Samsung | Alt-3 |
| Sharp | Alt-4b |
| Spreadtrum | Alt-2  Please do not update this table. See new table in Section 2.1.1. |
| ZTE | Alt-1 |
| vivo | Alt-2 |
| Lenovo | Alt-2 |
| Qualcomm | Alt-2 |
| Nokia, NSB | Alt-1 |
| Huawei | Alt-1 |

**Issue 1-2: Alternatives for FDRA field of DCI 0\_0 in a USS:**

* Alt-1: FDRA field of DCI 0\_1 in a USS contains X bits only
  + Alt-1a: PUSCH allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received
  + Alt-1b: PUSCH allocated to RB set 0 of the active UL BWP
* Alt-2: FDRA field of DCI 0\_1 in a USS contains X + Y bits
  + Alt-2a: Y is variable and given by size of active UL BWP
  + Alt-2b: Y is fixed at [4] bits

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| **Company** | **View/Position** |
| Apple | Alt-2a |
| Ericsson | Alt-1a |
| Fujitsu | Alt-1a |
| Huawei | Alt-2a |
| LGE | FFS between Alt-1a and Alt-2a |
| Lenovo | Alt-1b |
| DOCOMO | Alt-1a |
| OPPO | Alt-2a |
| Samsung | Alt-2b  Please do not update this table. See new table in Section 2.1.2. |
| Sharp | Alt-2 |
| Spreadtrum | Alt-1b |
| ZTE | Alt-2 |
| vivo | Alt-2a |
| Qualcomm | Alt-1b |
| Nokia, NSB | Alt-1a |

# 2 Discussion

## 2.1 FDRA Field for DCI 0\_0

### 2.1.1 Issue #1-1: DCI 0\_0 in a CSS

Judging by company responses in the preparation phase, there is clear majority support for either Alt-1 and Alt-2 for PUSCH scheduled by DCI 0\_0 received in a CSS. It is the FL’s proposal to limit discussion to of these two alternatives during this week.

1. The following is proposed for discussion this week, with down selection completed by 10/23. FL to draft TPs after down-selection.

* For PUSCH scheduled by DCI 0\_0 received in a CSS when UL resource allocation Type 2 is configured, down-select to one out of the following two alternatives for the RB set allocation:
  + **Alt-1**: PUSCH is allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received
  + **Alt-2**: PUSCH is allocated to RB set 0 of the active UL BWP

One technical aspect that has not been addressed in contributions is that Alt-2 effectively introduces “cross RB Set” scheduling (unless DCI 0\_0 is also transmitted in RB Set 0). In other words, the gNB transmits DCI 0\_0 in an arbitrary RB set, but the PUSCH transmission is always in RB Set 0. If LBT is successful at the gNB in DL RB Set X, isn’t there a higher chance that LBT is successful at the UE in the UL RB Set that overlaps X? Recall that the goal of DCI 0\_0 is for robust behaviour.

**FL recommendation**: A solution is needed for this issue in order to complete the DCI 0\_0 design. Companies are encouraged to provide technical merits of their preferred alternative. If no consensus can be achieved by 10/23, it is recommended to go with the majority view. Note: Currently there are 8 companies supporting Alt-1 and 4 companies supporting Alt-2.

Please provide your company view on the above two alternatives:

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| **Company** | **View/Position** |
| Sharp | I have a question for both alternatives. When the size of uplink carrier is 80 MHz and the active UL BWP is 20 MHz, and intra-cell guard bands nor RB-sets provided, how is the UE scheduled a PUSCH? The RB-set in which the PUSCH is scheduled is the RB-set which corresponds to the uplink carrier?  *Moderator: Please see updated proposal below*  *[Sharp] The moderator’s proposal is accepted although my concern may not be fully cleared-up. One minor clarification proposal is, to set the second bullet to a sub-bullet of the first one. The sub-bullet is also for PUSCH scheduled by DCI 0\_0 received in a CSS when UL resource allocation Type 2 is configured. Is it right?* |
| LG Electronics | Alt-1  Also, regarding to this issue, the reference BWP to determine the size of X bit in FDRA field of DCI format 0\_0 needs to be clarified as below.  - For DCI format 0\_0 transmitted in CSS, X bit size of FDRA field in the DCI format 0\_0 is determined based on the SCS of the initial UL BWP as in legacy Rel-15  *Moderator: The intention of the updated proposal below is that PUSCH is transmitted in the active UL BWP, hence the X = 5/6 if the SCS of the active UL BWP is 30/15 kHz SCS. It does not seem necessary to define a reference BWP.* |
| Lenovo, Motorola Mobility | We support Alt-2 since it is simpler than Alt-1.  Comments to Alt-1: if the current active DL BWP has no any overlapping with current active UL BWP in frequency domain, how can it work?  *Moderator: Please see updated (merged) proposal below* |
| NTT DOCOMO | Support Alt-1. Agree with FL that Alt-1 has higher chance that LBT is successful in the UL RB set allocated to the PUSCH |
| ZTE | Support Alt.1 |
| Huawei | Basically support Alt-1, which is benefit for UE to share the COT from gNB. But we have similar concern as Sharp, if no intra-cell guardband is configured, there is only one RB set. Then “the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received” is not clear. Our suggestion is waiting for the conclusion in wideband discussion.  *Moderator: We need to make progress, and cannot keep bouncing back and forth between these two agenda items* |
| Nokia, NSB | Alt –  *Moderator: I assume Nokia supports Alt-1* |
| Panasonic | Alt-1. It can more likely utilize the RB set where LBT is successful.  As the DL and UL BWPs of a DL / UL BWP pair share the same center frequency in TDD band, there is some overlap. |
| Samsung | We understand that the motivation of Alt-1 is to utilize the RB set where DL type-1 channel access is successful. But we have two questions for Alt-1:   1. If gNB fails LBT on DL RB sets overlapping with UL RB sets, e.g. gNB fails LBT on both DL RB set 2 &3 but succeeds LBT on DL RB set 1&4 in the figure 1 below, gNB can not schedule a PUSCH by DCI 0\_0 in CSS? 2. If the boundary of one DL RB set and one UL RB set is not well-aligned, e.g. due to different guardband configuration for UL/DL, how to determine the UL RB set overlapping with DL RB set DCI 0\_0 received ? For example, if one DL RB set (partially) overlaps with two UL RB sets, which UL RB set for PUSCH transmission?     *Moderator: Please see updated (merged) proposal below to address point (1), i.e., the case when the intersection is NULL. Regarding (2), for most configurations if there is an overlap of a DL and and UL RB set, there will be a full overlap, and any slight mismatch at the edges due to slightly misaligned guard bands should not change what is meant by the word “intersection.” If you can think of a better word that conveys the idea of “full or almost full overlap” I am open to suggestions.* |
| Fujitsu | Support Alt-1 |
| Qualcomm | Though Alt-1 is more flexible than Alt-2, it does not support the case that if legacy coreset is used (rb-Offset-r16 is UE capability), DCI 0\_0 may be across multiple RB sets (say a Rel.15 multi-cluster coreset is configured). In this case, there is ambiguity on which RB set this DCI 0\_0 is referring to. However, it might work if we use the RB set contains the first REG of the DCI 0\_0. May need some discussion. Or Alt-2 is simpler.  *Moderator: How does legacy CORESET with RB sets and guard bands work? It seems to me that legacy CORESET applies to the case of a carrier with no guard bands.* |
| Intel | We support Alt-1 which benefits from the COT sharing from the gNB as the corresponding RB-set is always available. |
| OPPO | Alt-1 determines the FRDA based on DL BWP and UL BWP, which diverges from the design principle of NR. This solution is tightly bundled with TDD. Please remember that we should design a band agonistic solution, NR never has designed a solution like this. Moreover, for Alt-1 with operation in wideband, the CORESET should be confined within RB set, the RB set in which a UE detects DCI 0\_0 does not mean that the LBT failure in other RB set for uplink has lower chance to fail. On the contrary, Alt-1 highly probably would impose the UE to do multiple LBT on multiple RB sets, which leads to higher LBT failure probability, contradicting the goal of robust DCI 0\_0 behaviour. **In this sense we are against Alt-1**.  In spite of that our proposal was limited by FL, we still respect FL’s guidance. Although it is a pity as we thought that we were not supposed to eliminate any solution during last week preparation phase. Anyway between Alt-1 and Alt-2, we can support Alt-2. At least Alt-2 is band agonistic solution and it does not impose UE to do multiple LBT. |
| vivo | Alt 2. It is not frequent to schedule PUSCH using DCI 0\_0 in CSS, simple solution is preferred.  *[vivo] The first bullet of moderator’s proposal is ok for us considering the time budget, although our concern may not be fully cleared-up. For the second bullet, if we understand right, it is also for PUSCH scheduled by DCI 0\_0 received in a CSS when UL resource allocation Type 2 is configured. We think it should be discussed later till the related discussion for an UL carrier without intra-cell guard bands under WB agenda has some outcomes.* |
| Spreadtrum | Alt 2. As stated by Lenovo and Samsung, in order to guarantee PUSCH transmission, the RB set where DCI 0\_0 is located should overlap with UL BWP. If the bandwidth of UL BWP is smaller than that of DL BWP, the channel access probability of DCI 0\_0 will decrease. Therefore, from perspective of channel access, Alt 1 has no advantage over Alt 2. In addition, Alt 2 is simpler.  *Moderator: Please see updated (merged) proposal below addressing this issue.* |

#### 2.1.1.1 Summary of Discussion on Issue #1-1

The following is the summary of company positions on Alt-1 vs. Alt-2:

* Alt-1 Supported by:
  + LGE, DCM, ZTE, Huawei, Nokia, Panasonic, Fujitsu, Intel, Apple, Ericsson
* Alt-2 Supported by:
  + Lenovo, OPPO, vivo, Spreadtrum

Some of the concerns that were raised in the discussion are:

* For an UL BWP smaller than a DL BWP, the DL RB set in which the DCI 0\_0 is received may not overlap with any RB set in the UL BWP
* PUSCH allocation if no guard bands are configured for the UL carrier
* Legacy CORESET is used spanning multiple RB sets

The FL recommendation is to make a compromise proposal by merging Alt-1 and Alt-2 while trying to address some of the concerns raised by companies. While this may not satisfy all companies, a solution is needed otherwise the DCI 0\_0 design is incomplete.

1. Support the following:

* For PUSCH scheduled by DCI 0\_0 received in a CSS when UL resource allocation Type 2 is configured, PUSCH is allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received. If there is no intersection, PUSCH is allocated to RB Set 0 of the active UL BWP.
* If the active UL BWP corresponds to an UL carrier without intra-cell guard bands (single RB Set), PUSCH is allocated to all RBs of the indicated interlace(s) within the active UL BWP.

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| Lenovo, Motorola Mobility | This compromised proposal is generally fine with us.  In addition, for the first bullet, one condition may be added, like “the active UL BWP contains more than one RB set”, since the second bullet covers the case of single RB set.  Regarding the wording of “intersection”, does it imply the RB set where DCI format 0-0 is transmitted and the RB set for PUSCH transmission have same central frequency considering the both RB sets have 20MHz bandwidth? |
| OPPO | we think Alt-2 is a simple solution and we don't see any problem with Alt-2. Could moderator point me to the issue of Alt-2, please? |
| Qualcomm | To address the Moderators question in our previous comments, we believe legacy CORESET still works and can be configured when there is guard band. You just need to configure multiple cluster coreset as in Rel.15. In that case, there is ambiguity if DCI 0\_0 is mapped to more than one RB sets. A simple fix is to locate the RB set that contains the first REG of the detected DCI 0\_0. |
| LG Electronics | On the updated proposals, we have several comments/concerns as below.  - First of all, for NR U-band, TDD frame structure of Rel-15 NR would be baseline, so it is uncertain whether the configuration of the UL BWP without overlapping with the DL BWP is possible. Therefore, it is necessary to check.  - Next, on the reference BWP to determine the FDRA field size (i.e., X bit) of DCI 0\_0 in CSS, there was arguments in last meeting, but we don’t have explicit/clear agreement. Therefore, it is needed for clarification and common understanding.  - Finally, regarding to no guard-band issue, even in wideband agenda, there is no explicit agreement that the BWP configured with no guard-band is defined as single RB set. On top of that, according to the following agreement in RAN1#99, the RB set is defined to be corresponding to the LBT BW.  - Therefore, even if the UL BWP is configured with no guard band, it would be possible to operate with multiple RB sets based on a certain rule (for example, by assuming the guard band locations defined in RAN4 specification as RB set boundary, or divide the UL BWP equally).  - If the UL BWP configured with no guard band but containing multiple LBT BWs, is defined as single RB set, the gNB will be enforced to allocate the entire RBs of BWP for any PUSCH transmission, and then, the granularity of MCS and TBS for PUSCH scheduling becomes coarse, and the UL resource utilization efficiency will be degraded.  C:\Users\admin\Documents\반디카메라\Cap 2020-04-24 02-51-33-833.png |

#### 2.1.1.2 Further Summary of Discussion

Based on the above feedback and discussion on the reflector, we need further discussion on the case of an UL carrier without guardbands, as it affects the rule for how PUSCH should be allocated. Several companies suggested that we wait for further decisions in the wideband agenda item before making an agreement here which seems prudent. In the conclusion of the Wideband Operation (WB-01) email thread on 4/24, Seonwook will moderate a discussion on two different options for realizing a carrier without intra-cell guard bands during the early part of next week. Companies are encouraged to contribute to the discussion in WB-01 so hopefully that can be concluded. If so, this will help speed progress on PUCCH/PUSCH resource allocation in this agenda item.

Since the first part of the Proposal 2 seems stable, it seems we can agree on that. For the 2nd part of the proposal for an UL carrier without intra-cell guardbands, I have made that FFS.

1. Support the following:

* For PUSCH scheduled by DCI 0\_0 received in a CSS when UL resource allocation Type 2 is configured, PUSCH is allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received. If there is no intersection, PUSCH is allocated to RB Set 0 of the active UL BWP.
* FFS1: PUSCH allocation within the active UL BWP corresponding to an UL carrier without intra-cell guard bands
* FFS2: Whether or not the first bullet is modified to “…the active DL BWP in which the first REG of the received DCI 0\_0 is located,” in order to facilitate a CORESET not confined to a single RB set.

**FL Recommendation**

* Adopt Proposal 3
* FFS1 to be resolved based on discussion in WB-01 agenda item concluding early next week. Companies encouraged to provide their view in the WB-01 Email Thread.
* FFS2 has had limited discussion between two companies, but I don’t feel it is stable or accepted by all yet. Suggest further discussion until 4/27. Companies are encouraged to provide views.
* FL to draft TP for endorsement by 4/29

### 2.1.2 Issue #1-2: DCI 0\_0 in a USS

In the company responses for PUSCH scheduled by DCI 0\_0 in a USS, there is no clear majority between the variants of Alt-1 and the variants of Alt-2, except that within the variants of Alt-2 there is a clear preference for Alt-2a vs. Alt-2b. Hence, it is the FL’s proposal to limit discussion to the technical merits of the following three alternatives during this week.

1. The following is proposed for discussion this week, with down selection completed by 10/23. FL to draft TP(s) after down-selection.

* For PUSCH scheduled by DCI 0\_0 received in a USS when UL resource allocation Type 2 is configured, down-select to one out of the following three alternatives:
  + **Alt-1a**: FDRA field of DCI 0\_0 contains X bits only
    - PUSCH is allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received
  + **Alt-1b**: FDRA field of DCI 0\_0 contains X bits only
    - PUSCH is allocated to RB set 0 of the active UL BWP
  + **Alt-2**: FDRA field of DCI 0\_1 contains X + Y bits
    - Y is variable and determined by the size of the active UL BWP

**FL recommendation**: A solution is needed for this issue in order to complete the DCI 0\_0 design. Companies are encouraged to provide technical merits of their preferred alternative, also considering the situation for Issue #1-1. If no consensus can be achieved by 10/23, it is recommended to go with the majority view.

Please provide your company view on the above three alternatives:

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| **Company** | **View/Position** |
| Sharp | Alt 2. One of the target use case for DCI format 0\_0 monitored in USS should be for user data scheduling. Wideband scheduling with dynamic RB-set indication is a straight forward solution.  *[Sharp] The moderator’s proposal is accepted although we see that Alt.2 will have benefits over Alt.1. One minor clarification proposal is, to set the second bullet to a sub-bullet of the first one. The sub-bullet is also for PUSCH scheduled by DCI 0\_0 received in a USS when UL resource allocation Type 2 is configured. Is it right?* |
| LG Electronics | Alt-1a  Also, regarding to this issue, the reference BWP to determine the size of X bit in FDRA field of DCI format 0\_0 needs to be clarified as below.  - For DCI format 0\_0 transmitted in USS, X bit size of FDRA field in the DCI format 0\_0 is determined based on the SCS of the active UL BWP as in legacy Rel-15 |
| Lenovo, Motorola Mobility | We support Alt-1b since it is simpler than Alt-1a and saves overhead than Alt-2.  Meanwhile, unified solution for DCI format 0\_0 in either CSS or USS is kept for Alt-1b. |
| NTT DOCOMO | Support Alt-1a to be consistent with issue #1-1. |
| ZTE | Alt 2. More flexible with no impact on the DCI size. |
| Huawei | Support Alt 2. If interlace is configured, it is most likely that the payload size of DCI 0\_0 is much smaller than DCI 1\_0, according to DCI size alignment step 1 in TS38.212 (zero padding bits are generated for the smaller one (DCI 0\_0) until the payload size equals that of the larger one (DCI 1\_0)).There is no need to save the Y bits |
| Nokia, NSB | Alt-1a to align with the CSS case |
| Panasonic | Alt-1a to align with the CSS case |
| Samsung | Alt-2.  It is obvious that Alt-1 and Alt-2 in issue #1-1 suffers either scheduling restriction, e.g. PUSCH can not be scheduled if gNB fails LBT on DL RB sets overlapping with UL RB sets by Alt-1(something like either type-2 UL LBT or no PUSCH transmission at all), or lower transmission opportunity, e.g. PUSCH can not take advantage of type-2 UL LBT if gNB fails DL LBT on the DL RB set overlaps with UL RB set 0 by Alt-2.  Adding Y bits in DCI 0\_0 in USS avoids the restrictions above and it does not increase DCI size.  And it is noted that such flexibility for DCI 0\_0 in USS is very important if gNB only configures DCI 0\_0 for a UE. |
| Fujitsu | Support Alt-1a |
| Qualcomm | Alt1-a is more efficient, but we see the same issue described in the CSS case. If we go with Alt-1a, need to discuss to come up with a fix. Or we can go with Alt-1b for simplicity. |
| Intel | Alt-1a to align with the CSS case and to make the operation simpler. |
| OPPO | We support Alt-2  For Alt-1a, the drawback has been stated in section 2.1.1.  For Alt-2, we believe it follows the NR design baseline. In NR, when a UE is scheduled by DCI 0\_0 in USS, the whole active UL BWP can be flexibly scheduled. Following this baseline, all the RB sets should be able to be scheduled. Introducing Y bits and the value of Y depends on the active UL BWP should be the baseline, unless the opposing companies can point out the essential problems.  [OPPO] updating our comments:  The claimed benefit from Alt-1 is that if the gNB managed to send DCI 0\_0, the UE will have more chance to pass the LBT. We suspect how much in practice the UE can benefit from this, but assuming this is true, Alt-2 can perfectly indicates the intended RB set as well, because Alt-2 has better flexibility.  Moreover, Alt-1 suffers scheduling restriction, because as also pointed by Samsung, if the gNB fails the LBT in RB set 1 and RB set 2, it cannot schedule the UE. However Alt-2 can! i.e. the network can schedule the UE in whichever RB set passed LBT. Thus, the claimed advantage of Alt-1 is not an advantage w.r.t. Alt-2, but rather is a restriction.    Moreover, thanks to the fact that gNB receives the measurement reporting from UE during the time, the gNB might have better idea on which RB set is freer than the others. Using Alt-2, the gNB can schedule the UE in a freer RB set to increase the UE’s LBT success probability. This is a real benefit with Alt-2.  Furthermore, the Alt-2 has the same DCI overhead as Alt-1, because the DCI 0\_0 in USS has to padding to the same size as DCI 1\_0 in USS.  In summary, compared with Alt-1, the Alt-2 has no drawback only advantages. More importantly, due to the good flexibility and no penalty, this design principle was adopted in NR Rel.15 for reasons. |
| vivo | We support Alt-2  Agree with views of companies that support Alt-2. A UE can be configured to monitor DCI 0\_0 only for UL scheduling, Alt 1 is too restrictive for wideband case. No need to save Y bits considering the procedure for DCI size alignment.  *[vivo] The moderator’s proposal is not acceptable for us. Firstly, we don’t see the need to adopt unified solution with DCI 0\_0 in CSS and USS. Even in Rel-15, there are different designs for DCI in USS and CSS, such as determination of FDRA field bit-width, interpretations of FDRA field when there is no enough bits to indicate the whole resources in active UL BWP (PUSCH in active BWP scheduled by DCI 0\_0 in CSS vs. PUSCH in active BWP scheduled by DCI 0\_0 in USS, but FDRA is determined based on initial BWP for DCI 0\_0 in USS due to DCI size alignment). Secondly, Alt 2 can be considered as a unified solution for different DCI formats in USS, i.e., DCI 0\_0 in USS and DCI 0\_1 in USS. Thirdly, we don’t find any benefit of Alt 1 to adopt unified solution for DCI in CSS and USS. From technical perspective, Alt 2 is a baseline of NR design and is obviously better than Alt 1.* |
| Spreadtrum | Alt-1b. unified solution for USS and CSS is kept for Alt-1b |

#### 2.1.2.1 Summary of Discussion on Issue #1-2

The following is the summary of company positions on Alt-1 vs. Alt-2:

* Alt-1a Supported by:
  + LGE, DCM, Nokia, Panasonic, Fujitsu, Qualcomm, Intel, Ericsson
* Alt-1b Supported by:
  + Lenovo, Qualcomm, Spreadtrum,
* Alt-2 Supported by:
  + Sharp, ZTE, Huawei, Samsung, OPPO, vivo, Apple

The main arguments in support of the alternatives are:

* Alt-1a/b (X bits only):
  + Unified solution with DCI 0\_0 in CSS
* Alt-2 (X + Y bits)
  + Flexible scheduling

The FL recommendation is to merge Alt-1a and Alt-1b in the same way as for DCI 0\_0 in a CSS, and due to the larger support for signalling only X bits instead of X + Y it is recommended to go with this merged proposal. Again, while this may not satisfy all companies, a solution is needed, otherwise the DCI 0\_0 design is incomplete.

1. Support the following (identical proposal as for DCI 0\_0 in CSS)

* For PUSCH scheduled by DCI 0\_0 received in a USS when UL resource allocation Type 2 is configured, PUSCH is allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received. If there is no intersection, PUSCH is allocated to RB Set 0 of the active UL BWP.
* If the active UL BWP corresponds to an UL carrier without intra-cell guard bands (single RB Set), PUSCH is allocated to all RBs of the indicated interlace(s) within the active UL BWP.

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| --- | --- |
| Lenovo, Motorola Mobility | This compromised proposal is generally fine with us.  In addition, for the first bullet, one condition may be added, like “the active UL BWP contains more than one RB set”, since the second bullet covers the case of single RB set.  Regarding the wording of “intersection”, does it imply the RB set where DCI format 0-0 is transmitted and the RB set for PUSCH transmission have same central frequency considering the both RB sets have 20MHz bandwidth? |
| OPPO | There are 7 companies supporting Alt-2, however the proposed solution is Alt1a+Alt1b.  DCI 0\_0 scheduling in USS is supposed to be flexible in NR R15, now we are designing R16 and the proposal intends to remove this flexibility. I don't see any technical issue with Alt-2, which follows the baseline of NR.  [OPPO] updating our comments:  The claimed benefit from Alt-1 is that if the gNB managed to send DCI 0\_0, the UE will have more chance to pass the LBT. We suspect how much in practice the UE can benefit from this, but assuming this is true, Alt-2 can perfectly indicates the intended RB set as well, because Alt-2 has better flexibility.  Moreover, Alt-1 suffers scheduling restriction, because as also pointed by Samsung, if the gNB fails the LBT in RB set 1 and RB set 2, it cannot schedule the UE. However Alt-2 can! i.e. the network can schedule the UE in whichever RB set passed LBT. Thus, the claimed advantage of Alt-1 is not an advantage w.r.t. Alt-2, but rather is a restriction.    Moreover, thanks to the fact that gNB receives the measurement reporting from UE during the time, the gNB might have better idea on which RB set is freer than the others. Using Alt-2, the gNB can schedule the UE in a freer RB set to increase the UE’s LBT success probability. This is a real benefit with Alt-2.  Furthermore, the Alt-2 has the same DCI overhead as Alt-1, because the DCI 0\_0 in USS has to padding to the same size as DCI 1\_0 in USS.  In summary, compared with Alt-1, the Alt-2 has no drawback only advantages. More importantly, due to the good flexibility and no penalty, this design principle was adopted in NR Rel.15 for reasons. |
| HUAWEI | We found the main reason for supporting Alt-1 is adopting a unified solution for USS and CSS, however, the motivation is not convincing. Even in NR, the designs for DCI 0\_0 in USS and CSS are different. Furthermore, we have clarified that in DCI size alignment procedure, the size of DCI 0\_0 and DCI 1\_0 in USS should be aligned by generating padding bits for the smaller one. Saving the Y bits is meaningless, and will restrict the scheduling.  The proposal is not acceptable for us. |
| ZTE | Similar as OPPO, vivo and HW, we do not see any reason why the design for CSS and USS should be the same. Alt-2 has advantage in terms of flexibility and including the Y bits will not increase the DCI size. |
| Qualcomm | Prefer a common design between CSS and USS. Our proposed fix for CSS should apply here as well. |

#### 2.1.2.2 Further Summary of Discussion

For the FDRA field of DCI 0\_0 in a USS, there has been quite a lot of discussion, but no consensus. Proponents of Alt-2 have raised technical arguments regarding scheduling flexibility and similarity to Rel-15 principles. Proponents of Alt-1 prefer common PUSCH allocation scheme as for DCI 0\_0 in a CSS. The FL has not seen companies prepared to compromise, and proponents of Alt-2 have indicated objection to Alt-1

* Alt-1: FDRA field of DCI 0\_0 includes X bits only. PUSCH allocation follows same rule as for DCI 0\_0 in a CSS (Proposal 1-1)
  + Supported by: LTE, DCM, Nokia, Panasonic, Fujitsu, Intel, Ericsson, Lenovo, Spreadtrum, Qualcomm
* Alt-2: FDRA field of DCI 0\_0 includes Y bits to indicate the allocated RB Set(s) for PUSCH
  + Supported by: ZTE, Huawei, Samsung, OPPO, vivo, Apple, Sharp

**FL Recommendation**: Focus the remainder of this meeting to finalizing the DCI 0\_0 design for a CSS. Come back next meeting and finish the design for USS. The decision next meeting should be based on the pros/cons of Alt-1 vs. Alt-2 in terms of technical merits and spec impact.

## 2.2 Issue #2: Minimum Number of RBs Within an Interlace

**Description**:

In RAN1 AH 1901, the following agreement was reached on interlace design for the case of 20 MHz carrier bandwidth which states that the number of RBs within an interlace is N = 10 or 11.

Agreement:

For interlace transmission of at least PUSCH and PUCCH, the following PRB-based interlace design is supported for the case of 20 MHz carrier bandwidth:

a. 15 kHz SCS: M = 10 interlaces with N = 10 or 11 PRBs / interlace

b. 30 kHz SCS: M = 5 interlaces with N = 10 or 11 PRBs / interlace

Note: PRACH design to be considered separately, including multiplexing aspects with PUSCH and PUCCH

In RAN1#98, the following agreement was reached on interlace design for the case of arbitrary bandwidths which states that the number of PRBs in an interlace N scales with the carrier bandwidth. The case of 10 MHz carrier bandwidth where N could potentially be less than 10 was left as FFS.

Agreement:

The working assumption from RAN1 AH1901 is converted to an agreement with the following modifications:

* For a given SCS, the following PRB-based interlace design is supported ~~at least~~ for PUSCH and PUCCH:
  + Same spacing (M) between consecutive PRBs in an interlace for all interlaces regardless of carrier BW, i.e., the number of PRBs per interlace is dependent on the carrier bandwidth
  + Point A is the reference for the interlace definition
* For 15 kHz SCS, M = 10 interlaces and for 30 kHz SCS, M = 5 interlaces for all bandwidths
* ~~FFS: Interlace design for PUCCH for bandwidths greater than 20 MHz~~
* FFS: Whether and how partial interlace allocation is supported considering mechanisms specific to PUSCH and PUCCH
* FFS: PUCCH bandwidth
* FFS: Whether or how an interlace design for PUSCH and/or PUCCH is supported on 10 MHz according to the revised WID objective

But, in the same meeting, the following conclusion was reached for 10 MHz carrier bandwidth.

Conclusion:

For 10 MHz carrier bandwidth, enhancements to Rel-15 UL signals and channels are not necessary.

This resolves the FFS: if a serving cell is configured with 10 MHz bandwidth, interlaced transmission for PUCCH/PUSCH is not supported. In other words, the minimum number of RBs within an interlace N is 10. This restriction is not yet captured in RAN1 specifications.

**Affected Specification(s)**:

* 38.211 Section 4.4.4.6

|  |  |
| --- | --- |
| **Company** | **View/Position** |
| Sharp | We are fine with the proposal. |
| LG Electronics | Support the proposal |
| Lenovo, Motorola Mobility | Ok with the proposal |
| NTT DOCOMO | OK with TP#1 |
| ZTE | Agree with the TP |
| Huawei | Agree with the TP |
| Nokia, NSB | Agree with the TP |
| Panasonic | Agree with the TP |
| Samsung | Agree with the TP |
| Fujitsu | Agree with the TP |
| Qualcomm | Agree with the TP |
| Intel | Agree with the TP |
| vivo | Agree with the TP |
| Spreadtrum | Agree with the TP |

Reason for changes

To capture RAN1 agreements that number of interlaces in within BWP can not be less than 10

Summary of changes

Include sentence that number of interlaces within a BWP can not be less than 10

Specs/Sections impacted

38.211 Section 4.4.4.6

Consequences if not approved

Misalignment between gNB configuration and UE expectation

------------------------------------- Text Proposal (TP#1) for 38.211, Section 4.4.4.6 --------------------------------

\*\*\* Unchanged text omitted \*\*\*

4.4.4.6 Interlaced resource blocks

Multiple interlaces of resource blocks are defined where interlace consists of common resource blocks , with being the number of interlaces given by Table 4.4.4.6-1. The relation between the interlaced resource block in bandwidth part and interlace and the common resource block is given by

where is the common resource block where bandwidth part starts relative to common resource block 0. When there is no risk for confusion the index may be dropped. The UE expects that the number of common resource blocks in an interlace contained within bandwidth part *i* is no less than 10.

**Table 4.4.4.6-1: The number of resource block interlaces.**

|  |  |
| --- | --- |
|  |  |
| 0 | 10 |
| 1 | 5 |

\*\*\* Unchanged text omitted \*\*\*

------------------------------------------------------ End Text Proposal -------------------------------------------------------

### 2.2.1 Summary of Discussion on Issue #2

There appears to be consensus to support TP#1. Therefore, the following is the FL recommendation

1. Support TP#1 for 38.211 Section 4.4.4.6

# 3 Conclusion After First Deadline

According to the Vice-Chairman’s guidance, the following was agreed after the first deadline:

Agreement:

* For PUSCH scheduled by DCI 0\_0 received in a CSS when UL resource allocation Type 2 is configured, PUSCH is allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which DCI 0\_0 is received. If there is no intersection, PUSCH is allocated to RB Set 0 of the active UL BWP.
* FFS1: PUSCH allocation within the active UL BWP corresponding to an UL carrier without intra-cell guard bands
* FFS2: Whether or not the first bullet is modified to “…the active DL BWP in which the first REG of the received DCI 0\_0 is located,” in order to facilitate a CORESET not confined to a single RB set.

FFS points in agreement for DCI 0\_0 in a CSS and corresponding TP for the entire agreement to be finalized by 4/29

Agreement:

Adopt TP#1 in Section 2.2 of [Draft R1-20xxxxx 100b-e-NR-unlic-NRU-ULSignalsChannels-01\_v28 – Moderator] for TS 38.211, Section 4.4.4.6

Agreement:

* For PUSCH scheduled by DCI 0\_0 received in a USS when UL resource allocation Type 2 is configured, PUSCH is allocated to the RB set(s) of the active UL bandwidth part indicated by the Y bits in the FDRA field of DCI 0\_0.

## 3.1 TP #2,3

Reason for changes

Capture the RAN1 agreement that DCI 0\_0 in a UE-specific search space include Y bits to indicate the RB set allocation.

Capture the RAN1 agreement for the PUSCH allocation rule for DCI 0\_0 in a common search space

Summary of changes

Modify description of FDRA field in DCI 0\_0 in 38.212 to capture RAN1 agreements

Modify corresponding procedure text in 38.214 to capture RAN1 agreements

Specs/Sections impacted

38.212 Section 7.3.1.1.1

38.214 Section 6.1.2.2.3

Consequences if not approved

PUSCH cannot be scheduled by DCI 0\_0

------------------------------------ Text Proposal (TP#2) for 38.212, Section 7.3.1.1.1 ------------------------------

\*\*\* Unchanged text omitted \*\*\*

7.3.1.1.1 Format 0\_0

DCI format 0\_0 is used for the scheduling of PUSCH in one cell.

The following information is transmitted by means of the DCI format 0\_0 with CRC scrambled by C-RNTI or CS-RNTI or MCS-C-RNTI:

\*\*\* Unchanged text omitted \*\*\*

- if any of the higher layer parameters *useInterlacePUSCH-Common* and *userInterlacePUSCH-Dedicated* is configured

- ~~[5 or~~ 5+Y~~]~~ bits provide the frequency domain resource allocation according to Clause 6.1.2.2.3 of [6, TS 38.214] if the subcarrier spacing for the active UL bandwidth part is 30 kHz and the DCI format 0\_0 is monitored in a UE-specific search space. If the DCI 0\_0 is monitored in a common search space Y = 0.

- ~~[6 or~~ 6+Y~~]~~ bits provide the frequency domain resource allocation according to Clause 6.1.2.2.3 of [6, TS 38.214] if the subcarrier spacing for the active UL bandwidth part is 15 kHz and the DCI format 0\_0 is monitored in a UE-specific search space. If the DCI 0\_0 is monitored in a common search space Y = 0.

\*\*\* Unchanged text omitted \*\*\*

------------------------------------------------------- End Text Proposal ------------------------------------------------------

----------------------------------- Text Proposal (TP#3) for 38.214, Section 6.1.2.2.3 -------------------------------

\*\*\* Unchanged text omitted \*\*\*

6.1.2.2.3 Uplink resource allocation type 2

In uplink resource allocation of type 2, the resource block assignment information defined in [5, TS 38.212] indicates to a UE a set of up to *M* interlace indices, and for DCI 0\_0 monitored in a UE-specific search space and DCI 0\_1, a set of up to contiguous RB sets, where *M* and interlace indexing are defined in Clause 4.4.4.6 in [4, TS 38.211]. For DCI 0\_0 monitored in a UE-specific search space and DCI 0\_1, ~~T~~the UE shall determine the resource allocation in frequency domain as an intersection of the resource blocks of the indicated interlaces and the indicated set of RB sets and intra-cell guard bands defined in Clause 7 between the indicated RB sets, if any. For DCI 0\_0 monitored in a common search space, the UE shall determine the resource allocation in the frequency domain as an intersection of the resource blocks of the indicated interlaces and a single uplink RB set of the active UL BWP. The uplink RB set is the one that intersects with the downlink RB set of the active downlink BWP in which the UE detects the DCI 0\_0. If there is no intersection, the uplink RB set is RB set 0 in the active uplink BWP.

For µ=0, the X MSBs of the resource block assignment information indicates to a UE a set of allocated interlace indices , where the indication consists of a resource indication value (*RIV*). For , the resource indication value corresponds to the starting interlace index *m0* and the number of contiguous interlace indices (). The resource indication value is defined by:

if then

else

For , the resource indication value corresponds to the starting interlace index *m0* and the set of values  according to Table 6.1.2.2.3-1.

**Table 6.1.2.2.3-1: *m0* and  for .**

|  |  |  |
| --- | --- | --- |
|  | ***m0*** |  |
| 0 | 0 | {0, 5} |
| 1 | 0 | {0, 1, 5, 6} |
| 2 | 1 | {0, 5} |
| 3 | 1 | {0, 1, 2, 3, 5, 6, 7, 8} |
| 4 | 2 | {0, 5} |
| 5 | 2 | {0, 1, 2, 5, 6, 7} |
| 6 | 3 | {0, 5} |
| 7 | 4 | {0, 5} |

For µ=1, the X MSBs of the resource block assignment information comprise a bitmap indicating the interlaces that are allocated to the scheduled UE. The bitmap is of size *M* bits with one bitmap bit per interlace such that each interlace is addressable, where *M* and interlace indexing is defined in Clause 4.4.4.6 in [4, TS 38.211]. The order of interlace bitmap is such that interlace 0 to interlace are mapped from MSB to LSB of the bitmap. An interlace is allocated to the UE if the corresponding bit value in the bitmap is 1; otherwise the interlace is not allocated to the UE.

For DCI 0\_0 monitored in a UE-specific search space and DCI 0\_1 ~~F~~for both µ=0 and µ=1, the the resource block assignment information indicate to a UE a set of contiguously allocated RB sets for PUSCH scheduled by DCI 0\_1 and Type 1 and Type 2 configured grant. The resource allocation field consists of a resource indication value (*RIVRBset*). For , the resource indication value corresponds to the starting RB set () and the number of contiguous RB sets . The resource indication value is defined by;

\*\*\* Unchanged text omitted \*\*\*

------------------------------------------------------ End Text Proposal -------------------------------------------------------

Regarding FFS1, I believe the agreement that was made in Wideband Operation email thread #1 means that the PUSCH resource allocation works for a carrier configured both with and without intra-cell guard bands. Hence, there is no need to differentiate now. However, if further agreements on configuring a carrier without guardbands necessitate any changes, we can address those in the next meeting.

Regarding FFS2, I have not captured it in the TPs yet. There has been some discussion between at least two companies, but I would like to hear additional views. If there is not consensus in this meeting, we can revisit the issue next meeting and develop TPs if needed.

In Email Thread #2, LGE has provided an alternative PUSCH allocation rule for PUSCH scheduled by a RAR UL grant (Alt-3), and suggests that the same rule should apply to PUSCH scheduled by DCI 0\_0 addressed to TC\_RNTI. Please see the FL summary for that email thread for the rationale. In summary, the following is the proposed PUSCH allocation rule:

LGE Proposal:

* When UL resource allocation Type 2 is configured, PUSCH scheduled by DCI 0\_0 with CRC scrambled by TC-RNTI is allocated as follows:
  + If the active UL BWP fully overlaps the initial UL BWP, PUSCH is allocated to the initial UL BWP
  + Otherwise, PUSCH is allocated to the RB set of the active UL BWP that intersects the RB set of the active DL BWP in which the DCI 0\_0 is received. If there is no intersection, PUSCH is allocated to RB Set 0 of the active UL BWP

If this rule is adopted, then an update to TP#3 would be needed to handle the case of DCI 0\_0 scrambled by TC-RNTI. I suggest that if we cannot achieve consensus on the this in this meeting that we still adopt TP#2,3. This does not preclude further discussing this issue next meeting and develop TPs to handle any new agreement at that time.

**Q1: Do you agree with the above TPs. If not, please provide suggestions on how to modify.**

**Q2: What is your view on FFS2**

**Q3: What is your view on the LGE proposal for the case of DCI 0\_0 addressed to TC-RNTI**

|  |  |
| --- | --- |
| **Company** | **View/Position** |
|  |  |
|  |  |
|  |  |
|  |  |

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