3GPP TSG RAN WG1 #100bis R1-200xxxx

e-Meeting, April 20th – 30th, 2020

**Agenda item: 7.2.10.6**

**Source: Moderator (Nokia)**

**Title: Discussion summary on cross-carrier scheduling with different numerology**

**Document for: Discussion and Decision**

# 1 Introduction

This document is used to collect companies views for the issues identified for AI 7.2.10.6 email discussion thread:

[100b-e-NR- LTE\_NR\_DC\_CA-X-CC scheduling-01] Email approval the TPs based on the following:

* Issue#1 of R1-R2002613
* Spec-improvement #1 of R1-R2002613
* TP of Proposal#4 of R1-2001692
* TP of Proposal#2 of R1-2002561

till 4/23 (Nokia, Karri)

# 2 Companies’ views on discussion topics

## 2.1 Issue#1 of R1-R2002613

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| **Description** | **Source** |
| Cross-carrier release of the SPS PDSCH – HARQ-ACK resource and type-1 codebook determination | ZTE, vivo, MTek, Intel CATT,Huawei |

[R1-2001622, ZTE]

* The codebook is associated with the SPS PDSCH carrier.
* The codebook is associated with the last slot overlapping with the PDCCH providing SPS release.

[R1-2001692, vivo]

* Cross-carrier SPS release with same SCS: The single carrier SPS release behavior is used
  + Specifically, the HARQ-ACK resource is determined based on the last PUCCH slot overlapping with the SPS PDCCH release, while the bit location of the SPS release in type-1 codebook is determined by the SLIV of the SPS PDSCH.
* Cross-carrier SPS release with different SCS:
  + the HARQ-ACK resource is determined based on the last PUCCH slot overlapping with the SPS PDCCH release (i.e., same as SPS release in single carrier case).
  + the HARQ-ACK bit location of the SPS release in type-1 codebook is determined by the SLIV of the last slot of SPS PDSCH overlapping with the SPS PDCCH release.

[R1-2001837, MediaTek]

* The codebook is associated with the SPS PDSCH carrier.
* The last PDSCH slot that overlaps with the end of last symbol of PDCCH slot containing the SPS PDSCH release is used to determine the location of the HARQ-ACK for SPS PDSCH release in HARQ-ACK Type-1 codebook when PDSCH and PDCCH are with different numerologies.
* The last PDSCH slot that overlaps with the end of last symbol of PDCCH slot containing the SPS PDSCH release is the reference slot used to determine PUCCH Tx slot for SPS PDSCH release HARQ-ACK reporting in HARQ-ACK Type-1 codebook when PDSCH, PDCCH and PUCCH are with different numerologies.

[R1-2002014, Intel]

* The last PDSCH slot overlapping with the SPS PDSCH release is used to derive a HARQ-ACK occasion in Type1 HARQ-ACK codebook.
* A HARQ-ACK occasion for SPS PDSCH release is derived corresponding to the SLIV of SPS PDSCH in the SPS PDSCH slot.
* Assuming X>1 DL DCIs scheduling unicast PDSCHs per scheduled cell can be transmitted in a PDCCH MO, C-DAI is used as a third dimension of HARQ-ACK bits ordering in Type2 HARQ-ACK CB.

[R1-2002067, CATT]

* For cross-carrier SPS release, if the HARQ-ACK generation of SPS release is based on the SPS PDSCH carrier, endorse the above text proposal#1.
* For cross-carrier SPS release, if the HARQ-ACK generation of SPS release is based on the SPS release carrier, endorse the above text proposal#2.

[R1-2002580, Huawei]

* A location in the Type-1 HARQ-ACK codebook for HARQ-ACK information
  + corresponding to a single SPS PDSCH release is same as for a corresponding SPS PDSCH reception in the last slot that overlaps with the PDCCH carrying the SPS PDSCH release.
  + corresponding to multiple SPS PDSCH releases by a single DCI format is same as for a corresponding SPS PDSCH reception with the lowest SPS configuration index among the multiple SPS PDSCH releases in the last slot that overlaps with the PDCCH carrying the SPS PDSCH release.

**Summary of alternatives:**

Type-1 HARQ-ACK Codebook for cross-carrier SPS release association

* Alt1: The codebook is associated with the last slot overlapping with the PDCCH providing SPS release.
  + ZTE, Intel, Huawei
* Alt2: The codebook is associated with the last slot overlapping with the slot containing the PDCCH providing SPS release.
  + MTek
* Alt3: the HARQ-ACK resource is determined based on the last PUCCH slot overlapping with the SPS PDCCH release
  + vivo

Type-1 HARQ-ACK bit-location in the codebook bit location:

* The bit location of the SPS release in type-1 codebook is determined by the SLIV of the SPS PDSCH.
  + vivo, Intel

**FL proposal:**

* Type-1 HARQ-ACK Codebook for cross-carrier SPS release association: The codebook is associated with the last slot overlapping with the PDCCH providing SPS release.
* The bit location of the SPS release in type-1 codebook is determined by the SLIV of the SPS PDSCH.

**Companies’ comments:**

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| **Company** | **Comment** |
| ZTE | We support the FL proposal.  Some clarifications from our side.  1. The “ bit location determination“ and “ PUCCH slot determination“ of HARQ-ACK of SPS release are two different issues. We are addressing the first issue here.  The first issue (i.e., bit location determination) is addressing where to put the bit of HARQ-ACK of SPS release within one codebook, e.g., associating with which PDSCH slot and associating with which SLIV.  The second issue (i.e., PUCCH slot determination) is address which PUCCH slot to transmit the HARQ-ACK of SPS release. Seems no need to update the PUCCH slot determination of HARQ-ACK of SPS release. Reusing the currect Rel-15 spec (copied below) should suffice.  *K=0 corresponds to the last slot of the PUCCH transmission that overlaps with the PDSCH reception or with the PDCCH reception in case of SPS PDSCH release.*  2. As we analyzed in R1-2001622, the FL proposal is backward compatible with Rel-15 description. |
| Samsung | No need for the proposal. Current specifications are sufficient.  The first part of the proposal is captured by Rel-15 timeline descriptions for HARQ-ACK generation for SPS PDSCH release. The second part of the proposal is also Rel-15 operation. |
| MTK | We support the FL proposal with one suggested modification:  Modify  “The codebook is associated with the last slot overlapping with the PDCCH providin SPS release“ to  “The codebook is associated with the last slot overlapping with the PDCCH **slot** providin SPS release“  The reason for this change is that, to our understanding, the above two descriptions seem to map to two different PDSCH slot if the PDCCH symbols are located in the beginning of a slot as illustrated in the figure below: |
| vivo | Basically, we are fine with the FL proposals, with the following modifications:   1. The first sub-bullet can be agreed without any spec changes (i.e., simply a conclusion to confirm RAN1’s understanding). 2. The second sub-bullet is applied for cross-carrier scheduling with different numerologies. Spec changes are expected because in this case more than one SPS PDSCH slots overlap with the PUCCH slot, which is different from that in Rel-15. |
| Intel | We are OK wiht FL proposal. Some clarifications for better alignment. As ZTE commented, there are two issues to form Type1 HARQ-ACK CB.   * Derive a PDSCH slot and a SLIV which is used to derive a HARQ-ACK position in the slot * Derive the PUCCH slot k=0, then the PUCCH slot k=K1 for HARQ-ACK transmisison   Our understanding on defining k=0 is Fig B, i.e. derive a PDSCH slot (overlap with PDCCH of SPS release), then derive a PUCCH slot k=0 by the SLIV of SPS PDSCH (last PUCCH slot overlap with the SLIV). The pseudo code for Type1 HARQ-ACK CB has a rule to valid K1 values. In this sense, it is better to define k=0 based on SLIV of SPS PDSCH, which guarantee we could find a HARQ-ACK occasion for SPS release. |
| CATT | As we discussed in the last meeting, the major issue is how to generate HARQ-ACK bits for SPS release with cross-carrier scheduling, i.e. based on SPS release carrier or based on SPS PDSCH release.  For the current wording of the proposal, it is confusing to me as it doesn’t seem to reflect the spirit of previous discussion. As pointed out by Aris, the two bullets are exactly same as the current specification.  As mentioned by companies, there are two steps to determine a HARQ-ACK bit location in a type1-codebook:  Step1: find the slot which is covered by the feedback window based on K1 and PUCCH slot.  Step2: determine the SLIV used to generate HARQ-ACK bit  Hence we propose to update the proposal as below:   * Type-1 HARQ-ACK Codebook for cross-carrier SPS release association: The bit location of the SPS release is determined by the last slot of PUCCH transmission that overlaps with the PDCCH providing SPS release on the SPS SDSCH CC and the SLIV of the SPS PDSCH   Here I assume the intention of the proposal is to generate the HARQ-ACK for SPS release based on SPS PDSCH release with cross carrier scheduling. Although our preference is to generate the HARQ-ACK for SPS release based on SPS release carrier and identify some issues need to be fixed for the other one, we can go with majority views for sake of progress. |

## 2.2 Spec improvement #1 of R1-R2002613

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| **Description** | **Source** |
| TP for subclause 5.5, 38.214 for specification improvement  < unchanged text omitted >  This clause applies only if the PDCCH carrying the scheduling DCI is received on one carrier with one OFDM subcarrier spacing (µPDCCH), and the PDSCH scheduled to be received by the DCI is on another carrier with another OFDM subcarrier spacing (µPDSCH).  If the µPDCCH < µPDSCH, the UE is expected to receive the scheduled PDSCH, if the first symbol in the PDSCH allocation, including the DM-RS, as defined by the slot offset *K0* and the start and length indicator *SLIV* of the scheduling DCI starts no earlier than the first symbol of the slot allocated for the PDSCH ~~PDSCH slot~~ starting at least *Npdsch* PDCCH symbols after the end of the PDCCH scheduling the PDSCH, not taking into account the effect of receive timing difference between the scheduling cell and the scheduled cell.  < unchanged text omitted > | R1-2002423  (Ericsson) |

**FL proposal:** Adopt the TP above

**Companies’ comments:**

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| **Company** | **Comment** |
| ZTE | We are fine with the above update. |
| Samsung | OK with the proposal but the text can be imporved – e.g. <<slot allocated for the PDSCH>> 🡪 <<slot of the PDSCH reception>> |
| MTK | We are fine to adopt this proposal |
| vivo | We are OK with this changes. |
| Intel | We are fine to adopt this proposal |
| CATT | We are fine with the proposal |

## 2.3 TP of proposal #4 of R1-R2001692

Proposal 4 [R1-2001692]: Accept the proposed TP to clarify the additional timing delay d for cross carrier scheduling.

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| If the PDCCH carrying the scheduling DCI is received on one component carrier, and the PDSCH scheduled by that DCI is on another component carrier and the UE is configured with [*~~enabledDefaultBeamForCCS~~ enableDefaultBeamForCSS*]:  - The *timeDurationForQCL* is determined based on the subcarrier spacing of the scheduled PDSCH. If µPDCCH < µPDSCH an additional timing delay is added to the *timeDurationForQCL*, where *d* is defined in 5.2.1.5.1a-1, otherwise *d* is zero;  - For both the cases, when the offset between the reception of the DL DCI and the corresponding PDSCH is less than the threshold *timeDurationForQCL,* and when the DL DCI does not have the TCI field present, the UE obtains its QCL assumption for the scheduled PDSCH from the activated TCI state with the lowest ID applicable to PDSCH in the active BWP of the scheduled cell. |

**FL proposal:** Adopt the TP above

**Companies’ comments:**

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| --- | --- |
| **Company** | **Comment** |
| ZTE | We are fine with the above update. |
| Samsung | OK with the proposal |
| MTK | We are fine to adopt this proposal |
| vivo | We are supportive to the changes (of course ☺). |
| Intel | We are fine to adopt this proposal |
| CATT | We are fine with the proposal |

## 2.4 TP of proposal #2 of R1-R2002561

**Proposal 2 [R1-2002561]:** Update specification text to include cross-carrier scheduling with different SCS in the description of PDCCH limits for secondary cells. Adopt the corresponding text proposal in Section 10.1 in TS 38.213.

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| 10.1 UE procedure for determining physical downlink control channel assignment >>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>> unchanged text omitted <<<<<<<<<<<<<<<<<<<<<<<  For same cell scheduling or for cross-carrier scheduling, a UE does not expect a number of PDCCH candidates, and a number of corresponding non-overlapped CCEs per slot on a secondary cell to be larger than the corresponding numbers that the UE is capable of monitoring on the secondary cell per slot.  >>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>> unchanged text omitted <<<<<<<<<<<<<<<<<<<<<<< |

**FL proposal:** Adopt the TP above

**Companies’ comments:**

|  |  |
| --- | --- |
| **Company** | **Comment** |
| ZTE | We are fine with the above update. |
| Samsung | OK with the proposal. |
| MTK | We are fine to adopt this proposal |
| vivo | We are OK with this change. |
| Intel | We are fine to adopt this proposal |
| CATT | We are fine with the proposal |

# 3 Conclusion

To be written

# References

1. R1-2001622 Remaining Issues on Cross-carrier Scheduling with Mixed Numerologies, ZTE
2. R1-2001692 Remaining issues on cross-carrier scheduling with mix numerologies, vivo
3. R1-2001837 Remaining issues on X-carrier scheduling with different SCS, MediaTek Inc.
4. R1-2001942 Remaining issue on cross-carrier scheduling with different numerology, LG Electronics
5. R1-2002014 Remaining issues on cross-carrier scheduling with different numerology, Intel Corporation
6. R1-2002067 Discussion on HARQ-ACK feedback for SPS PDSCH release with cross-carrier scheduling, CATT
7. R1-2002423 Remaining issues for cross-carrier scheduling with different numerologies, Ericsson
8. R1-2002580 Remaining issues on cross-carrier scheduling with different numerology, Huawei, HiSilicon
9. R1-2002613 FL summary on cross-carrier scheduling with different numerology Moderator (Nokia)
10. R1-2002614 FL summary #2 on cross-carrier scheduling with different numerology Moderator (Nokia)