TSG-RAN Working Group1 meeting #8
New York, USA, 12 – 15 October 1999

TSGR1#8(99)F47

Agenda Item:

Source: **Nokia**

Title: **Corrections to TS 25.212**

Document for: **Decision**

Editorial changes for TS 25.212 are presented in this document.

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

[1] 3GPP RAN TS 25.201: “Physical layer – General Description”

[2] 3GPP RAN TS 25.211: “Transport channels and physical channels (FDD)”

[3] 3GPP RAN TS 25.213: “Spreading and modulation (FDD)”

[4] 3GPP RAN TS 25.214: “Physical layer procedures (FDD)”

[5] 3GPP RAN TS 25.221: “Transport channels and physical channels (TDD)”

[6] 3GPP RAN TS 25.222: “Multiplexing and channel coding (TDD)”

[7] 3GPP RAN TS 25.223: “Spreading and modulation (TDD)”

[8] 3GPP RAN TS 25.224: “Physical layer procedures (TDD)”

[9] 3GPP RAN TS 25.231: “Measurements”

[10] 3GPP RAN TS 25.302: "Services provided by the physical layer"

4.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

<ACRONYM> <Explanation>

ACS Add, Compare, Select
ARQ Automatic Repeat Request
BCH Broadcast Channel
BER Bit Error Rate
BLER Block Error Rate
BS Base Station
CCPCH Common Control Physical Channel
CCTrCH Coded Composite Transport Channel
CRC Cyclic Redundancy Code
DCH Dedicated Channel
DL Downlink (Forward link)
DPCH Dedicated Physical Channel
DPCCH Dedicated Physical Control Channel
DPDCH Dedicated Physical Data Channel
DS-CDMA Direct-Sequence Code Division Multiple Access
DSCH Downlink Shared Channel
DTX Discontinuous Transmission
FACH Forward Access Channel
FDD Frequency Division Duplex
FER Frame Error Rate
GF Galois Field
MAC Medium Access Control
Mcps Mega Chip Per Second
MS Mobile Station
OVSF Orthogonal Variable Spreading Factor (codes)
PCCC Parallel Concatenated Convolutional Code
PCH Paging Channel
PRACH Physical Random Access Channel
PhCH Physical Channel
QoS Quality of Service

RACH	Random Access Channel
RSC	Recursive Systematic Coder
RX	Receive
SCH	Synchronisation Channel
SF	Spreading Factor
SFN	System Frame Number
SIR	Signal-to-Interference Ratio
SNR	Signal to Noise Ratio
TF	Transport Format
TFC	Transport Format Combination
TFCI	Transport Format Combination Indicator
TPC	Transmit Power Control
TrCH	Transport Channel
TTI	Transmission Time Interval
TX	Transmit
UL	Uplink (Reverse link)

Table 1: Error Correction Coding Parameters

Transport channel type	Coding scheme	Coding rate
BCH	Convolutional code	1/2
PCH		
FACH		
RACH		
CPCH		1/3, 1/2 ~~or no coding~~
DCH		
CPCH	Turbo Code	1/3 ~~or no coding~~
DCH		
CPCH	No coding	
DCH		

4.2.3.2.1 Turbo coder

The initial value of the shift registers of the PCCC encoder shall be all zeros.

The output of the PCCC encoder is punctured to produce coded bits corresponding to the desired code rate ~~1/3~~. For rate 1/3, none of the systematic or parity bits are punctured, and the output sequence is X(0), Y(0), Y'(0), X(1), Y(1), Y'(1), etc.

4.2.3.2.3 Turbo code internal interleaver

Figure depicts the overall 8 state PCCC Turbo coding scheme including Turbo code internal interleaver. The Turbo code internal interleaver consists of mother interleaver generation and pruning. For arbitrary given block length K, one mother interleaver is selected from the 134 mother interleavers set. The generation scheme of mother interleaver is described in section 4.2.3.2.3.1. After the mother interleaver generation, *l*-bits are pruned in order to adjust the mother interleaver to the block length K. Tail bits T_1 and T_2 are added for constituent encoders RSC1 and RSC2, respectively. The definition of *l* is shown in section 4.2.3.2.3.2.

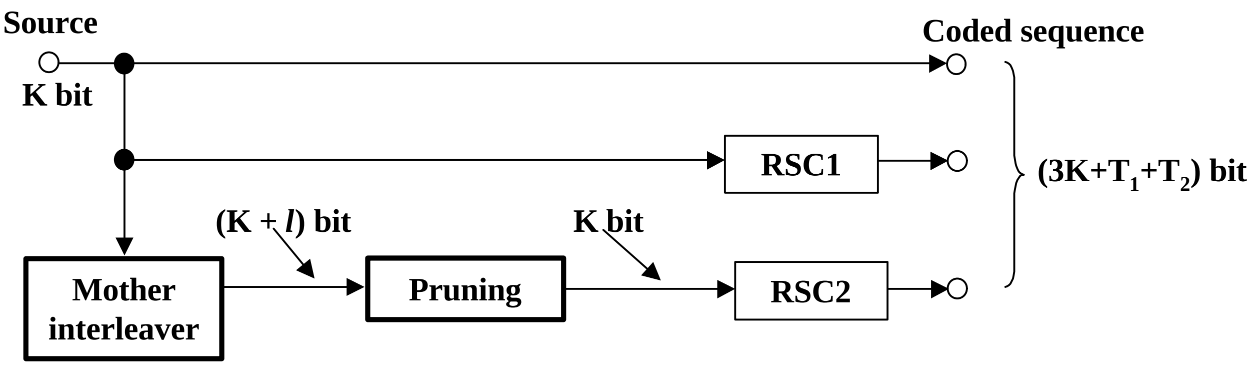

Figure 5: Overall 8 State PCCC Turbo Coding

First Stage:

(1) Determine the number of rows~~a row number~~ R such that

R=10 (K = 481 to 530 bits; Case-1)

R=20 (K = any other block length except 481 to 530 bits; Case-2)

(2) Determine the number of columns~~a column number~~ C such that

Case-1; C = *p = 53*

Csae-2;

(i) find minimum prime *p* such that,

0 =< (*p*+1)-K/R,

(ii) if (0 =< *p*-K/R) then go to (iii),

else C = *p*+1.

(iii) if (0 =< *p*-1-K/R) then C=*p*-1,

else C = *p*.

(3) The input sequence of the interleaver is written into the RxC rectangular matrix row by row starting form row 0.

Third Stage:

(1) Perform the inter-row permutation based on the following P(*j*) (*j*=0,1, ..., R-1) patterns, where P(*j*) is the original row position of the *j*-th permuted row.

P_A: {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 10, 8, 13, 17, 3, 1, 16, 6, 15, 11} for R=20

P_B: {19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 16, 13, 17, 15, 3, 1, 6, 11, 8, 10} for R=20

P_C: {9, 8, 7, 6, 5, 4, 3, 2, 1, 0} for R=10

The usage of these patterns is as follows:

Block length K: P(*j*)

320 to 480-bit: P_A

481 to 530-bit: P_C

531 to 2280-bit: P_A

2281 to 2480-bit: P_B

2481 to 3160-bit: P_A

3161 to 3210-bit: P_B

3211 to 5114-bit: P_A

(2) The output of the mother interleaver is the sequence read out column by column from the permuted R $\times$ C matrix starting from column 0.

Table 2: Table of prime p and associated primitive root

p	g_0	*p*~~P~~	g_0	*p*	g_0	*p*~~P~~	g_0	*p*	g_0
17	3	59	2	103	5	157	5	211	2
19	2	61	2	107	2	163	2	223	3
23	5	67	2	109	6	167	5	227	2
29	2	71	7	113	3	173	2	229	6
31	3	73	5	127	3	179	2	233	3
37	2	79	3	131	2	181	2	239	7
41	6	83	2	137	3	191	19	241	7
43	3	89	3	139	2	193	5	251	6
47	5	97	5	149	2	197	2	257	3
53	2	101	2	151	6	199	3		

4.2.13.1 Relation between input and output of 1st interleaving in uplink

The bits input to the 1st interleaving are denoted by $t_{i1}, t_{i2}, t_{i3}, \ldots, t_{iT_i}$, where *i* is the TrCH number and ~~E~~T_i the number of bits. Hence, $x_{ik} = t_{ik}$ and $X_i = T_i$.

The bits output from the 1st interleaving are denoted by $d_{i1}, d_{i2}, d_{i3}, \ldots, d_{iT_i}$, and $d_{ik} = y_{ik}$.

4.2.6 Radio frame segmentation

When the transmission time interval is longer than 10 ms, the input bit sequence is segmented and mapped onto consecutive radio frames. Following rate matching in the DL and radio frame size equalisation in the UL the input bit sequence length is guaranteed to be an integer multiple of F_i.

The input bit sequence is denoted by $x_{i1}, x_{i2}, x_{i3}, \ldots, x_{iX_i}$ where *i* is the TrCH number and X_i is the number bits. The *Fi* output bit sequences per TTI are denoted by $y_{i,n_i1}, y_{i,n_i2}, y_{i,n_i3}, \ldots, y_{i,n_iY_i}$ where n_i is the radio frame number in current TTI and Y_i is the number of bits per radio frame for TrCH *i*. The output sequences are defined as follows:

$y_{i,n_ik} = x_{i,((n_i-1)Y_i)+k}$, $n_i = 1 \ldots F_i$, ~~j~~$k = 1 \ldots Y_I$

4.2.8 TrCH multiplexing

Every 10 ms, one radio frame from each TrCH is delivered to the TrCH multiplexing. These radio frames are serially multiplexed into a coded composite transport channel (CCTrCH). The Transport channels are multiplexed to the frame in the ascending order of DCH Ids. These DCH Ids are assigned to L1 by L2.

The bits input to the TrCH multiplexing are denoted by $f_{i1}, f_{i2}, f_{i3}, \ldots, f_{iV_i}$, where *i* is the TrCH number and V_i is the number of bits in the radio frame of TrCH *i*. The number of TrCHs is denoted by *I*. The bits output from TrCH multiplexing are denoted by $s_1, s_2, s_3, \ldots, s_S$, where *S* is the number of bits, i.e. $S = \sum_i V_i$. The TrCH multiplexing is defined by the following relations:

4.2.9.2 Insertion of DTX indication bits with flexible positions

Note: ~~Below, it is assumed that all physical channels belonging to the same CCTrCH use the same SF. Hence,~~ U_p=U=constant, since all physical channels belonging to the same CCTrCH use the same SF.

This step of inserting DTX indication bits is used only if the positions of the TrCHs in the radio frame are flexible. The DTX indication bits shall be placed at the end of the radio frame. Note that the DTX will be distributed over all slots after 2nd interleaving.

SFN(System Frame Number)

- synchronisation TS 25.211)
of SFN field is 12 bits
,
- SFN is multiplexed with a BCH transport block (see).

Figure 9 SFN multiplexing